CIPOS™ Maxi CoolSiC™ MOSFET IPM

IM12S60EA2

Description

The CIPOS™ Maxi CoolSiC™ MOSFET IPM family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs. It is designed to operate as high-performance inverter for demanding motor drive applications and active power factor correction. The product concept is specially adapted to power applications, which need good thermal performance and electrical isolation as well as EMI save control and overload protection. Three phase inverter with 1200 V CoolSiC MOSFETs are combined with an optimized 6-channel SOI gate driver for excellent electrical performance. The bodydiodes of CoolSiC MOSFETs can be used as free-wheeling diode and turning on the MOSFET during bodydiode conduction (synchronous rectification) can be used to reduce losses further.

Features

- Fully isolated Dual In-Line molded module with AlN DCB substrate
- 1200 V CoolSiC MOSFETs technology with turn-off stability thanks to higher $V_{GS(th)}$
- 1200 V C5SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11 V for signal transmission at V_{BS} = 15 V
- Integrated bootstrap functionality
- Over current shutdown and under-voltage lockout at all channels
- Built-in NTC thermistor for temperature monitor
- Low side source pins accessible for phase current monitoring (open source)
- Anti-cross conduction functionality
- All of 6 switches turn off during protection
- Fault reporting, programmable fault clear timing and enable input
- Lead-free terminal plating; RoHS compliant

Potential applications

Fans & pumps drives, high-performance motor drives, and active harmonic filter for HVAC

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Part Ordering Table

Product name	Package type	Standard pack		Orderable part number
		Form	MOQ	
IM12S60EA2	DIP 36x23D	14 pcs / tube	280	IM12S60EA2XKMA1

Table of contents

1 Internal electrical schematic

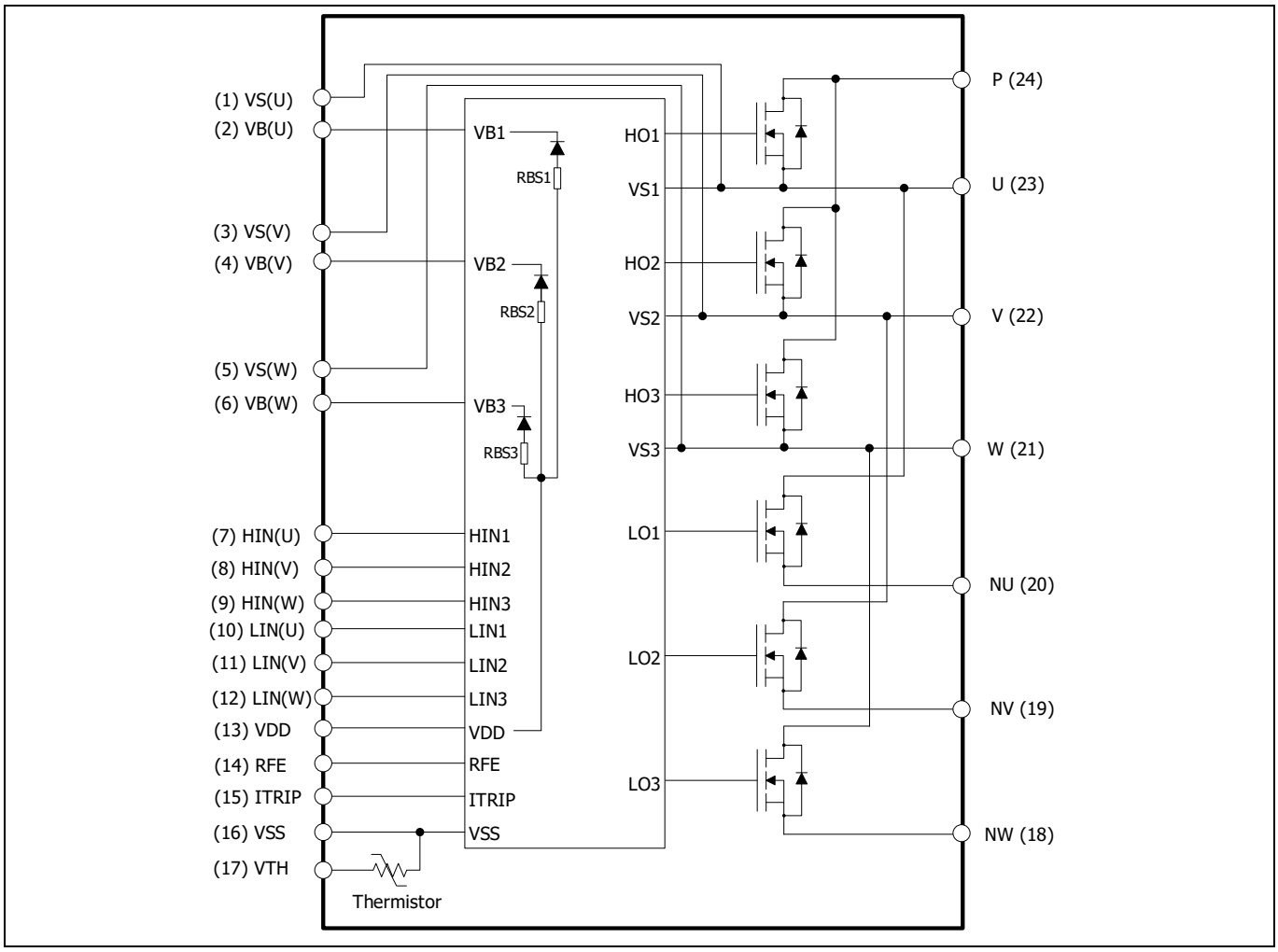


Figure 1 Internal electrical schematic

2 Pin configuration

2.1 Pin assignment

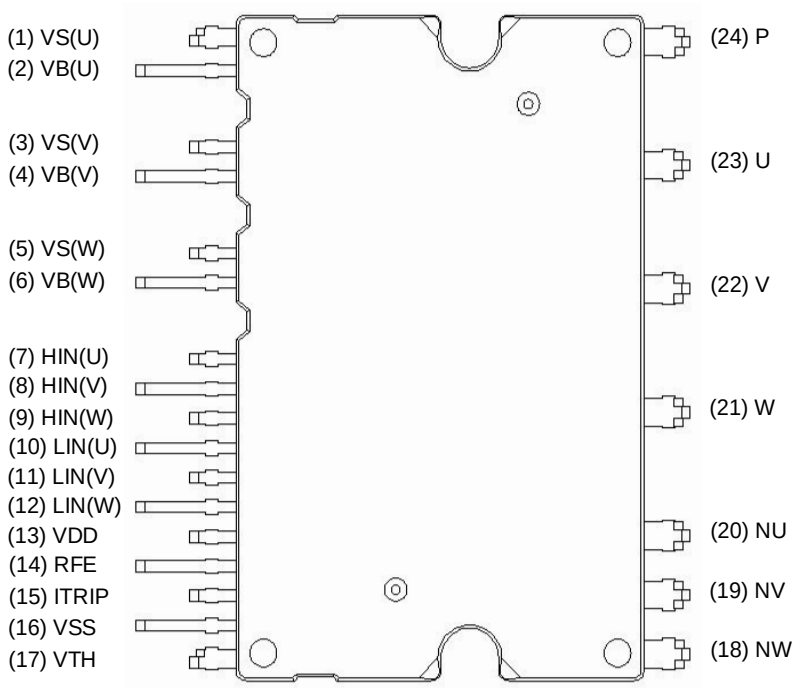


Figure 2 Module pinout

Table 2 Pin assignment

Pin number	Pin name	Pin description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	RFE	Programmable fault clear time, fault output, enable input
15	ITRIP	Over current shutdown input

Pin configuration

Pin number	Pin name	Pin description
16	VSS	Low side control negative supply
17	VTH	Thermistor terminal
18	NW	W-phase low side source
19	NV	V-phase low side source
20	NU	U-phase low side source
21	W	Motor W-phase output
22	V	Motor V-phase output
23	U	Motor U-phase output
24	P	Positive bus input voltage

2.2 Pin description

HIN (U, V, W) and LIN (U, V, W) (Low side and high side control pins, Pin 7 - 12)

These pins are positive logic, and they are responsible for the control of the integrated MOSFETs. The schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time $t_{FIL,IN}$. The filter acts according to Figure 4.

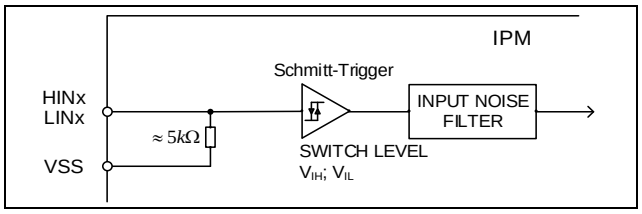


Figure 3 Input pin structure

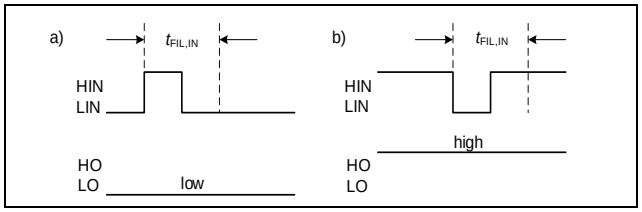


Figure 4 Input filter timing diagram

It is not recommended for proper work to provide input pulse-width lower than 1 µs.

The integrated gate driver provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e., HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 300 ns is also provided by driver IC, to reduce cross-conduction of the external power switches.

RFE (Fault / Fault clear time / Enable, Pin 14)

The RFE pin combines three functions in one pin: programmable fault clear time by RC-network, fault-out and enable input.

The programmable fault-clear time can be adjusted by RC network, which is external pull-up resistor and capacitor. For example, typical value is about 1ms at 2 MΩ and 1 nF.

The fault-out indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP.

The microcontroller can pull this pin low to disable the IPM functionality. This is enabling function.

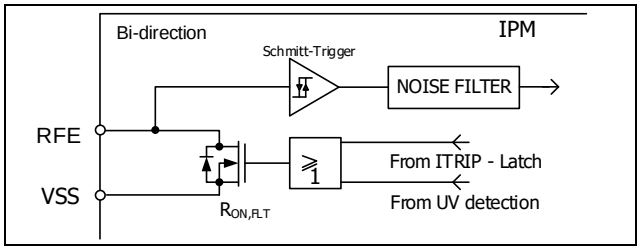


Figure 5 Internal circuit at pin RFE

Pin configuration

VTH (Thermistor, Pin 17)

The VTH pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

ITRIP (Over current detection function, Pin 15)

The IPM provides an over current detection function by connecting the ITRIP input with the MOSFET drain current feedback. The ITRIP comparator threshold (typ. 0.5 V) is referenced to VSS ground. An input noise filter (t_{ITRIP} = typ. 500 ns) prevents the driver to detect false over-current events.

Over current detection generates a shutdown of all outputs of the gate driver after the shutdown propagation delay of typically 1µs.

Fault-clear time is set to typical 1.1ms at R_{RCIN} = 2 MΩ and C_{RCIN} = 1 nF.

VDD, VSS (Low side control supply and reference, Pin 13, 16)

VDD is the control supply, and it provides power both to input logic and to output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.2 V is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below V_{DDUV-} = 11.2 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB (U, V, W) and VS (U, V, W) (High side supplies, Pin 1 - 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device source voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.2 V and a falling threshold of V_{BSUV-} = 10.2 V.

VS (U, V, W) provide a high robustness against negative voltage in respect of VSS of -50 V transiently. This ensures very stable designs even under rough conditions.

NW, NV, NU (Low side source, Pin 18 - 20)

The low side sources are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible to avoid unnecessary inductive voltage drops.

W, V, U (High side source and low side drain, Pin 21 - 23)

These pins are motor U, V, W input pins.

P (Positive bus input voltage, Pin 24)

The high side MOSFETs are connected to the bus voltage. It is noted that the bus voltage does not exceed 950 V.

3 Absolute maximum ratings

(V_{DD} = 18 V and T_{VJ} = 25°C, if not stated otherwise)

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_{VJ}		-40 ~ 150	°C
Isolation test voltage	V_{ISO}	1min, RMS, f = 60Hz	2500	V

3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{DSS}		1200	V
DC link supply voltage of P-N[1]	V_{PN}	Applied between P-N	900	V
DC link supply voltage (surge) of P-N[2]	$V_{PN(surge)}$	Applied between P-N	1000	V
Output phase current[3] limited by $T_{VJ(max)}$	I_O		±26.7	A_{rms}
Maximum output phase peak current[4]	I_{OM}		±50	A
Power dissipation per MOSFET	P_{tot}	T_C = 25°C	142	W
Short circuit withstand time	t_{SC}	$V_{DC} \leq$ 600 V, V_{DD} = 15 V $T_{VJ(start)}$ = 25°C	3	µs

3.3 Control section

Description	Symbol	Condition	Value	Unit
High Side offset voltage	V_S		1200	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		1200	V
Module control supply voltage	V_{DD}		-0.3 ~ 20	V
High side floating supply voltage (V_B reference to V_S)	V_{BS}		-0.3 ~ 20	V
Input voltage (LIN, HIN, ITRIP, RFE)	V_{IN}		-0.3 ~ V_{DD} + 0.3	V
Logic ground	V_{SS}		0 ~ V_{DD} + 0.3	V
Allowable Vs offset supply transient relative to V_{SS}	dV_S / dt		50	V/ns

[1] Verified by design. External stray inductance by PCB trace is limited by $V_{PN(surge)}$
[2] Verified by design.
[3] Verified by design. Based on sinusoidal output current waveform
[4] Verified by design. Non-repetitive such as protection event

4 Thermal characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single MOSFET thermal resistance, junction-case	R_{thJC}	Single-chip heating	-	-	0.88	K/W
Package Stray Inductance[1]	L_p	P to N_U, N_V, N_W	-	26	-	nH

[1] The package parasitic stray inductance per phase based on AQG324 7.1 (IEC 60747-15:2012)

5 Recommended operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	400	600	800	V
Low side supply voltage	V_{DD}	15.0	18.0	20.0	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	14.0	17.0	20.0	V
Logic input voltages LIN, HIN, ITRIP, RFE	V_{IN}	0	-	5	V
PWM carrier frequency at V_{DD} = 18 V	F_{PWM}	-	-	40	kHz
External dead time between HIN & LIN	DT	0.5	-	-	µs
Voltage between VSS - N (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1	-	-	µs
Control supply variation	$\Delta V_{BS,}$ ΔV_{DD}	-1 -1	- -	1 1	V/µs

6 Static parameters

(V_{DD} = 18 V and T_{VJ} = 25°C, if not stated otherwise)

6.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 13 A, V_{IN} = 5 V V_{DD} = 18 V, T_{VJ} = 25°C 150°C	- -	60 100	83 -	mΩ
Drain-source leakage current[1]	I_{DSS}	V_{DS} = 1200V	-	-	1	mA
Diode forward voltage	V_{SD}	I_{SD} = 13 A, V_{IN} = 0 V T_{VJ} = 25°C 150°C	- -	4.1 3.9	5.2 -	V

6.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (LIN, HIN)	V_{IH}		-	2.0	2.3	V
Logic "0" input voltage (LIN, HIN)	V_{IL}		0.7	0.9	-	V
ITRIP positive going threshold	$V_{IT,TH+}$		475	500	525	mV
ITRIP input hysteresis	$V_{IT,HYS}$		-	55	-	mV
V_{DD} and V_{BS} supply under voltage positive going threshold	V_{DDUV+} V_{BSUV+}		11.5 10.5	12.2 11.2	13.0 12.0	V
V_{DD} / V_{BS} supply under voltage negative going threshold	V_{DDUV-} V_{BSUV-}		10.5 9.5	11.2 10.2	12.0 11.0	V
V_{DD} / V_{BS} supply under voltage lockout hysteresis	V_{DDUVH} V_{BSUVH}		-	1	-	V
Quiescent V_{Bx} supply current (V_{Bx} only)	I_{QBS}	H_{IN} = 0 V	-	200	-	µA
Quiescent V_{DD} supply current (V_{DD} only)	I_{QDD}	L_{INX} = 0 V, H_{INX} = 5 V	-	1.2	-	mA
Input bias current for LIN, HIN	I_{IN+}	V_{IN} = 5 V	-	1	-	mA
Input bias current for ITRIP	I_{ITRIP+}	V_{ITRIP} = 5 V	-	30	100	µA
Input bias current for RFE	I_{RFE}	V_{RFE} = 5 V, V_{ITRIP} = 0 V	-	-	5	µA
RFE output voltage	V_{RFE}	I_{RFE} = 10 mA, V_{ITRIP} = 1 V	-	0.4	-	V
V_{RFE} positive going threshold	$V_{RFE,TH+}$		-	.9	2.3	V
V_{RFE} negative going threshold	$V_{RFE,TH-}$		0.7	0.9	-	V

[1] Included gate driver IC & other phase MOSFET leakage current due to internal structure.

Static parameters

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Bootstrap diode forward voltage	V_{F_BSD}	I_F = 0.3 mA	-	0.9	-	V
Bootstrap diode resistance	R_{BSD}	Between V_F = 4 V and V_F = 5 V	-	120	-	Ω

7 Dynamic parameters

(V_{DD} = 18 V and T_{VJ} = 25°C, if not stated otherwise)

7.1 Inverter section

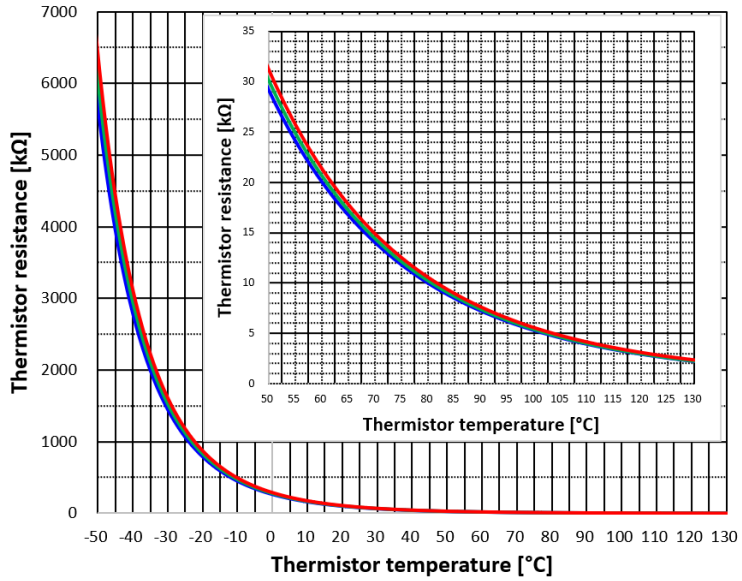
Description		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
High side	Turn-on propagation delay time	t_{on}	V_{HIN} = 5 V, V_{DC} = 600 V, I_D = 25 A	-	780	-	ns
	Turn-on rise time	t_r		-	30	-	ns
	Turn-on switching time	$t_{c(on)}$		-	60	-	ns
	Reverse recovery time	t_{rr}		-	40	-	ns
	Turn-off propagation delay time	t_{off}	V_{HIN} = 0 V, V_{DC} = 600 V, I_D = 25 A	-	750	-	ns
	Turn-off fall time	t_f		-	20	-	ns
	Turn-off switching time	$t_{c(off)}$		-	40	-	ns
	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	0.55 0.72	- -	mJ
	MOSFET turn-off energy	E_{off}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	0.35 0.48	- -	mJ
	Bodydiode recovery energy	E_{rec}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	0.10 0.14	- -	mJ
Low side	Turn-on propagation delay time	t_{on}	V_{LIN} = 5 V, V_{DC} = 600 V, I_D = 25 A	-	870	-	ns
	Turn-on rise time	t_r		-	70	-	ns
	Turn-on switching time	$t_{c(on)}$		-	70	-	ns
	Reverse recovery time	t_{rr}		-	40	-	ns
	Turn-off propagation delay time	t_{off}	V_{LIN} = 0 V, V_{DC} = 600 V, I_D = 25 A	-	700	-	ns
	Turn-off fall time	t_f		-	20	-	ns
	Turn-off switching time	$t_{c(off)}$		-	30	-	ns
	MOSFET turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	1.03 1.19	- -	mJ
	MOSFET turn-off energy	E_{off}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	0.17 0.23	- -	mJ
	Bodydiode recovery energy	E_{rec}	V_{DC} = 600 V, I_D = 25 A T_{VJ} = 25°C 150°C	- -	0.03 0.06	- -	mJ
Short circuit propagation delay time		t_{SCP}	From $V_{IT,TH+}$ to 10% I_{SC}	-	1000	-	ns

7.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time ITRIP	t_{ITRIP}	V_{ITRIP} = 1 V	-	500	-	ns
Input filter time at LIN, HIN for turn on and off	$t_{FIL,IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	350	-	ns
Fault clear time after ITRIP-fault	$t_{FLT,CLR}$	V_{ITRIP} = 1V, $V_{pull-up}$ = 5V R_{RFE} = 2 MΩ, C_{RFE} = 1 nF		1.1	-	ms
ITRIP to Fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or 5 V, V_{ITRIP} = 1V	-	650	900	ns
Internal deadtime	DT_{IC}	V_{IN} = 0 or V_{IN} = 5 V	300	-	-	ns
Matching propagation delay time (On & Off) all channels	M_T	External dead time > 500ns	-	-	130	ns

8 Thermistor characteristics

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resistance	T_{NTC} = 25°C	R_{NTC}	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient)		B (25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	29.151	30.157	31.178
55	24.100	24.908	25.727
60	20.018	20.669	21.329
65	16.701	17.229	17.763
70	13.994	14.424	14.858
75	11.774	12.125	12.479
80	9.946	10.234	10.523
85	8.434	8.670	8.908
90	7.177	7.373	7.569
95	6.130	6.292	6.454
100	5.253	5.388	5.523
105	4.510	4.629	4.748
110	3.884	3.990	4.096
115	3.356	3.449	3.544
120	2.908	2.991	3.075
125	2.527	2.601	2.676

Figure 6 Thermistor resistance – temperature curve and table

(For more information, please refer to the application note 'AN2020-41 CIPOS™ Maxi application note')

9 Mechanical characteristics and ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Backside curvature	Refer to Figure 8	0	-	150	µm
Weight		-	6.94	-	g

10 Qualification information

UL Certification	File number E314539	
Moisture sensitivity level (SOP package only)	-	
RoHS Compliant	Yes (Lead-free terminal plating)	
ESD (Electrostatic Discharge)	HBM (Human body model) Class	2
	CDM (Charged Device model) Class	C2a

11 Diagrams and tables

11.1 T_C measurement point

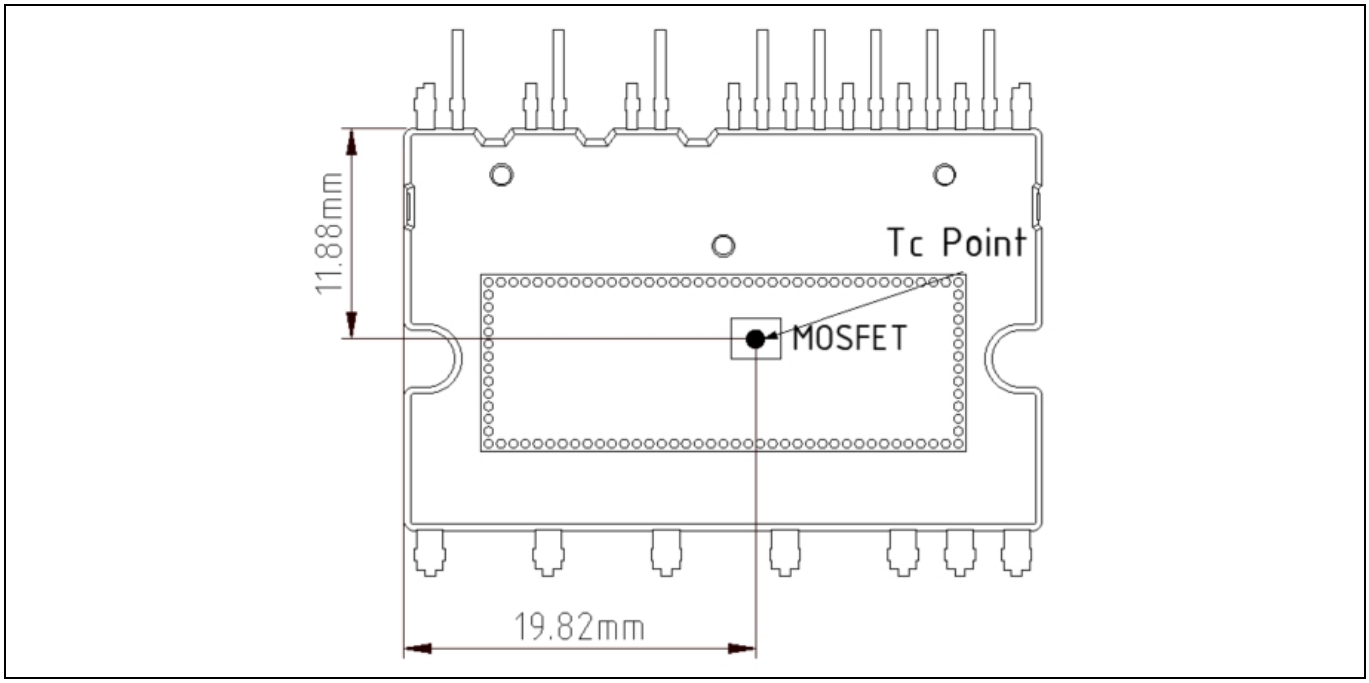


Figure 7 T_C measurement point[1]

11.2 Backside curvature measurement point

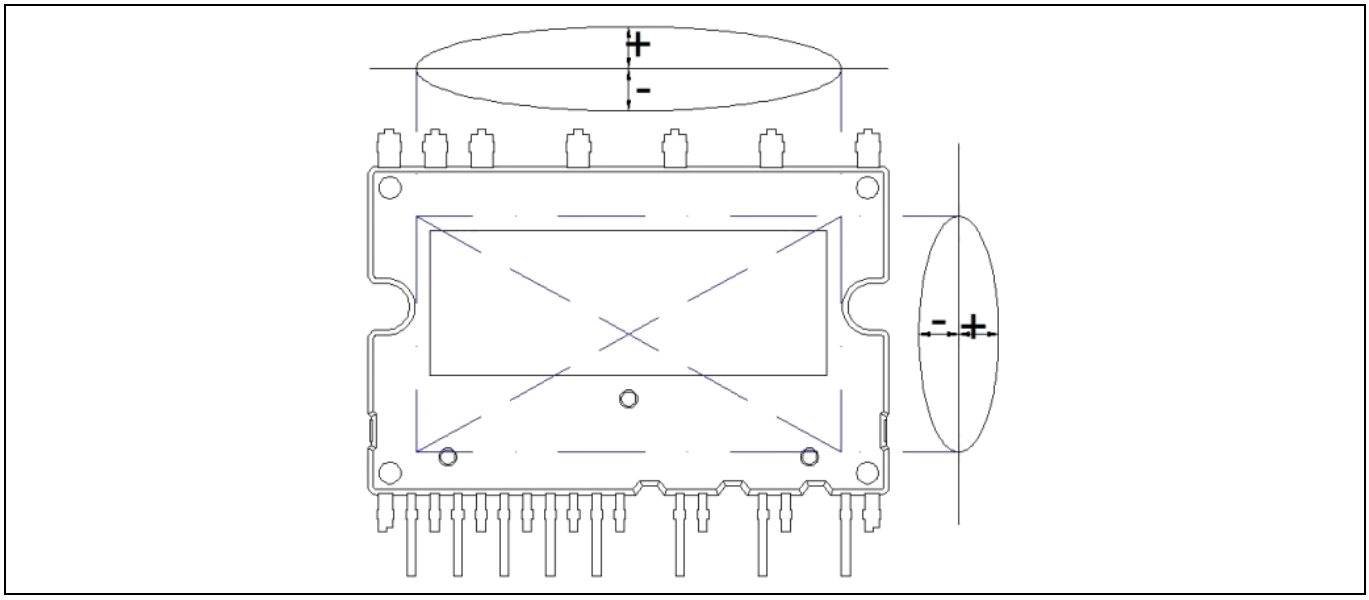


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching test circuit

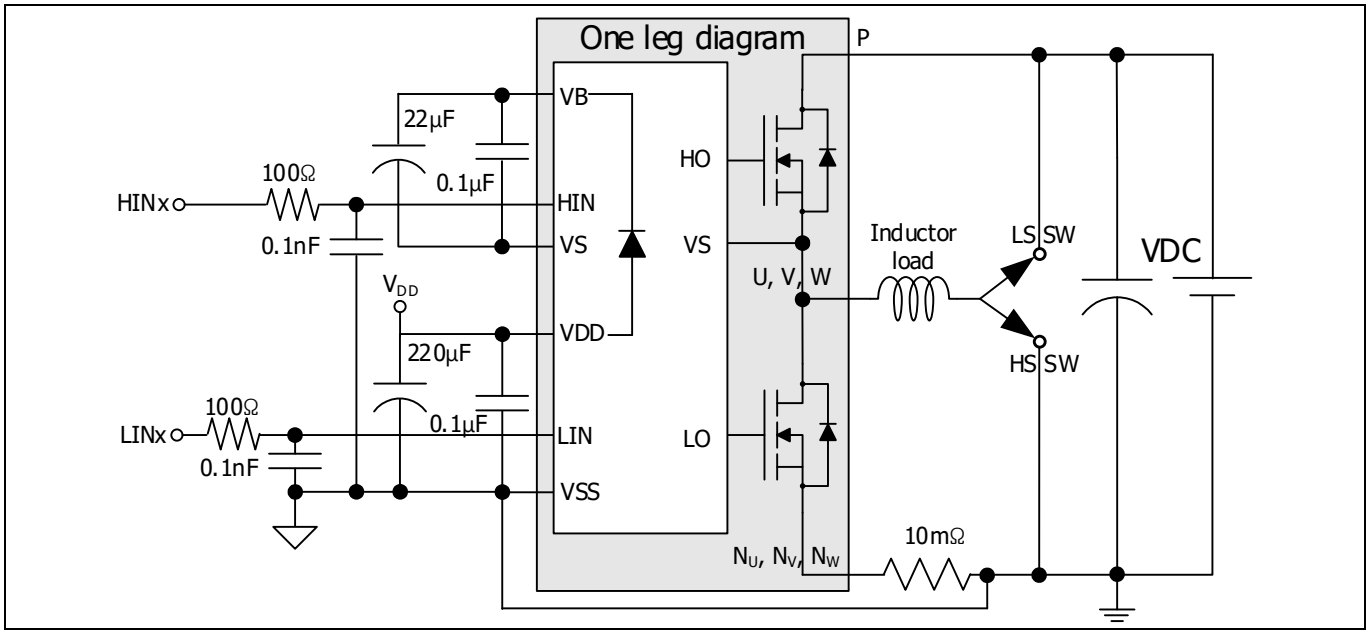


Figure 9 Switching test circuit

11.4 Switching times definition

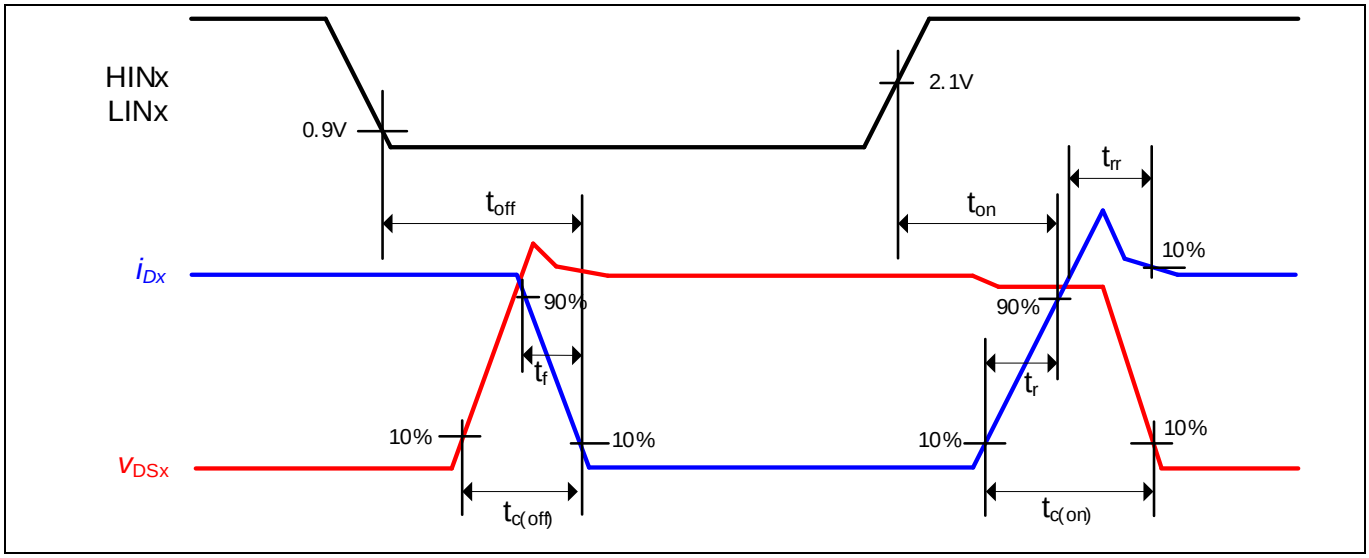


Figure 10 Switching times definition

12 Application guide

12.1 Typical application schematic

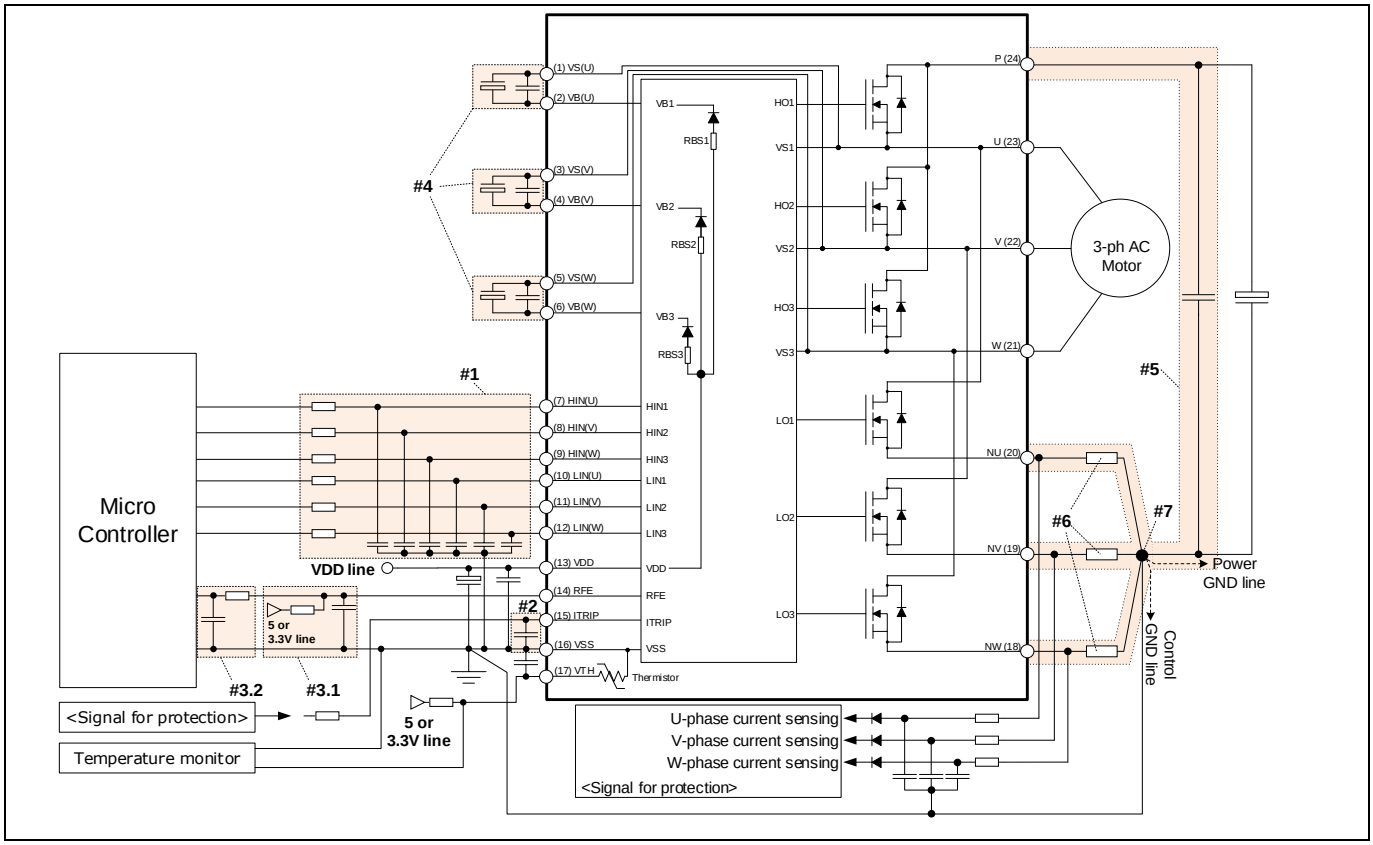


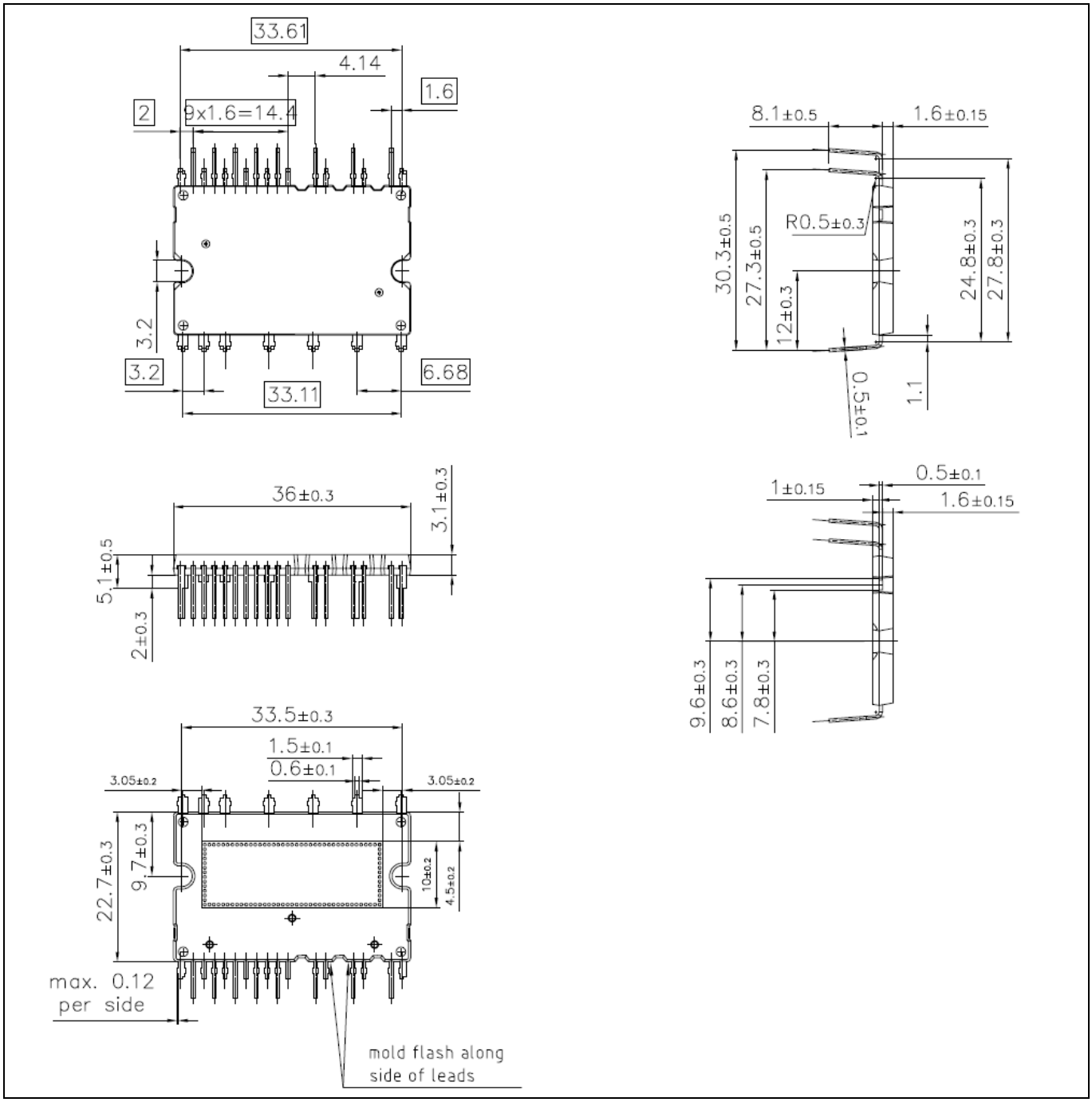
Figure 11 Typical application circuit

1. Input circuit
   - To reduce input signal noise by high-speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω, 1 nF)
   - C_{IN} should be placed as close to V_{SS} pin as possible.
2. Itrip circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to Itrip and V_{SS} pins as possible.
3. RFE circuit

   3.1 Pull-up resistor (R_{RFE}) and pull-down capacitor (C_{RFE})
   - RFE output is an open drain output. This signal line should be pulled up to the positive side of the 5 V / 3.3 V control power supply voltage (V_{CTR}) with a proper resistor R_{FE}.
   - The fault-clear time is adjusted by RC network of R_{RFE} and C_{RFE} and pull-up voltage.
     - $t_{FLTCLR} = -R_{RFE} \cdot C_{RFE} \cdot \ln(1 - V_{RFE,TH+}/V_{CTR})$ + internal fault-clear time 160 µs
     - $t_{FLTCLR} = -2\ M\Omega \times 1\ nF \times \ln(1 - 1.9 / 5\ V) + 160\mu s \cong 1.1ms$ at $R_{RFE} = 2\ M\Omega$, $C_{RFE} = 1\ nF$ and $V_{CTR} = 5\ V$
     - A pull-up resistor is limited to max. 2 MΩ
     - In case of V_{CTR} is higher than 5 V, the R_{RFE} needs to be at least 200 kΩ to limit the IC power dissipation.

   3.2 RC filter
   - It is recommended that RC filter be placed as close to the controller as possible.
4. VB-VS circuit
   - Capacitor for Low side floating supply voltage should be placed as close to VB and VS pins as possible.
5. Snubber capacitor
   - The wiring between IPM and snubber capacitor including shunt resistor should be as short as possible.
6. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance.
7. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

13 Package outline



Revision history

Document version	Date of release	Description of changes
2.0	2025-04-14	1st release

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