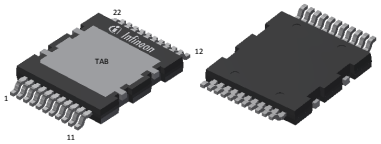
# SiC MOSFET

Q-DPAK

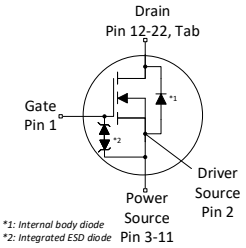
## CoolSiC™ MOSFET 750 V G2



Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 750 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.

## Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class $R_{DS(on)}$ x $Q_{fr}$
- Excellent $R_{DS(on)}$ x $Q_{oss}$ and $R_{DS(on)}$ x $Q_G$
- Unique combination of low $C_{rss}/C_{iss}$ and high $V_{GS(th)}$
- Infineon proprietary die attach technology
- Cutting edge TSC package with material group I
- Driver source pin available
- Best-in-class $R_{DS(on)}$ in SMD device




## Benefits

- Enhanced robustness and reliability for bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

## Potential applications

- Solid state relays and circuit breakers
- EV charging infrastructure
- Solar PV inverters and UPS
- Energy storage and battery formation
- Telecom and Server SMPS

## Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction. When paralleling MOSFETs the placement of the gate resistor is generally recommended to be in series to the Driver Source instead of the Gate.*

**Table 1 Key performance parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DSS}$ over full $T_{j,range}$ | 750 | V |
| $R_{DS(on),typ}$ | 60 | mΩ |
| $R_{DS(on),max}$ | 78 | mΩ |
| $Q_{G,typ}$ | 20 | nC |
| $I_{D,pulse}$ | 94 | A |
| $Q_{oss,typ}$ @ 500 V | 42 | nC |
| $E_{oss,typ}$ @ 500 V | 7.5 | µJ |

| Part number | Package | Marking | Related links |
|---|---|---|---|
| IMDQ75R060M2H | PG-HDSOP-22 | 75R060M2 | see Appendix A |

# Table of contents

# 1 Maximum ratings

at $T_j$ = 25°C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.
"Linear mode" operation is not recommended. For assessment of potential "linear mode" operation, please contact Infineon sales office.

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous DC drain current [1] | $I_{DDC}$ | - | - | 30 | A | $T_c$ = 25°C |
| Continuous DC drain current | $I_{DDC}$ | - | - | 21 | A | $T_c$ = 100°C |
| Peak drain current [2] | $I_{DM}$ | - | - | 94 | A | $T_c$ = 25°C, $V_{GS}$ = 18 V |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 86 | mJ | $I_D$ = 3.2 A, $V_{DD}$ = 50 V; see table 11 |
| Avalanche energy, repetitive | $E_{AR}$ | | | 0.43 | | |
| Avalanche current, single pulse | $I_{AS}$ | - | - | 3.2 | A | - |
| MOSFET *dv/dt* ruggedness | *dv/dt* | - | - | 200 | V/ns | $V_{DS}$= 0…500 V |
| Gate source voltage (static) [3] | $V_{GS}$ | -7 | - | 23 | V | - |
| Gate source voltage (transient) | $V_{GS}$ | -11 | - | 25 | V | $t_p \leq$ 500 ns, duty cycle ≤ 1% |
| Power dissipation | $P_{tot}$ | - | - | 128 | W | $T_c$ = 25°C |
| Storage temperature | $T_{stg}$ | -55 | - | 150 | °C | - |
| Operating junction temperature | $T_j$ | | | 175 | | |
| Extended operating junction temperature [4] | $T_j$ | - | - | 200 | °C | ≤ 100 h in the application lifetime |
| Mounting torque | - | - | - | n.a | Ncm | - |
| Continuous reverse drain current [1] | $I_{SDC}$ | - | - | 30 | A | $V_{GS}$ = 18 V, $T_c$ = 25°C |
| | | | | 21 | | $V_{GS}$ = 0 V, $T_c$ = 25°C |
| Peak reverse drain current [2] | $I_{SM}$ | - | - | 94 | A | $T_c$ = 25°C, $t_p \leq$ 250 ns |
| | | | | 26 | | $T_c$ = 25°C |
| Insulation withstand voltage | $V_{ISO}$ | - | - | n.a. | V | $V_{rms}$, $T_c$ = 25°C, $t$ = 1 min |

[1] Limited by $T_{j,max}$.

[2] Pulse width $t_{pulse}$ limited by $T_{j,max}$.

[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

[4] Up to 7500 temperature cycles, where maximum delta $T$ is limited to 100K.

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{th(j-c)}$ | - | - | 1.17 | °C/W | Not subject to production test. Parameter verified by design/characterization according to JESD51-14. |
| Soldering temperature, reflow soldering allowed | $T_{sold}$ | - | - | 260 | °C | reflow MSL1 |

# 3 Operating range

**Table 4 Operating range**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Recommended turn-on voltage | $V_{GS(on)}$ | - | 18 | - | V | - |
| Recommended turn-off voltage | $V_{GS(off)}$ | | 0 | | | |

# 4 Electrical characteristics

at $T_j$ = 25°C, unless otherwise specified

**Table 5 Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source voltage [5] | $V_{DSS}$ | 840 | - | - | V | $V_{GS}$ = 0 V, $I_D$ = 0.30 mA |
| Gate threshold voltage [6] | $V_{GS(th)}$ | 3.5 | 4.5 | 5.6 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 3.0 mA, $T_j$ = 25°C |
| | | - | 3.3 | - | | $V_{DS}$ = $V_{GS}$, $I_D$ = 3.0 mA, $T_j$ = 175°C |
| Zero gate voltage drain current | $I_{DSS}$ | - | 1 | 75 | µA | $V_{DS}$ = 750 V, $V_{GS}$ = 0 V, $T_j$ = 25°C |
| | | | 10 | - | | $V_{DS}$ = 750 V, $V_{GS}$ = 0 V, $T_j$ = 175°C |
| Gate-source leakage current | $I_{GSS}$ | - | - | 1 | µA | $V_{GS}$ = 23V, $V_{DS}$ = 0 V, $T_j$ = 25°C |
| | | | | -1 | | $V_{GS}$ = -7V, $V_{DS}$ = 0 V, $T_j$ = 25°C |
| Forward transconductance | $g_{fs}$ | - | 8.3 | - | S | $I_D$ = 13.8 A, $V_{DS}$ = 20 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 81 | - | mΩ | $V_{GS}$ = 15 V, $I_D$ = 13.8 A, $T_j$ = 25°C |
| | | | 60 | 78 | | $V_{GS}$ = 18 V, $I_D$ = 13.8 A, $T_j$ = 25°C |
| | | | 56 | - | | $V_{GS}$ = 20 V, $I_D$ = 13.8 A, $T_j$ = 25°C |
| Drain-source on-state resistance [7] | $R_{DS(on)}$ | - | 95 | 124 | mΩ | $V_{GS}$ = 18 V, $I_D$ = 13.8 A, $T_j$ = 150°C |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 108 | - | mΩ | $V_{GS}$ = 18 V, $I_D$ = 13.8 A, $T_j$ =175°C |
| Internal gate resistance | $R_{G,int}$ | - | 4.5 | - | Ω | $f$ = 1 MHz |

[5] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

[6] Tested after pre-conditioning pulse at $V_{GS}$ = +20 V. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

[7] Specified by design, not subject to production test.

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 716 | - | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 500 V, $f$ = 250 kHz |
| Reverse transfer capacitance | $C_{rss}$ | | 3.6 | - | | |
| Output capacitance [8] | $C_{oss}$ | | 49 | 64 | | |
| Output charge [8] | $Q_{oss}$ | - | 42 | 55 | nC | calculation based on $C_{oss}$ |
| Effective output capacitance, energy related [9] | $C_{o(er)}$ | - | 60 | - | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0…500 V |
| Effective output capacitance, time related [10] | $C_{o(tr)}$ | - | 84 | - | pF | $I_D$ = constant, $V_{GS}$ = 0 V, $V_{DS}$ = 0…500 V |

## Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Turn-on delay time | $t_{d(on)}$ | - | 6.6 | - | ns | $V_{DD}$ = 500 V, $V_{GS}$ = 0/18 V, $I_D$ = 13.8 A, $R_{G,ext}$ = 1.8 Ω, $L_{stray}$ = 15 nH; see table 10 |
| Rise time | $t_r$ | | 5.6 | | ns | |
| Turn-off delay time | $t_{d(off)}$ | | 12.6 | | ns | |
| Fall time | $t_f$ | | 5.0 | | ns | |
| Turn-ON switching losses [11] | $E_{on}$ | | 32 | | µJ | |
| Turn-OFF switching losses [11] | $E_{off}$ | | 13 | | µJ | |
| Total switching losses [11] | $E_{tot}$ | | 45 | | µJ | |

[8] Maximum specification is defined by calculated six sigma upper confidence bound.

[9] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 500 V.

[10] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 500 V.

[11] MOSFET used in half-bridge configuration without external diode. Parameter verified by characterization according to IEC 60747-8.

## Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Plateau gate to source charge | $Q_{GS(pl)}$ | - | 5.1 | - | nC | $V_{DD}$ = 500 V, $I_D$ = 13.8 A, $V_{GS}$ = 0 to 18 V |
| Gate to drain charge | $Q_{GD}$ | | 4.1 | | | |
| Total gate charge | $Q_G$ | | 20 | | | |

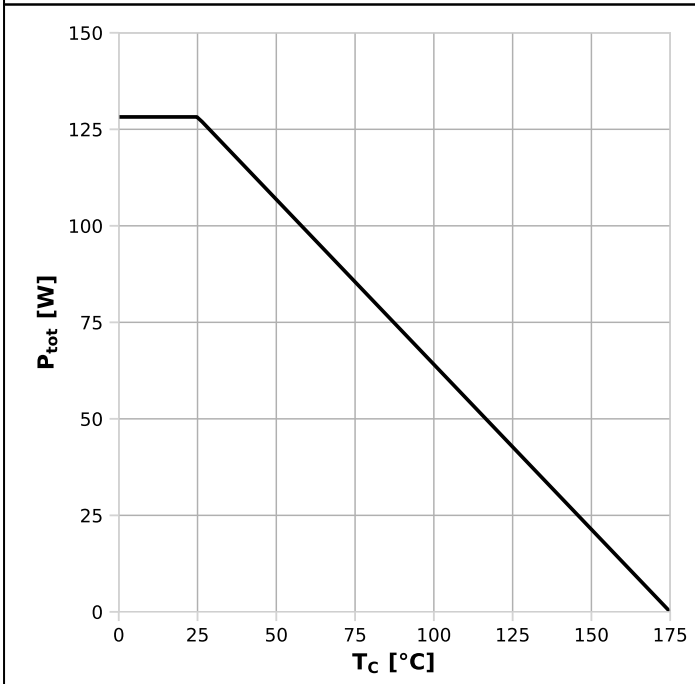
## Table 8 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source reverse voltage | $V_{SD}$ | - | 4.0 | 5.0 | V | $V_{GS}$ = 0 V, $I_S$ = 13.8 A, $T_j$ = 25°C |
| | | | 3.7 | - | | $V_{GS}$ = 0 V, $I_S$ = 13.8 A, $T_j$ = 175°C |
| MOSFET forward recovery time | $t_{fr}$ | - | 5.4 | - | ns | $V_{DD}$ = 500 V, $I_S$ = 13.8 A, $di_S/dt$ = 4000 A/µs; see table 9 |
| MOSFET forward recovery charge [12] | $Q_{fr}$ | | 44 | | nC | |
| MOSFET peak forward recovery current | $I_{frm}$ | | 16 | | A | |

[12] $Q_{fr}$ includes $Q_{oss}$.

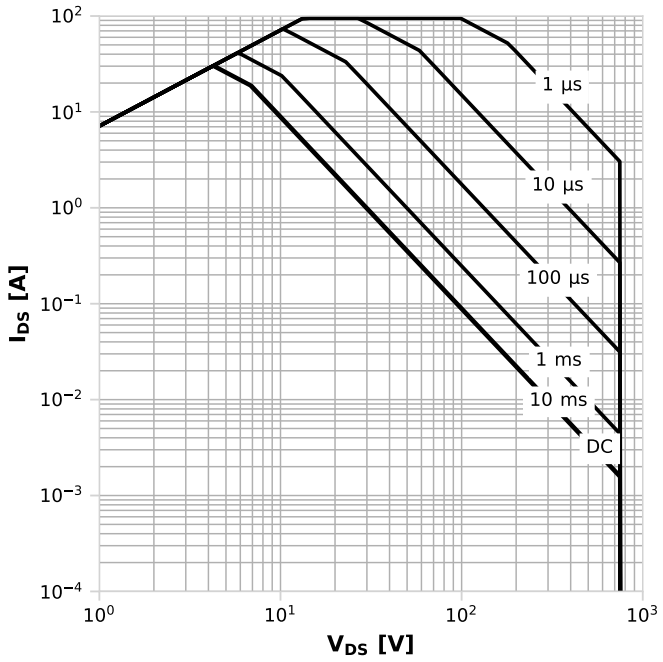
# 5 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



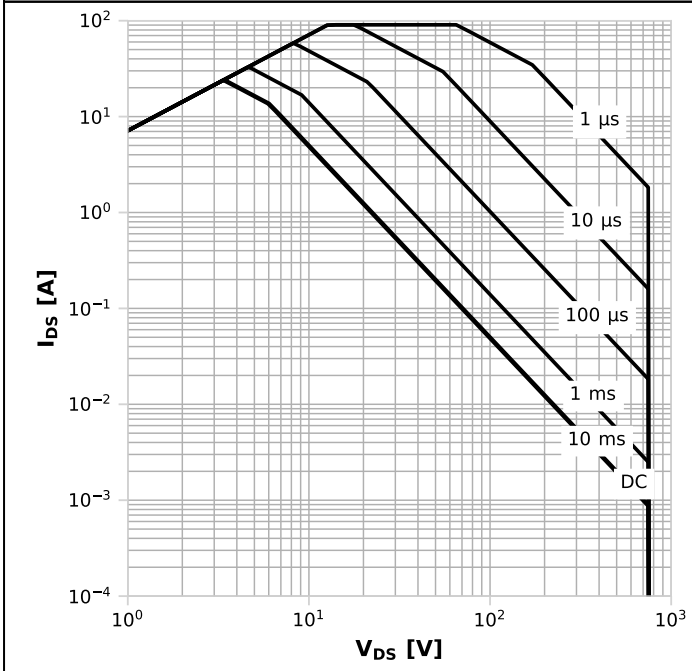

$P_{tot}=f(T_C)$

**Diagram 2: Safe operating area**



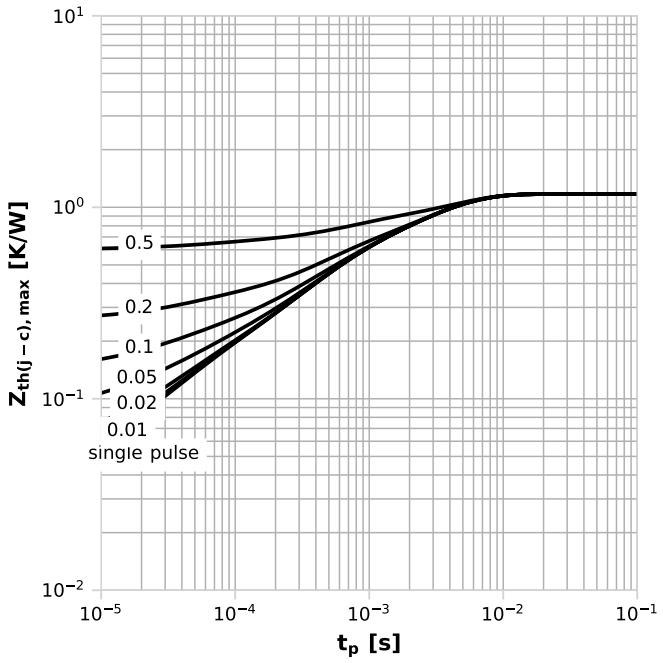

$I_{DS}=f(V_{DS})$; $T_C$=25°C; D=0; parameter: $t_p$

**Diagram 3: Safe operating area**



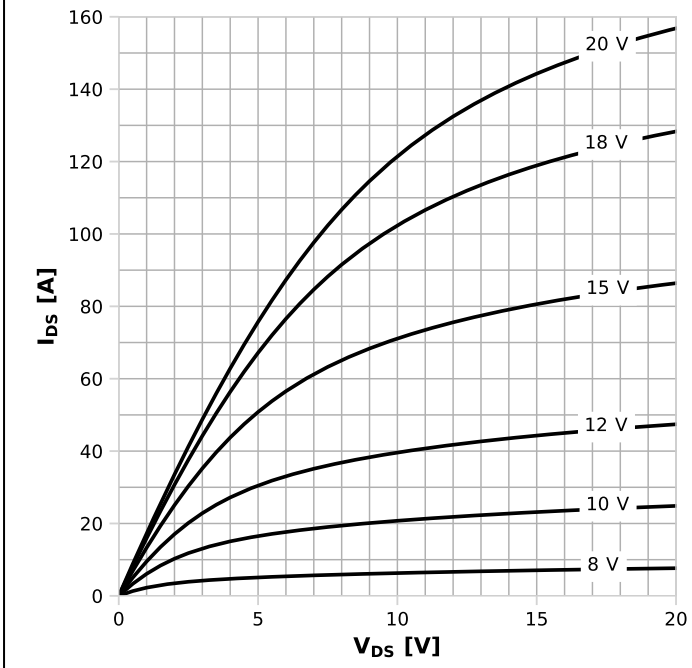

$I_{DS}=f(V_{DS})$; $T_C$=80°C; D=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



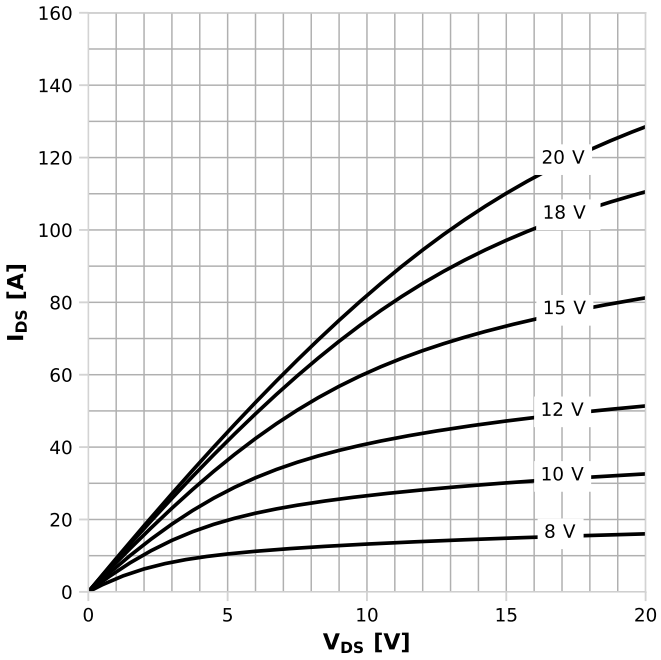

$Z_{th(j-c),max}=f(t_P)$; parameter: $D=t_p/T$

**Diagram 5: Typ. output characteristics**



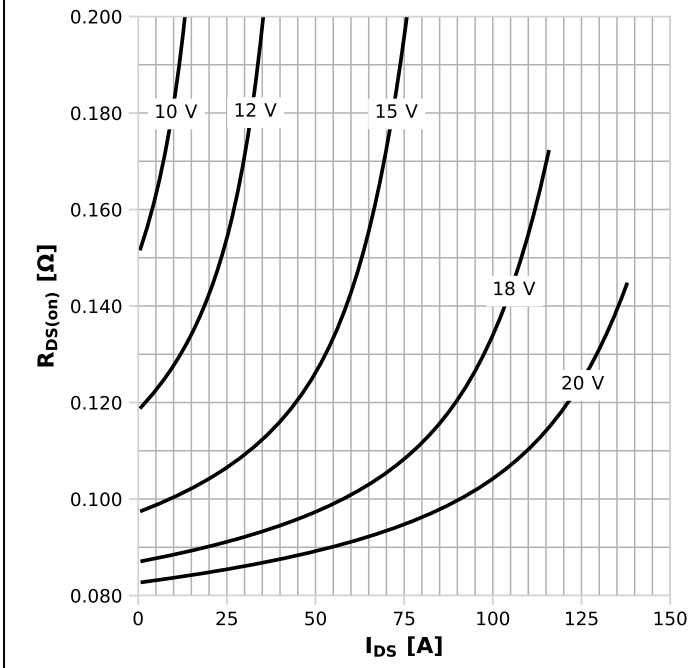

$I_{DS}=f(V_{DS})$; $T_j=25°C$; parameter: $V_{GS}$

**Diagram 6: Typ. output characteristics**



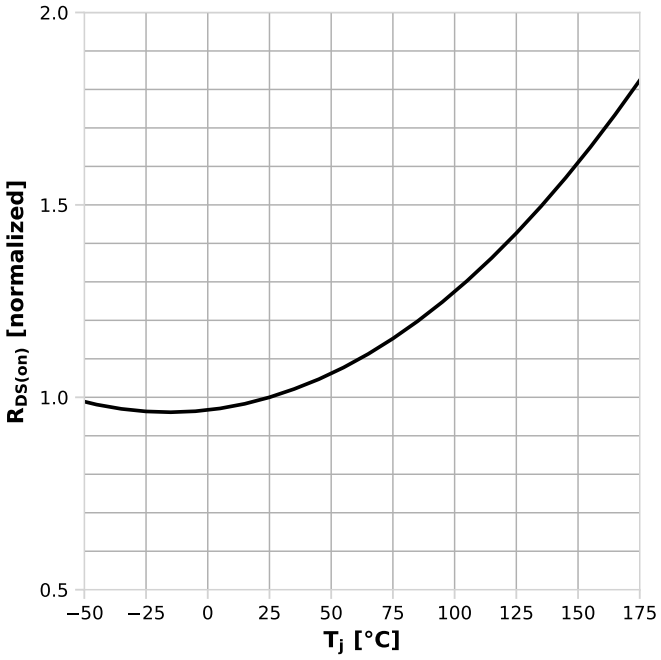

$I_{DS}=f(V_{DS})$; $T_j=175°C$; parameter: $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**

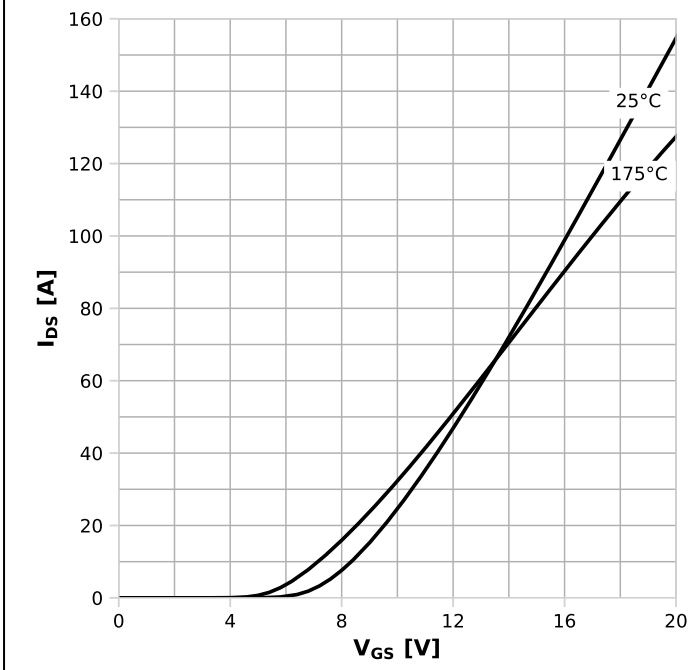
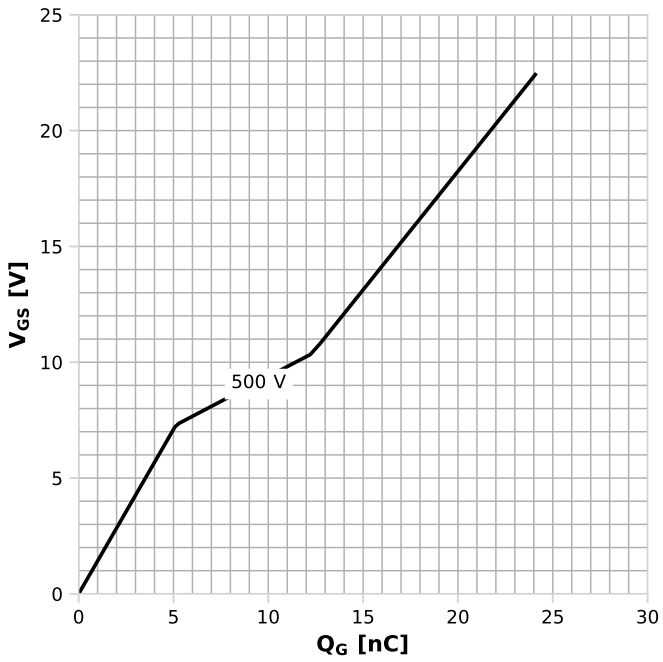


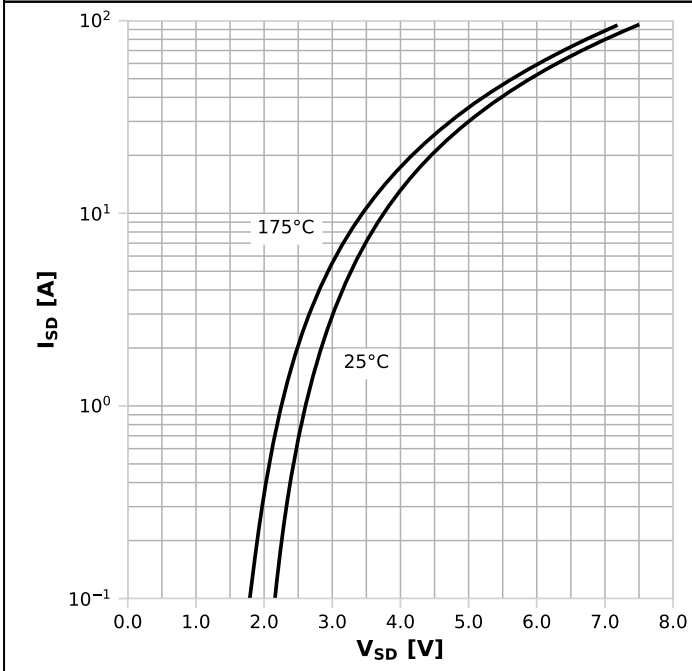
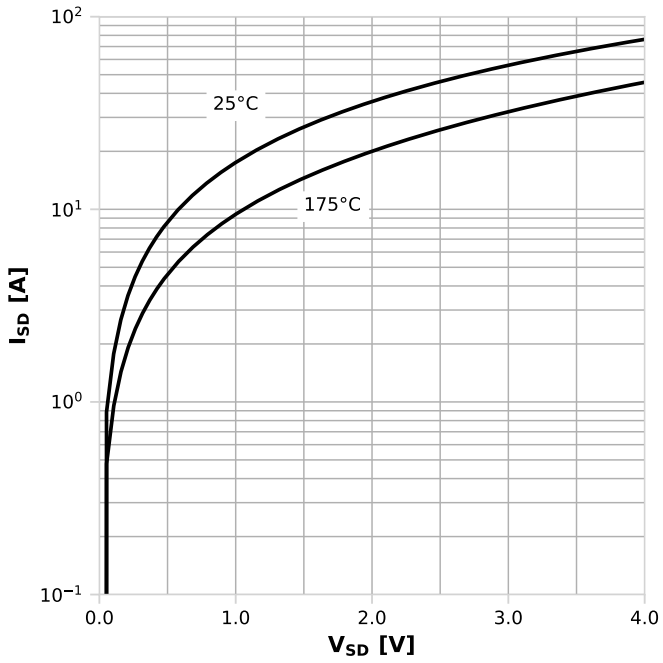

$R_{DS(on)}=f(I_{DS})$; $T_j=125°C$; parameter: $V_{GS}$

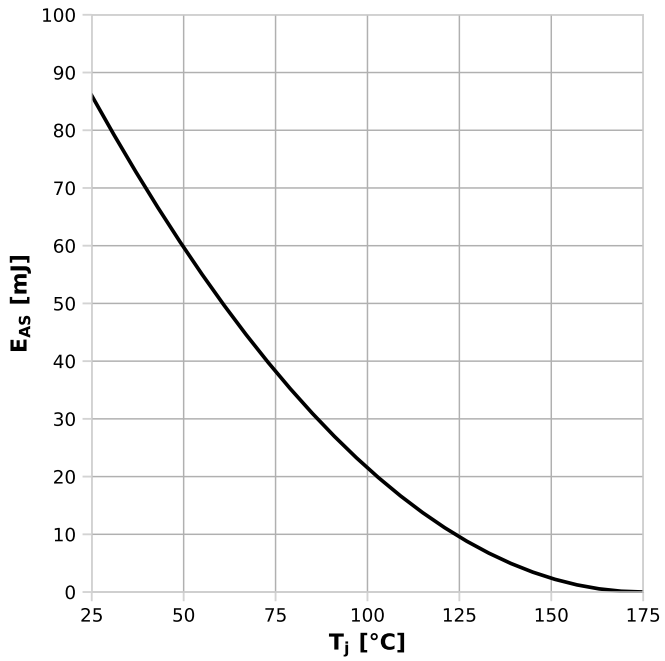
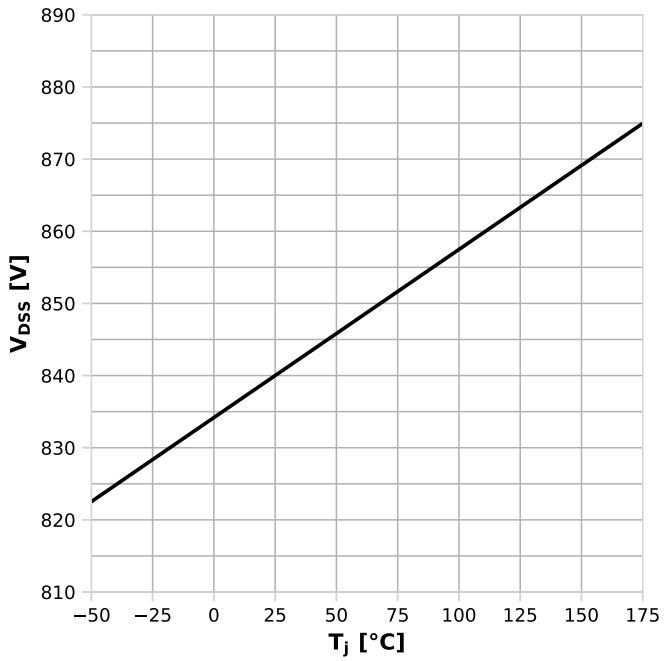
**Diagram 8: Drain-source on-state resistance**




$R_{DS(on)}=f(T_j)$; $I_D=13.8$ A; $V_{GS}=18$ V

| Diagram 9: Typ. transfer characteristics | Diagram 10: Typ. gate charge |
|---|---|
|  |  |
| $I_{DS}=f(V_{GS})$; $V_{DS}=20$ V; parameter: $T_j$ | $V_{GS}=f(Q_G)$; $I_D=13.8$ A pulsed; parameter: $V_{DD}$ |

| Diagram 11: Typ. reverse drain current characteristics | Diagram 12: Typ. reverse drain current characteristics |
|---|---|
|  |  |
| $I_{SD}=f(V_{SD})$; $V_{GS}=0$ V; parameter: $T_j$ | $I_{SD}=f(V_{SD})$; $V_{GS}=18$ V; parameter: $T_j$ |

| Diagram 13: Avalanche energy | Diagram 14: Drain-source breakdown voltage |
|---|---|
|  |  |
| $E_{AS}=f(T_j)$; $I_D$=3.2 A; $V_{DD}$=50 V | $V_{DSS}=f(T_j)$; $I_D$=0.3 mA |

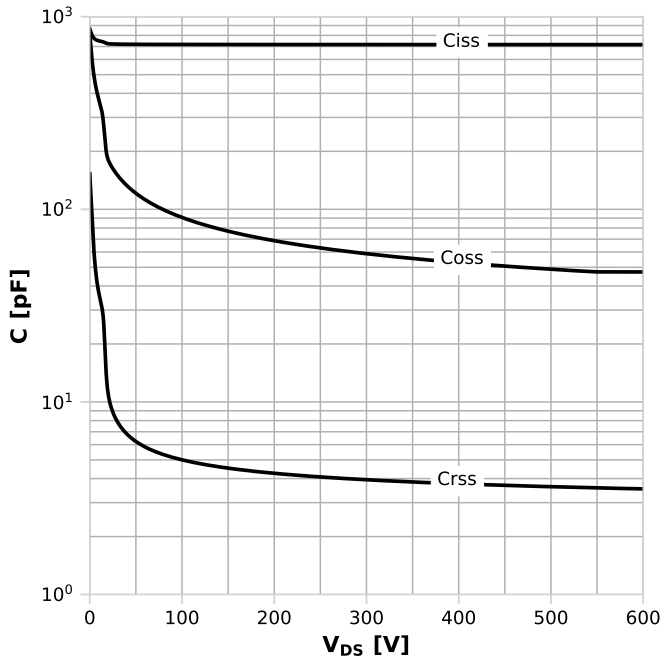
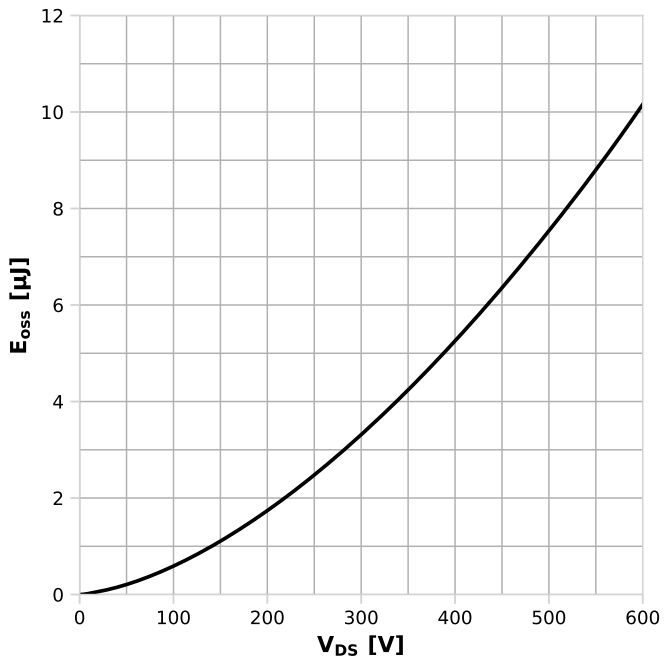
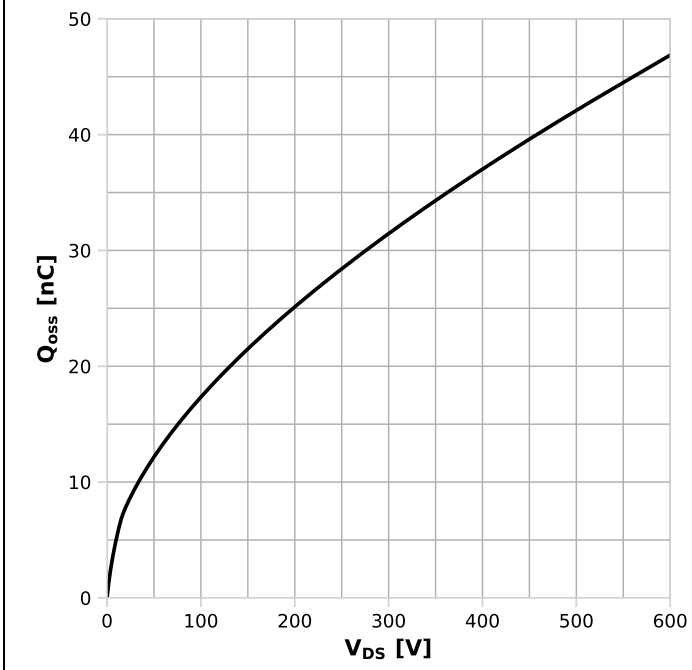
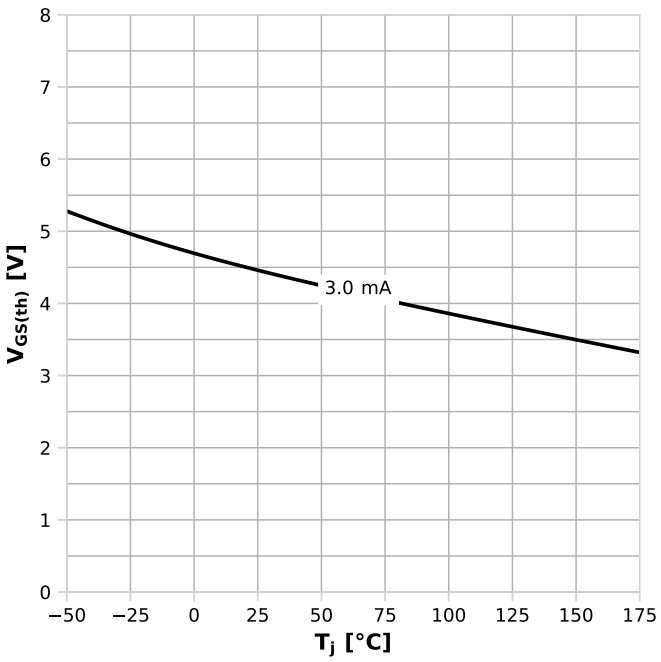
| Diagram 15: Typ. capacitances | Diagram 16: Typ. Coss stored energy |
|---|---|
|  |  |
| C=f($V_{DS}$); $V_{GS}$=0 V; f=250 kHz | $E_{oss}=f(V_{DS})$ |

**Diagram 17: Typ. Qoss output charge**



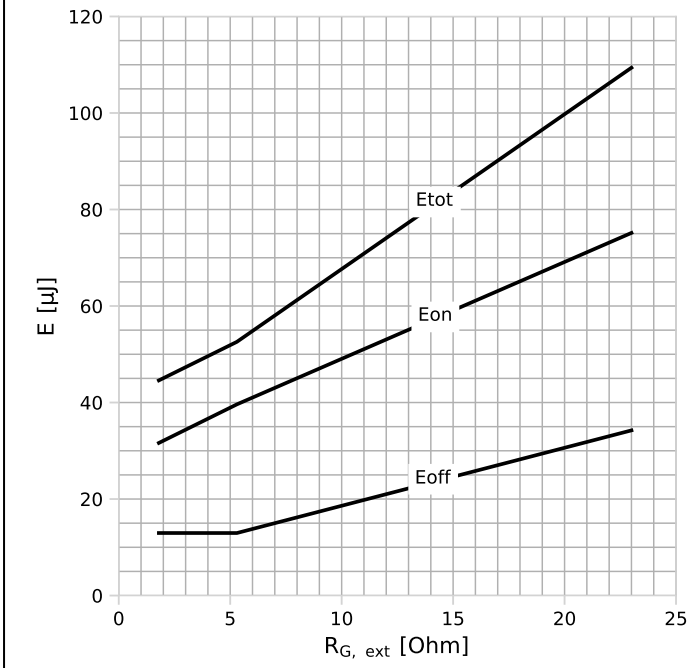

$Q_{oss}=f(V_{DS})$

**Diagram 18: Typ. gate threshold voltage**



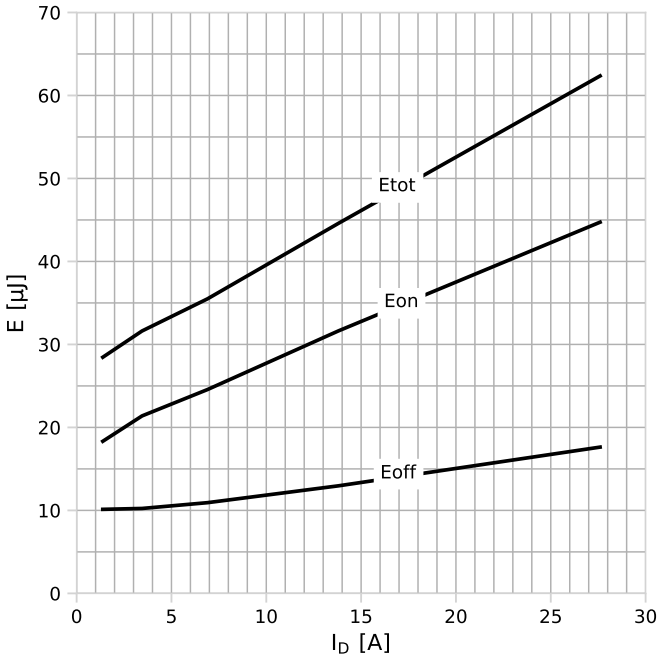

$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: $I_D$

**Diagram 19: Typ. Switching Losses vs $R_{G,ext}$**



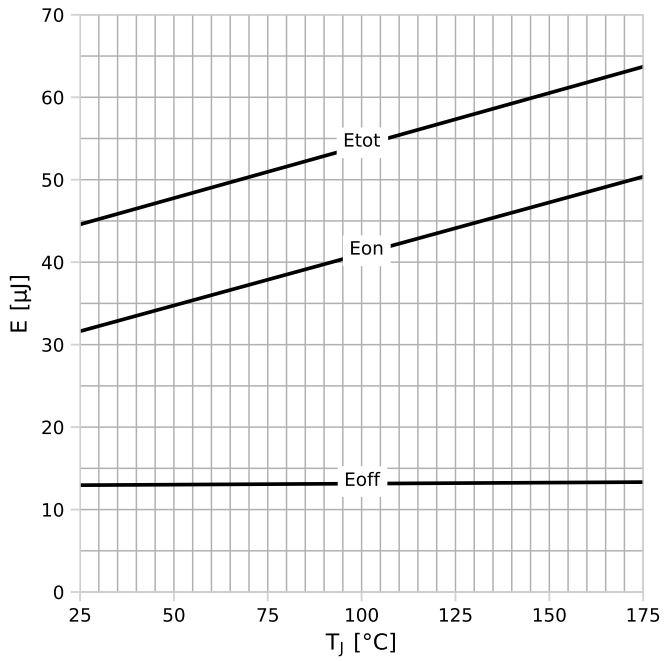

$V_{DD}$=500 V; $I_D$=13.8 A; $T_J$=25 °C

**Diagram 20: Typ. Switching Losses vs switching current**




$V_{DD}$=500 V; $R_{G,ext}$=1.8 Ohm; $T_J$=25 °C

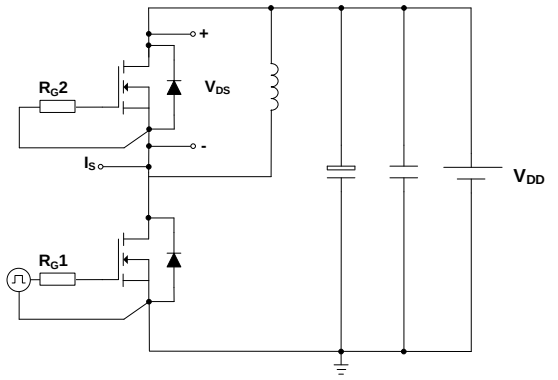
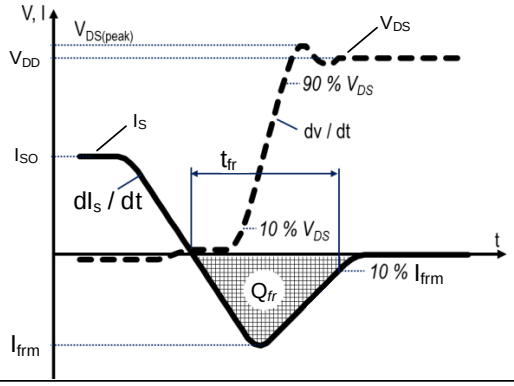
**Diagram 21: Typ. Switching Losses vs $T_J$**




$V_{DD}$=500 V; $R_{G,ext}$=1.8 Ohm; $I_D$=13.8 A

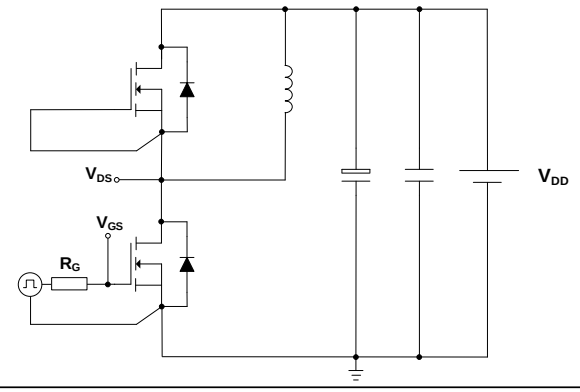
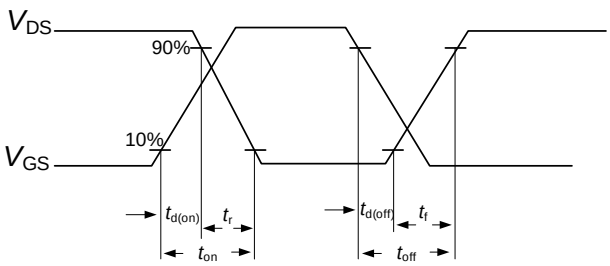
# 6 Test circuits

## Table 9 Body diode characteristics

| Test circuit for body diode characteristics | Body diode recovery waveform |
|---|---|
|  |  |

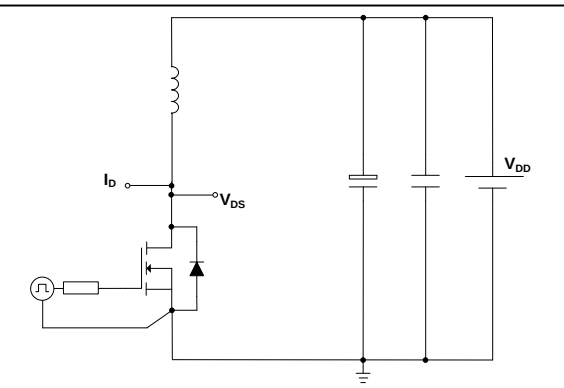
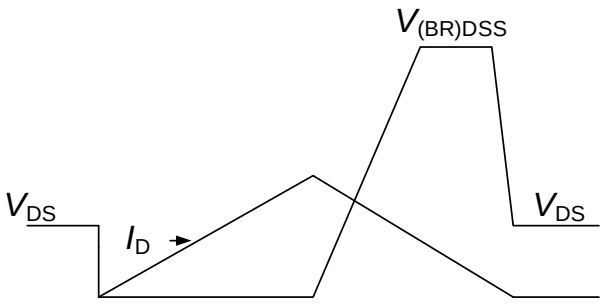


## Table 10 Switching times

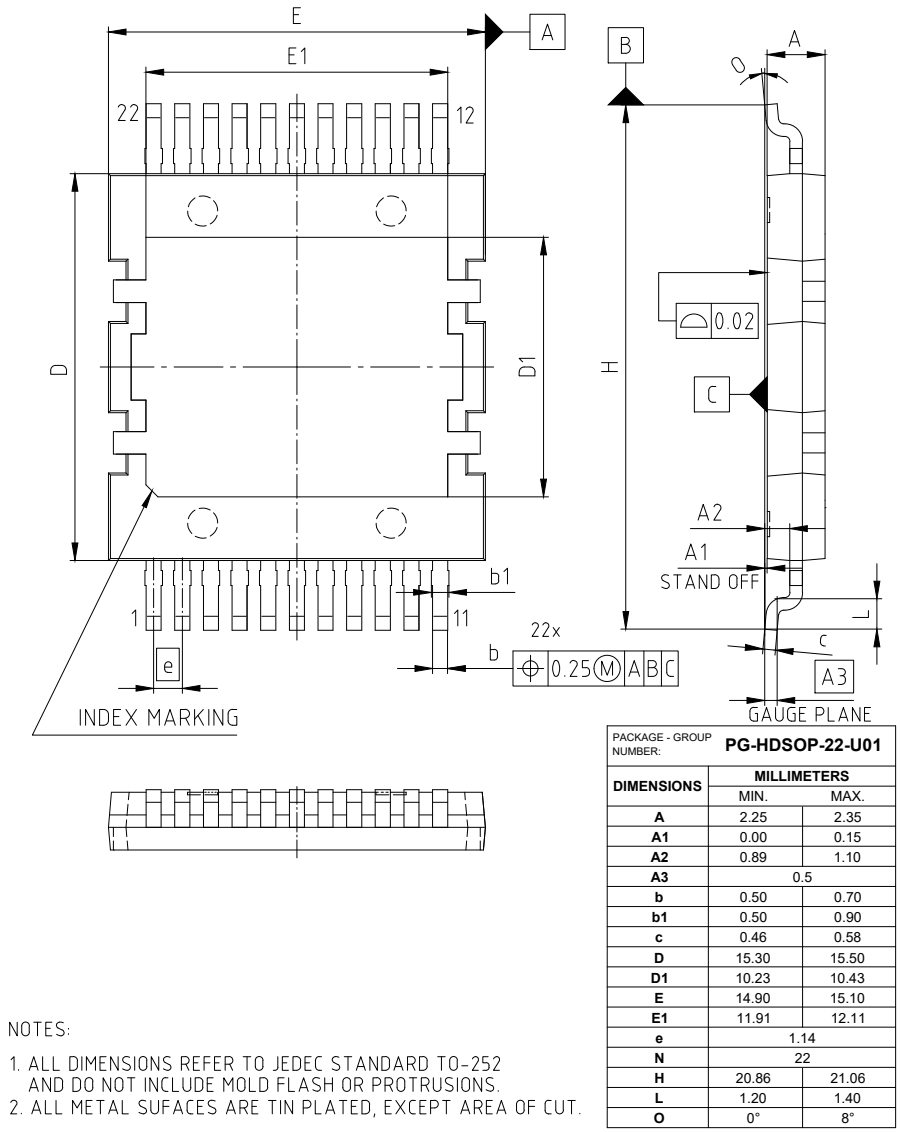
| Switching times test circuit for inductive load | Switching times waveform |
|---|---|
|  |  |



## Table 11 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|---|
|  |  |

# 7 Package outlines




| PACKAGE - GROUP NUMBER: | PG-HDSOP-22-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.25 | 2.35 |
| A1 | 0.00 | 0.15 |
| A2 | 0.89 | 1.10 |
| A3 | 0.5 | |
| b | 0.50 | 0.70 |
| b1 | 0.50 | 0.90 |
| c | 0.46 | 0.58 |
| D | 15.30 | 15.50 |
| D1 | 10.23 | 10.43 |
| E | 14.90 | 15.10 |
| E1 | 11.91 | 12.11 |
| e | 1.14 | |
| N | 22 | |
| H | 20.86 | 21.06 |
| L | 1.20 | 1.40 |
| O | 0° | 8° |

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. ALL METAL SUFACES ARE TIN PLATED, EXCEPT AREA OF CUT.

**Figure 1 Outline PG-HDSOP-22, dimensions in mm**

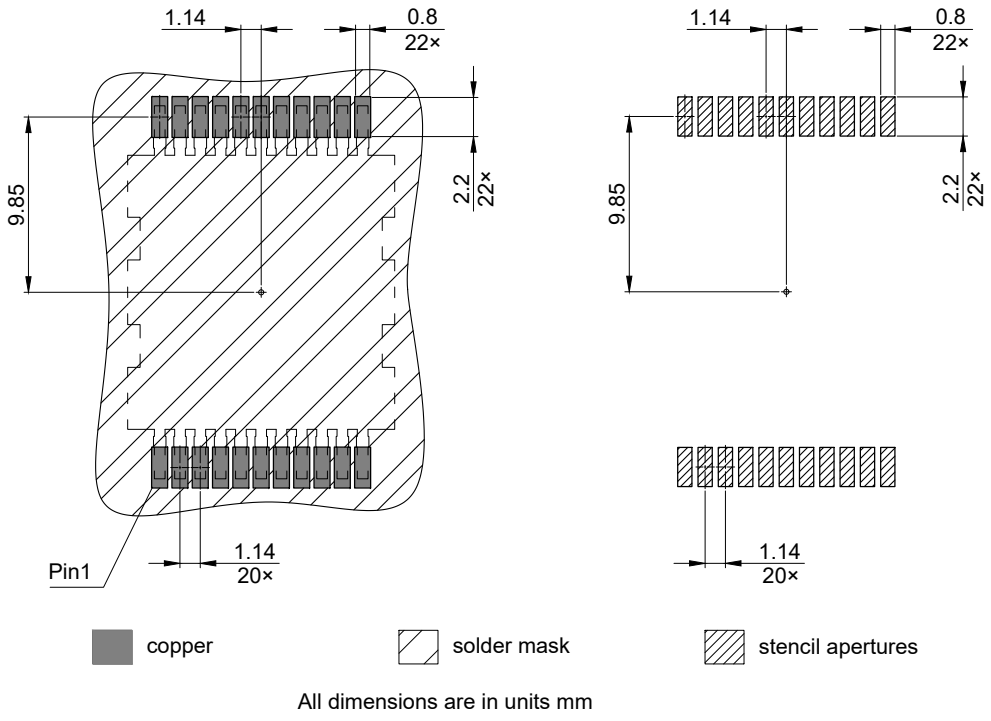



**Figure 2 Footprint drawing PG-HDSOP-22, dimensions in mm**

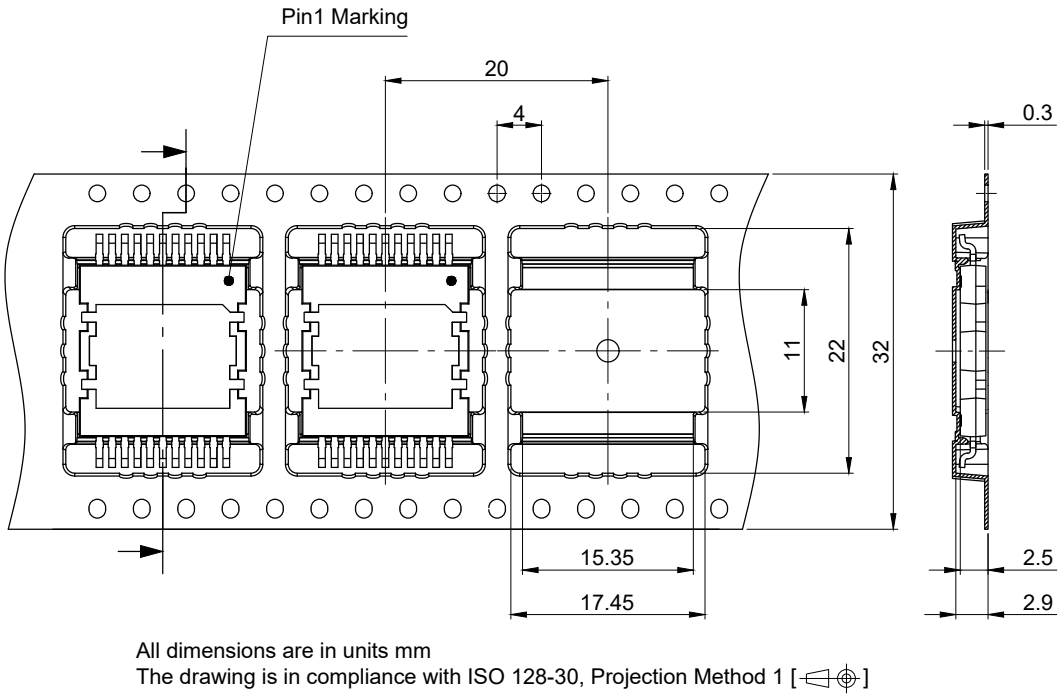



**Figure 3 Packaging variant PG-HDSOP-22, dimensions in mm**

# 8 Appendix A

**Table 12 Related links**

- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Application Note
- IFX CoolSiC CoolSiC™ MOSFET 750 V G2 Simulation Model
- IFX Design tools

## Revision history

IMDQ75R060M2H

### Revision 2025-03-07, Rev. 2.0

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2025-03-07 | Release of final version |

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