IS31CS8977

PRELIMINARY

MCU with 2KB SRAM and 64KB ECC E-Flash

GENERAL DESCRIPTION

CS8977 is a general-purpose MCU with 64KB Code e-Flash memory with ECC, 2K SRAM with ECC. The embedded flash for code storage has built-in ECC that correct 1-bit error and detect two-bit errs. CPU accesses the e-Flash through program address read and through Flash Controller which can performs software read/writer operations of e-Flash.

CPU in CS8977 is 1-T 8051 with enhanced multiplication and division accelerator. There are three clock sources for system, one is a 16MHz/32MHz IOSC (manufacturer calibrated +/- 2%), one is XCLK, and the other one is 32KHz/64KHz SOSCDIV which divided from 128HKz SOSC. ALL clock sources have a clock programmable divider for scaling down the frequency to save power dissipations. The clock selections are combined with flexible power management schemes, including NORMAL, and STOP, and SLEEP modes to balance speed and power consumption.

There are T0/T1/T2/T3/T4/T5 timers coupled with CPU and three WDT where WDT1 is clocked by SYSCLK, and WDT2/WDT3 are clocked by a non-stop SOSCDIV. An 8-bit/16-bit checksum and 16-bit CRC accelerator is included. There are EUART/LIN controller and I2C master/Slave controller as well as SPI master/slave controller. The interfaces of these controllers are multiplexed with GPIO pins. Other useful peripherals include a buzzer control, six 8/10/12-bit PWM, and one channel of 16-bit timer/capture and quadrature decoder. There is also 16 channels 8-bit PWM for LED control.

Analog peripherals include a 12-bit ADC with internal temperature sensor, an 8-bit voltage output DAC, and four analog comparators with programmable threshold. A touch key controller up to 20-bit resolutions is also included. The touch key controller also has shield output capability for moisture immunity. The touch key controller allows sleep mode (under 20uA) and use auto detection for wakeup. The maximum number of key input can be scanned is 27.

CS8977 also provides a flexible means of flash programming that supports ISP and IAP. The protection of data loss is implemented in hardware by access restriction of critical storage segments. The code security is reinforced with sophisticated writer commands and ISP commands. The on-chip break point processor also allows easy debugging which can be integrated with ISP. Reliable power-on-reset circuit and low supply voltage detection allows reliable operations under harsh environments.

Applications

- Touch key applications with high robustness and reliability requirements
- Automotive and appliance

FEATURES

CPU and Memory

- 1-Cycle 8051 CPU core up to 32MHz
- 16-bit Timers T0/T1/T2/T3/T4 and 24-bit T5
- Checksum and CRC accelerator
- WDT1 by SYSCLK, WDT2/WDT3 by SOSCDIV
- Clock fault monitoring
- Up to 6 external interrupts shared with GPIO pins
- Power saving modes – Normal, STOP, and SLEEP modes
- 256B IRAM and 1792B XRAM with ECC check
- 64KB Code e-Flash with ECC and two 128x16 Information Block
  - Code security and data loss protection
  - 100K endurance and 10 years retention

Clock Sources

- Internal oscillator at +/- 2% 16MHz/32MHz
  - Spread Spectrum option
- Internal low power oscillator 128KHz/256KHz
- External clock option and clock out

Digital Peripherals

- 6 CH 8/10/12-bit center-aligned PWM controller
  - Tigger interrupt and ADC conversion
- 16 CH 8-bit PWM left/right aligned
- One 16-bit Timer/Capture and One 16-bit quadrature decoder
- Buzzer/Melody generator
- One I^2C Master
- One I^2C Slave – also for ISP and debug
- One SPI Master/Slave Controllers
- One EUART1 and one EUART2/LIN

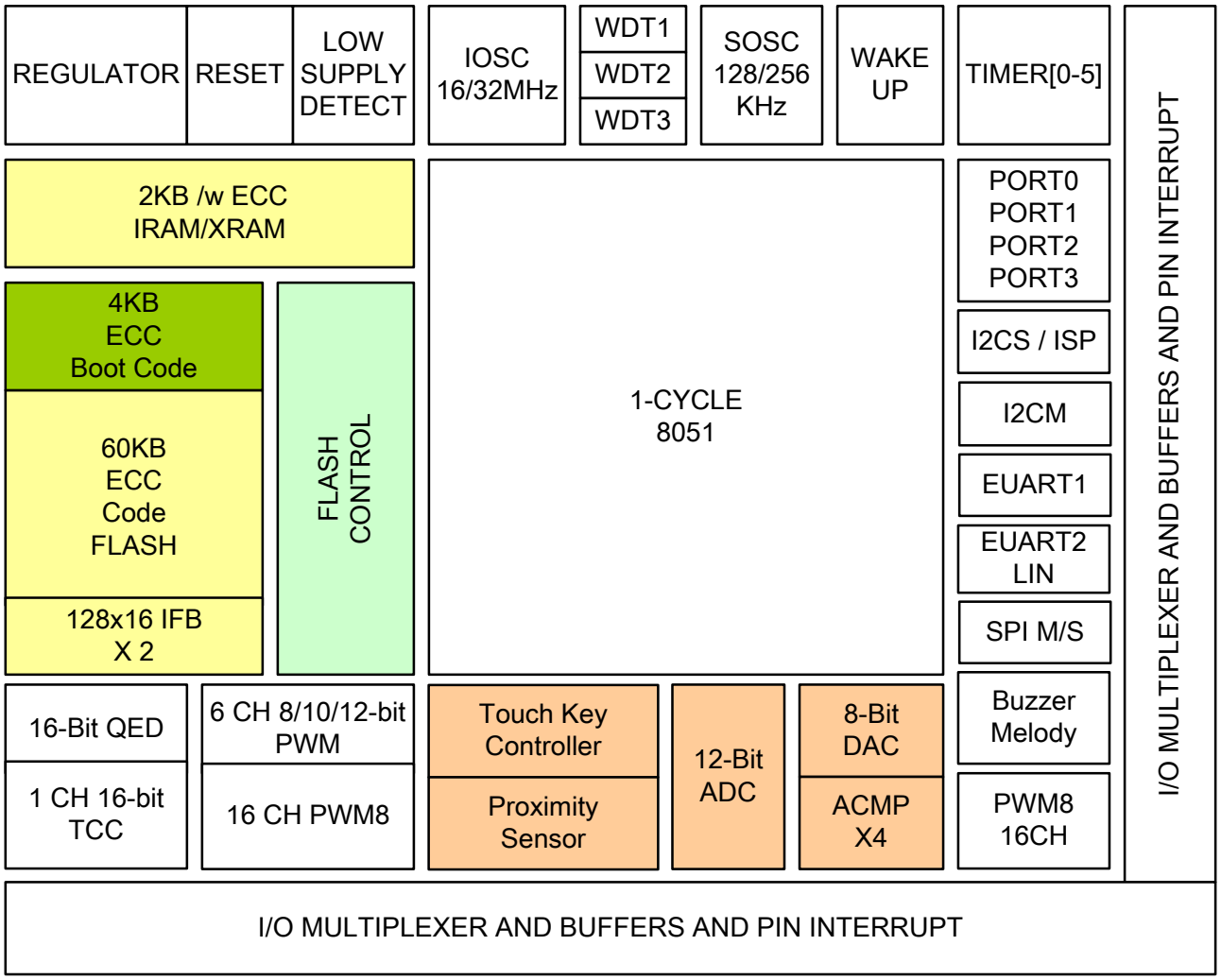
Analog Peripherals

- Capacitance sense touch-key controller scan up to 27 key inputs
  - Shield output for moisture immunity
  - Low power sleep mode wakeup (<20uA).
- 12-Bit SAR ADC with GPIO analog input
  - Track and hold
  - Temperature sensor and supply measurement
- 8-Bit DAC and four analog comparators
- Power on reset and Low voltage detect (2.2V-4.5V)

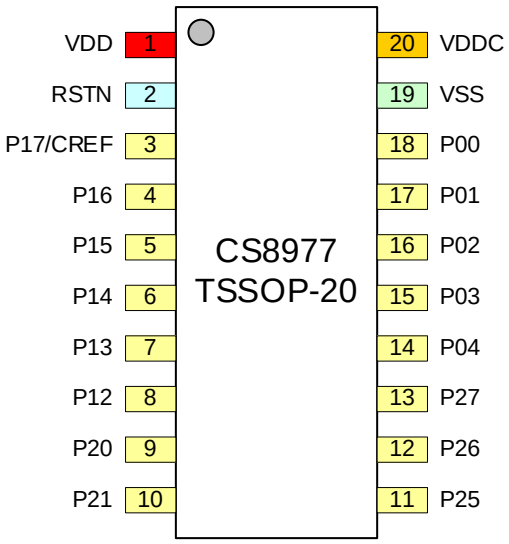
Miscellaneous

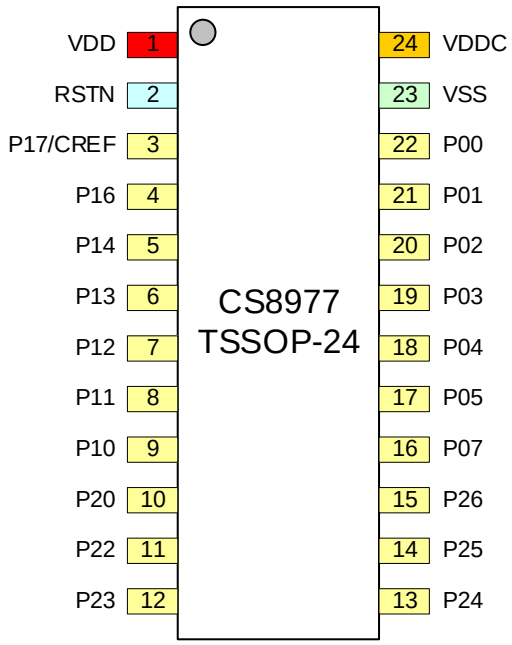
- Up to 28 GPIO pins with multi-function options
  - Configurable IO structure and noise filters
- 2.3V to 5.5V single supply
- Active current < 150uA/MHz in Normal mode
- Low power standby (1uA) in SLEEP mode
- Operating temperature -40°C t0 85°C
- TSSOP20/24/28 and LQFP32 package (RoHS compliant)

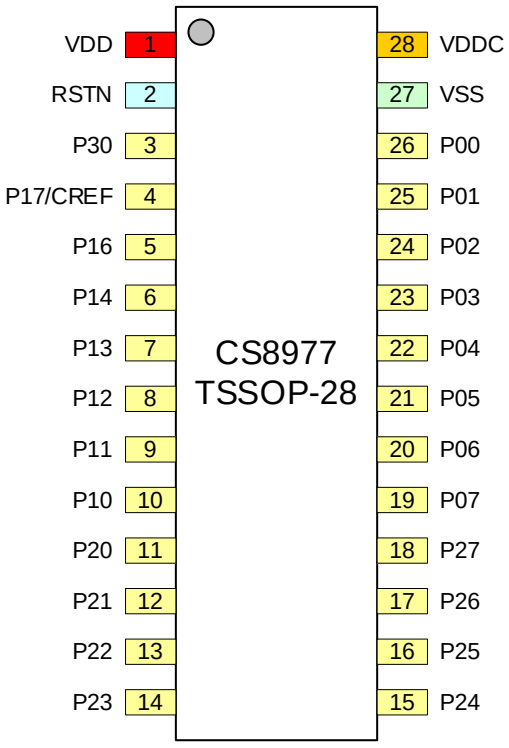
BLOCK DIAGRAM

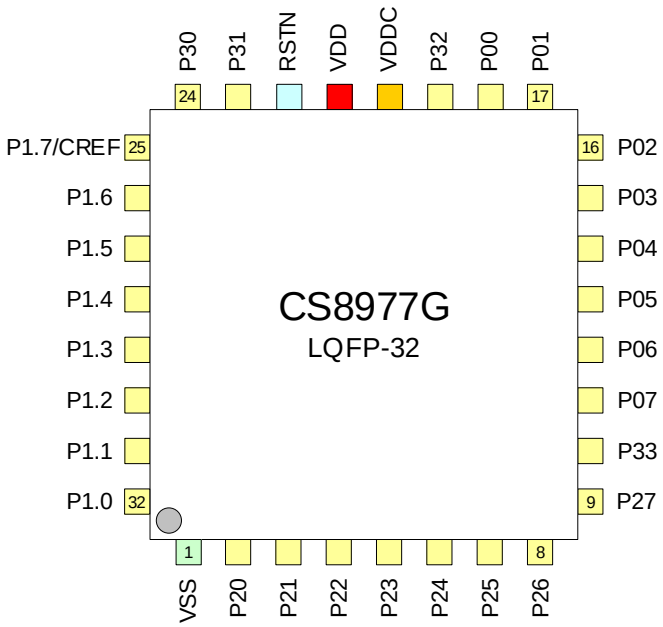


PIN OUT


VDD 1
RSTN 2
P17/CREF 3
P16 4
P15 5
P14 6
P13 7
P12 8
P20 9
P21 10
20 VDDC
19 VSS
18 P00
17 P01
16 P02
15 P03
14 P04
13 P27
12 P26
11 P25
CS8977
TSSOP-20


VDD 1
RSTN 2
P17/CREF 3
P16 4
P14 5
P13 6
P12 7
P11 8
P10 9
P20 10
P22 11
P23 12
24 VDDC
23 VSS
22 P00
21 P01
20 P02
19 P03
18 P04
17 P05
16 P07
15 P26
14 P25
13 P24
CS8977
TSSOP-24


VDD 1
RSTN 2
P30 3
P17/CREF 4
P16 5
P14 6
P13 7
P12 8
P11 9
P10 10
P20 11
P21 12
P22 13
P23 14
28 VDDC
27 VSS
26 P00
25 P01
24 P02
23 P03
22 P04
21 P05
20 P06
19 P07
18 P27
17 P26
16 P25
15 P24
CS8977
TSSOP-28


P30 24
P31
RSTN
VDD
VDDC
P32
P00
P01 17
P1.7/CREF 25
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0 32
16 P02
P03
P04
P05
P06
P07
P33
9 P27
1 VSS
P20
P21
P22
P23
P24
P25
8 P26
CS8977G
LQFP-32

PIN Description and Multifunction Table

NAME	TYPE	ANIO1	ANIO2	PIN DESCRIPTION
VDDH	P	-	-	Supply Voltage 2.3V to 5.5V
VDDC	P/O	-	-	Internal 1.5V supply. Connect to external 1.0uF decoupling capacitor.
RSTN	IO	-	-	Active low reset input with internal 5K Ohm pull-up.
VSS	G			VSS
P00	IO/A	KEY	ADCA	Port 0.0 I/O with multi-function.
P01	IO/A	KEY	ADCB	Port 0.1 I/O with multi-function.
P02	IO/A	KEY	DAC	Port 0.2 I/O with multi-function.
P03	IO/A	KEY	CMPA	Port 0.3 I/O with multi-function.
P04	IO/A	KEY	CMPB	Port 0.4 I/O with multi-function.
P05	IO/A	KEY	CMPC	Port 0.5 I/O with multi-function.
P06	IO/A	KEY	CMPD	Port 0.6 I/O with multi-function.
P07	IO/A	KEY	CMPTH	Port 0.7 I/O with multi-function.
P10	IO/A	KEY	ADCA	Port 1.0 I/O with multi-function.
P11	IO/A	KEY	ADCB	Port 1.1 I/O with multi-function.
P12	IO/A	KEY	SHIELD	Port 1.2 I/O with multi-function.
P13	IO/A	KEY	CMPTH	Port 1.3 I/O with multi-function.
P14	IO/A	KEY	CMPD	Port 1.4 I/O with multi-function.
P15	IO/A	KEY	CMPC	Port 1.5 I/O with multi-function.
P16	IO/A	KEY	CMPB	Port 1.6 I/O with multi-function.
P17	IO/A	KEYR	CMPA	Port 1.7 I/O with multi-function. Also serves as CREF for touch key controller
P20	IO/A	KEY	SHIELD	Port 2.0 I/O with multi-function.
P21	IO/A	KEY	ADCA	Port 2.1 I/O with multi-function.
P22	IO/A	KEY	ADCB	Port 2.2 I/O with multi-function.
P23	IO/A	KEY	CMPA	Port 2.3 I/O with multi-function.
P24	IO/A	KEY	CMPB	Port 2.4 I/O with multi-function.
P25	IO/A	KEY	CMPC	Port 2.5 I/O with multi-function.
P26	IO/A	KEY	CMPD	Port 2.6 I/O with multi-function.
P27	IO/A	KEY	CMPTH	Port 2.7 I/O with multi-function.
P30	IO/A	KEY	ADCA	Port 3.0 I/O with multi-function.
P31	IO/A	KEY	ADCB	Port 3.1 I/O with multi-function.
P32	IO/A	KEY	DAC	Port 3.2 I/O with multi-function.
P33	IO/A	KEY	SHIELD	Port 3.3 I/O with multi-function.

Each GPIO pin can use MFCFG register to select pin functions. The function table is shown as following table.

MFCFG[6-0]	Function NAME	FUNCTION DESCRIPTION
00000	LOW	This force the output to logic low state. Actual output depends on OPOL setting in IOCFG register.
000001	GPIO	8051 GPIO port
000010	SCK	SPI SCK input or output depending SPI MS setting.
000011	SDI	SPI SDI input corresponding to MI or SI depending SPI MS setting.
000100	SDO	SPI SDO output corresponding to MO or SO depending SPI MS setting.
000101	SSN	SPI SSN input or output depending SPI MS setting.
000110	SSCL	I2C Slave SCL I/O
000111	SSDA	I2C Slave SDA I/O
001000	MSCL	I2C Master SCL I/O
001001	MSDA	I2C Master SDA I/O
001010	TX1	EUART1 TX output