DK-START-GW2A55-PG484 Development Board

User Guide

DBUG362-1.0E,10/17/2019

Disclaimer

Revision History

Date	Version	Description
10/17/2019	1.0E	Initial version published.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

The DK-START-GW2A55-PG484 development board (hereinafter referred to development board) user manual consists of the following four parts:

1. A brief introduction to the features of the development board;
2. An introduction to the development board architecture and hardware resources;
3. An introduction to the hardware circuit functions, circuits, and pins distribution;

1.2 Supported Products

The information presented in this guide applies to GW2A-LV55PG484 device.

1.3 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS102, GW2A series FPGA Products Data Sheet
2. UG113, GW2A-55 Pinout Manual
3. UG111, GW2A series of FPGA Products Package and Pinout Manual

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
B-SRAM	Block Static Random Access Memory
DDR	Double-Data-Rate Synchronous Dynamic Random Access Memory
DSP	Digital Signal Processing
FLASH	Flash Memory
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
LDO	Low Dropout Regulator
LUT4	Four-input Look-up Tables
LVDS	Low-Voltage Differential Signaling
S-SRAM	Shadow SRAM

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

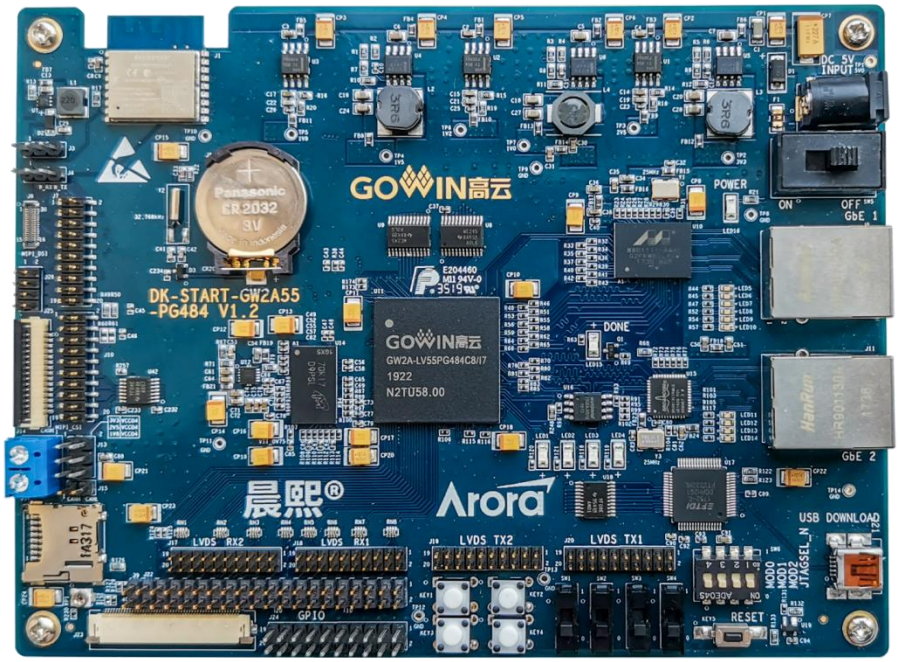
E-mail:support@gowinsemi.com

+Tel: 86 -20 -8757 -8868

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK-START-GW2A55-PG484



DK-START-GW2A55-PG484 applies to high speed data storage based on DDR3, high-speed communication test based on MIPI, LVDS and GbE, 55k series FPGA functions evaluation, the verification of hardware reliability, software learning and debugging, etc.

The development board uses the GW2A- LV55PG484 FPGA device, which is the first generation product of Gowin Arora family. The GW2A series of FPGA products offer a range of comprehensive features and rich internal resources like high-performance DSP resources, a high-speed LVDS interface, and abundant BSRAM memory resources. These

embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.

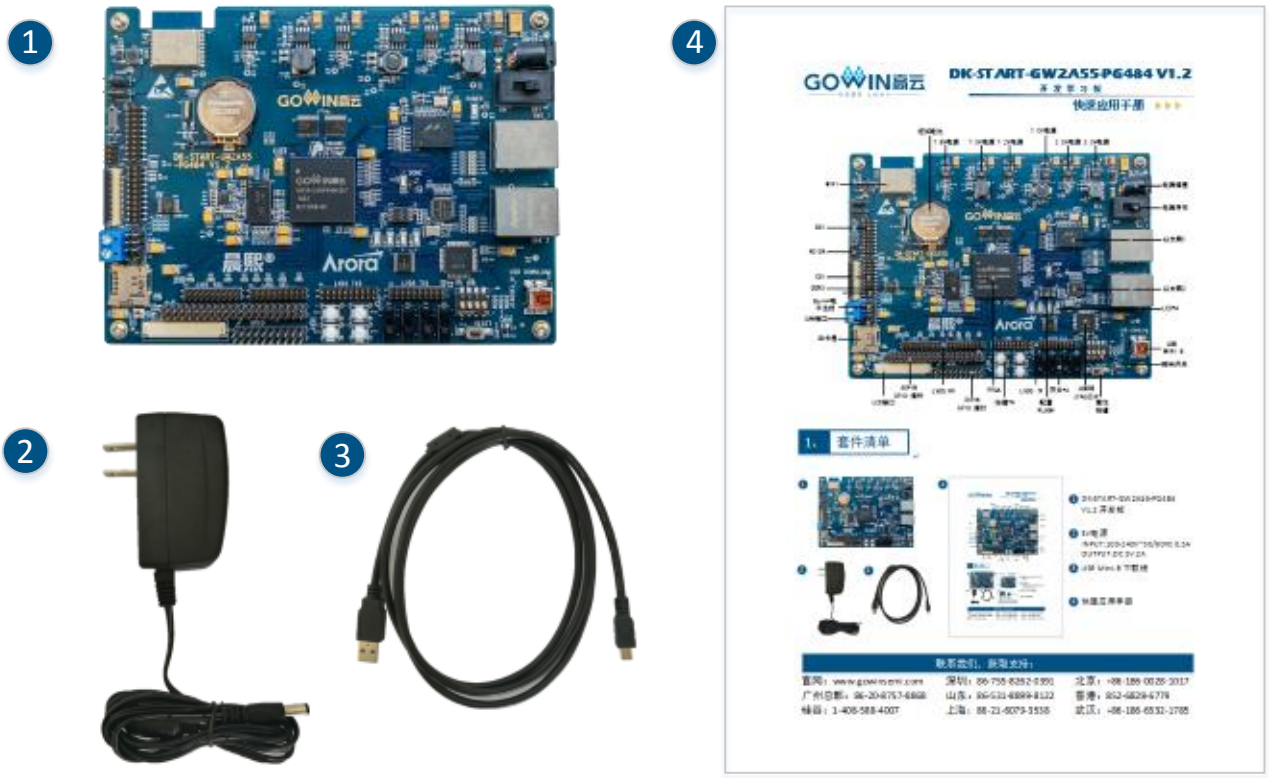
GW2A- LV55PG484 includes a DDR3 chip with 2Gbit storage space, 16 bits data bus width. Its two Gigabit Ethernet interfaces support 10M, 100M, 1000M Ethernet communication. It has abundant peripheral interfaces, including LVDS interfaces, a SD card slot, CAN bus interface, MIPI CSI, MIPI DSI, AD/DA interface and GPIO interfaces. RTC module is designed to provide real-time clock for MCU IP. Besides that, it also offers an external Flash, slide switches, key switches, LED, etc.

2.2 A Development Board Suite

A development board suite includes the following items:

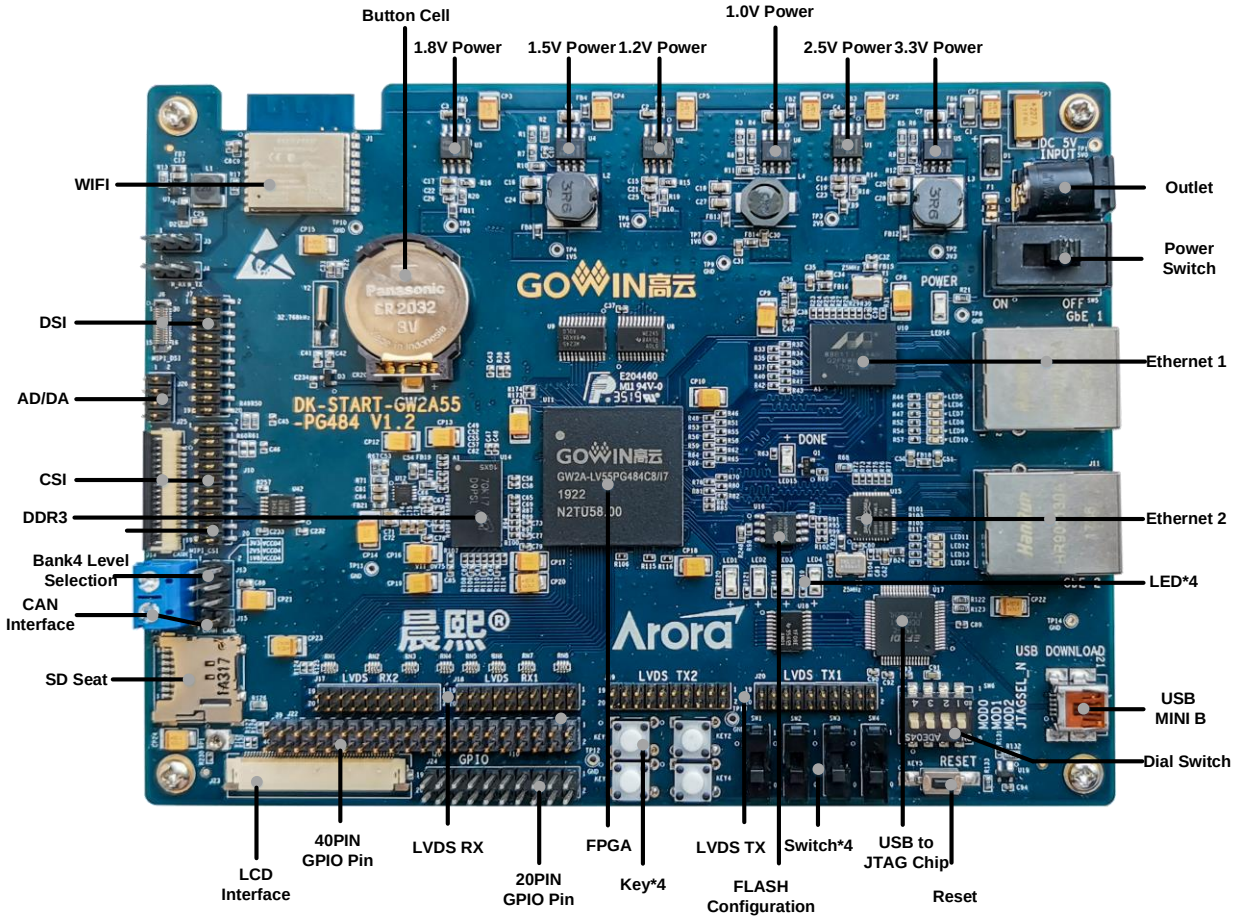
- DK-START-GW2A55-PG484
- 5V power (Input: 100-240V~50/60Hz 0.5A, output: DC 5V 2A)
- USB cable
- Quick Start Guide

Figure 2-2 A Development Board Suite



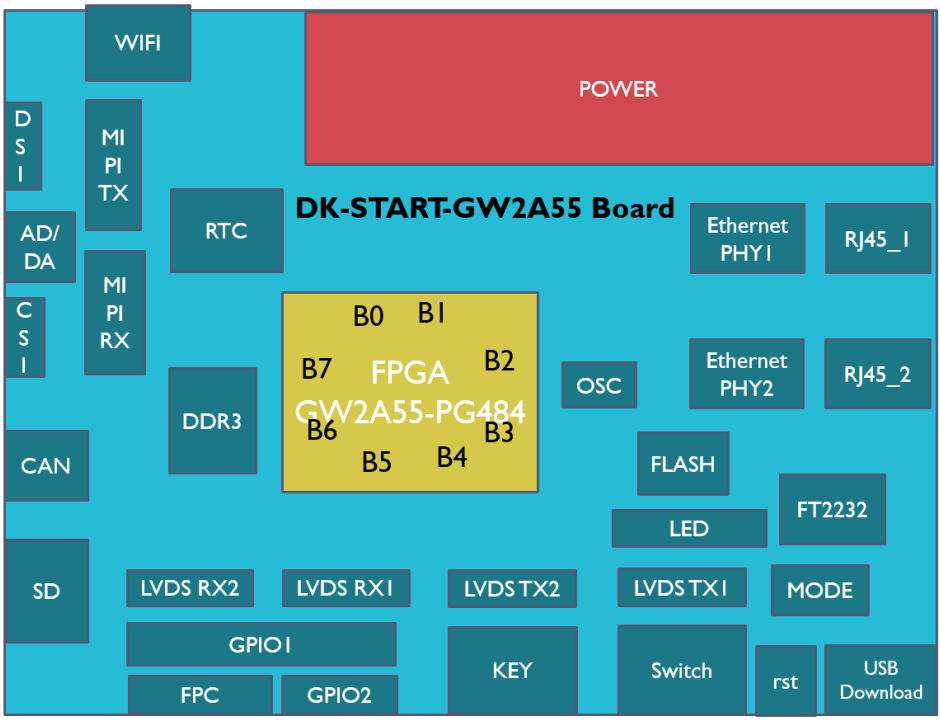
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Diagram

Figure 2--4 System Architecture



2.5 Features

The key features of DK-START-GW2A55-PG484 are as follows:

1. The FPGA device
   - Gowin GW2A-LV55PG484 FPGA
   - Up to 319 user I/O
2. Download and Boot
   - Integrates the download module; can be downloaded with the USB Mini B cable
   - External Flash boot
   - The blue DONE light is on after loading
3. Power
   - External 5V 2A Power supply
   - The blue POWER light is on after power on
   - The development board generates 3.3v, 2.5v, 1.8v, 1.5v, 1.2v, 1.0v, 0.75v and the power supply needed by LCD interface and MIPI interface
4. Clock system

50MHz crystal oscillator input

5. Memory Device
   - 2Gbit DDR3 SDRAM
   - 64Mbit FLASH
6. Ethernet interface
   - Two Ethernet interfaces
   - One adopts B50610KML chip from Broadcom and supports RGMII (10/100/1000) interface.
   - The other adopts 88E1111 chip from Marvell and supports MII, GMII, RGMII (10/100/1000) interface.
   - RJ45 connector with built-in transformer
7. LVDS interfaces
   - Two LVDS interfaces for receiving, including ten pairs of differential signals.
   - Two LVDS interface for sending, including ten pairs of differential signals.
   - I/O voltage is adjustable when used as GPIO, supporting 3.3v, 2.5v and 1.8v.

   Note!

   J13 needs to be set to 2.5V when LVDS is used.
8. MIPI DSI Interface
   - The interface includes 5 pairs of differential signals, among which one clock and four data include.
   - The stacked board connector with 30 contacts, 04mm pitch is used.
   - Five lane DSI signals are simultaneously channelled to 20pin double row of pins with 2.00mm pitch.
9. MIPI CSI Interface
   - Interface includes 3 pairs of differential signal, amonng which one clock and four data include.
   - 15pin FPC connector with 1mm pitch is used.
   - Three lane differential signals are simultaneously channelled to 20pin a double row pins with 2.00mm pitch.
10. SD card slot
    - Eight contacts, push-push type
    - Card detection
11. RTC
    - NXP PCF8563 externally connected to 32.768kHz quartz crystal is used.

- Dual power supply design can be used to develop board power supply or button battery
- The communication interface with FPGA is I2C

12. AD/DA
    - ADI AD5593R chip is adopted
    - It support 12-bit A/D and D/A converters, and 8-channel interfaces can be configured to any combination of ADC/DAC/GPIO
    - The input and output interface adopts 8pin
13. CAN
    - NXP TJA1050 transceiver chip is used
    - The communication with FPGA is through UART interface
    - The maximum transmission rate is 1Mbps
14. WIFI
    - The ESP-WROOM-02 WIFI module of Lexin is adopted
    - The communication with FPGA is through SPI interface
    - SPI communication speed is 20Mbps
15. GPIO Interface
    - There are 40PIN double row pins, including 34 GPIO. I/O Bank voltage is adjusted to 3.3V and there are also 3.3V voltage and 5V voltage and two ground pins.
    - There are 20PIN double row pins, including 16 GPIO. All I/O and 40PIN multiplexes GPIO of FPGA. There are two 3.3V voltages, one 5V voltage and three ground pins.
16. Debugging module
    - Four keys
    - Four switches
    - Four blue LEDs

3 Development Board Circuit

3.1 FPGA Module

3.1.1 Introduction

The resources of GW2A-LV55PG484 FPGA are set out in Table 3-1.

Table 3-1 GW2A-LV55PG484 FPGA Resources List

Device	GW2A-LV55PG484
LUT4	54,720
Flip-Flop (FF)	41,040
Shadow Static Random Access Memory S-SRAM (bits)	109,440
Block Static Random Access Memory B-SRAM (bits)	2,520K
The number of B-SRAM	140
18 x 18 Multiplier	40
PLLs+DLLs	6+4
Total number of I/O banks	8
Max. User I/O	319
Core voltage	1.0V

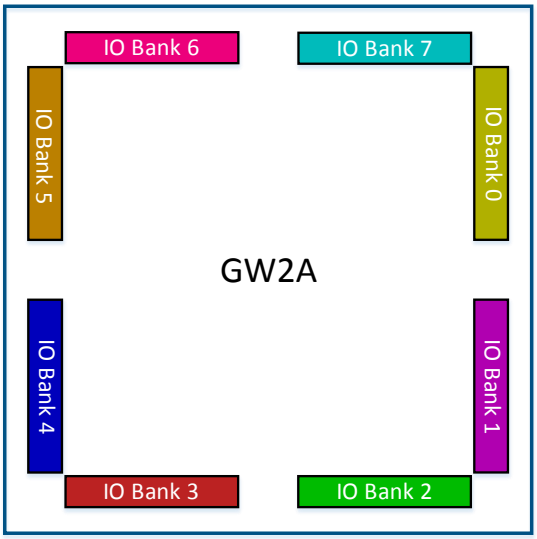
Note!

See *GW2A series of FPGA Products Data Sheet* for further details.

3.1.2 I/O Distribution

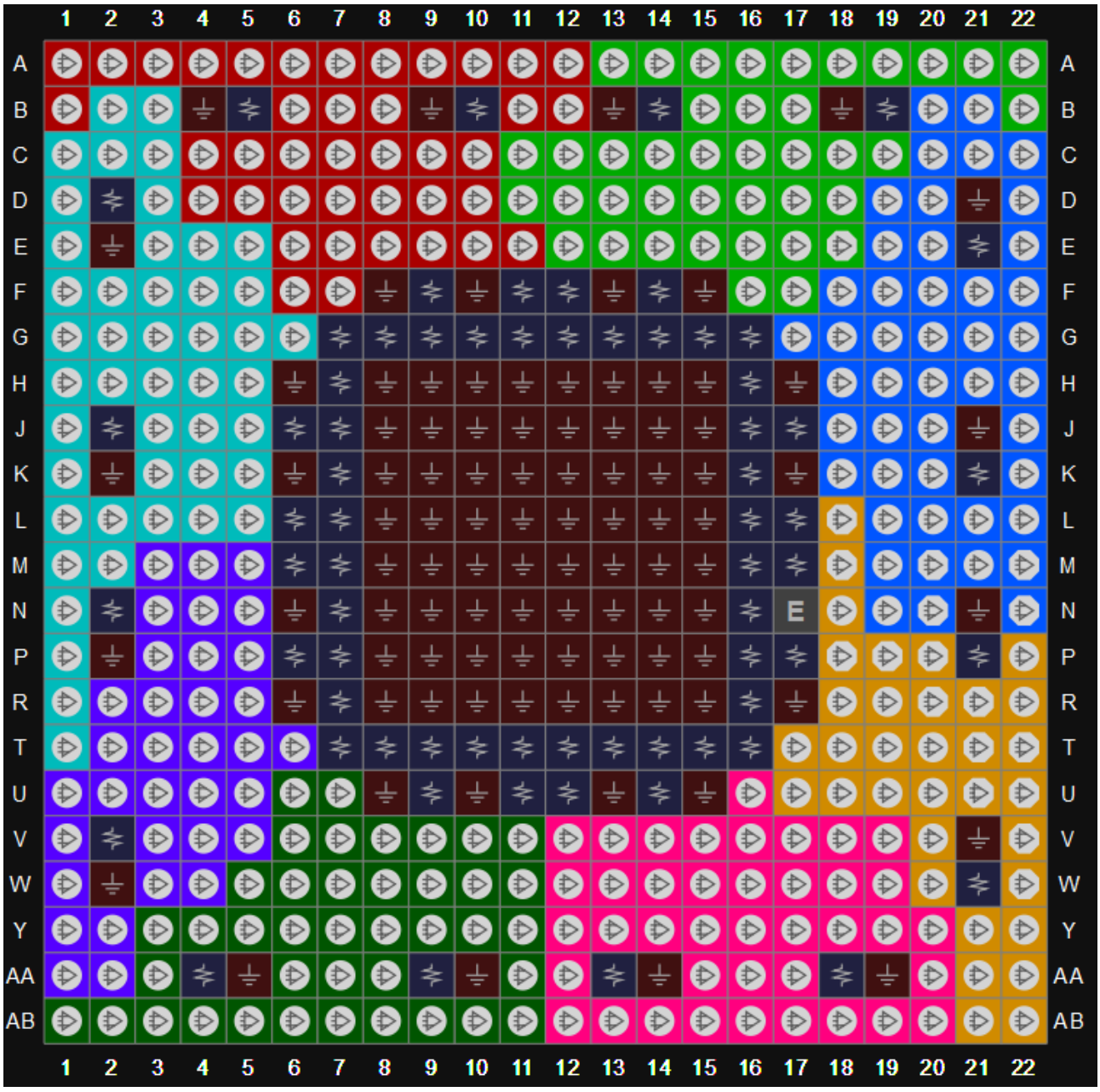
GW2A series FPGA products includes eight I/O Bank. The I/O Bank Distribution is as shown in Figure 3-1.

Figure 3-1 GW2A I/O Bank Distribution



The view of GW2A-55 PG484 pins distribution is as shown in Figure 3-2.

Figure 3-2 View of GW2A-55 PG484 Pins Distribution (Top View)



The I/O Bank voltage and functions are as listed in Table 3-2.

Table 3-2 FPGA I/O Bank Voltage and Functions

I/O BANK No.	Supply voltage	Functions
BANK0	1.2V	MIPI DSI LP MIPI CSI LP WIFI POWER_EN USB to FIFO
BANK1	2.5V	MIPI DSI HS MIPI CSI HS USB to FIFO RTC AD/DA CAN RST
BANK2	3.3V	Ethernet (M88E1111) Ethernet (B50610KML) Clk JTAG
BANK3	1.5V	FAST_N FLASH Configuration READY/DONE/RECONFIG LED light DDR3 SD card detection foot Four keys Four switches
BANK4	3.3V, 2.5V, 1.8V (Adjustable)	LVDS output interface LVDS input interface
BANK5	3.3V	GPIO SD card FPC
BANK6	1.5V	DDR3
BANK7	1.5V	DDR3

3.2 Download Module

3.2.1 Introduction

The development board provides USB download interface, which is realized by the A channel of FT2232 USB conversion chip. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the data stream file will be lost if the device is power down. When downloaded to Flash, the data stream file will

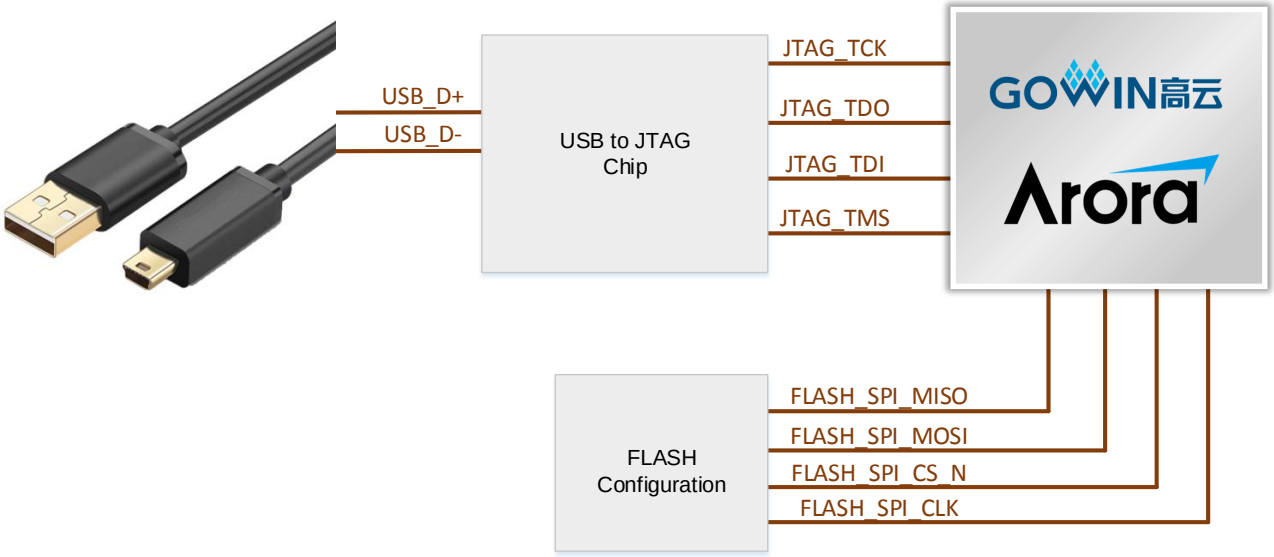
not be lost.

The MODE value configuration:

1. In any modes, you can download the data stream file to the on-chip SRAM and run it immediately.
2. Set MODE as "011" to download the data stream file to the external Flash. Set MODE to "000" and power on again. The device will read the FPGA configuration data from the Flash automatically.

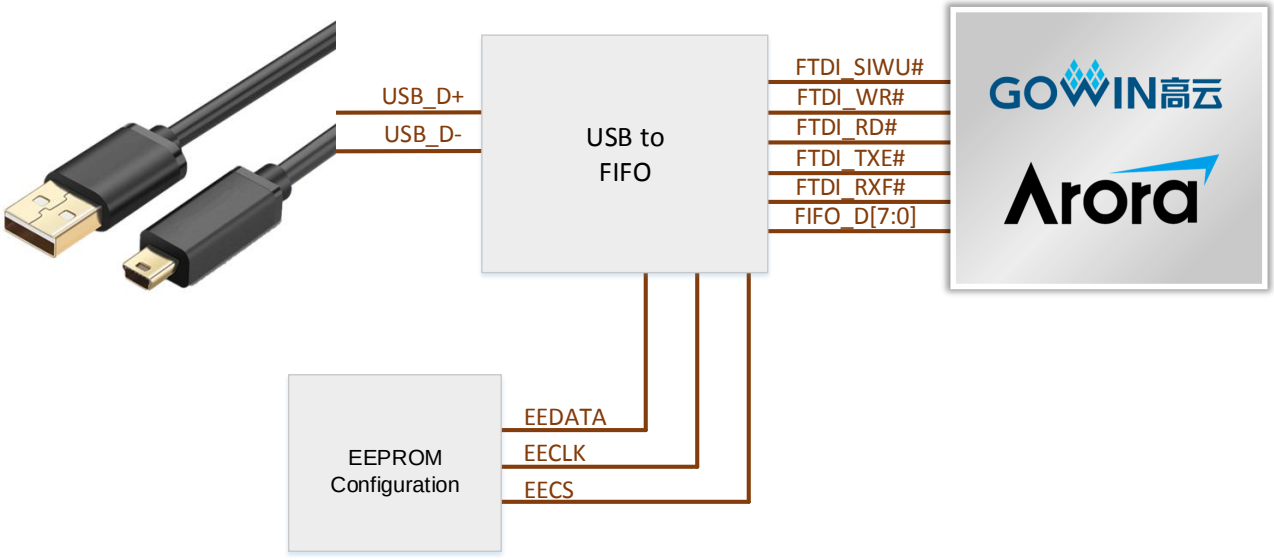
The connection diagram of downloading and configuration is as show in Figure 3-3:

Figure 3-3 Connection Diagram of FPGA Downloading and Configuration



By configuring EEPROM chip, the B channel of FT2232 can be configured as an asynchronous FIFO interface. The connection diagram is shown in Figure 3-4.

Figure 3-4 Asynchronous FIFO Connection Diagram



3.2.2 Pins Distribution

Table 3-3 FPGA Download and Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
JTAG_TCK	N20	2	3.3V	JTAG Signal
JTAG_TDO	M22	2	3.3V	JTAG Signal
JTAG_TDI	M20	2	3.3V	JTAG Signal
JTAG_TMS	N22	2	3.3V	JTAG Signal
FLASH_SPI_MISO	P19	3	1.5V	FLASH Signal Configuration
FLASH_SPI_MOSI	P20	3	1.5V	FLASH Signal Configuration
FLASH_SPI_CS_N	N18	3	1.5V	FLASH Signal Configuration
FLASH_SPI_CLK	P18	3	1.5V	FLASH Signal Configuration

Table 3-4 Asynchronous FIFO Pins Distribtion

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
FTDI_SIWU#	B12	0	1.2V	Send/wake up signal
FTDI_WR#	A11	0	1.2V	Write signal
FTDI_RD#	B11	0	1.2V	Read signal
FTDI_TXE#	C9	0	1.2V	Write Enable Signal
FTDI_RXF#	C10	0	1.2V	Read Enable Signal
FIFO_D0	A20	1	2.5V	Data bits 0
FIFO_D1	A21	1	2.5V	Data bits 1
FIFO_D2	C17	1	2.5V	Data bits 2
FIFO_D3	D18	1	2.5V	Data bits 3
FIFO_D4	D17	1	2.5V	Data bits 4
FIFO_D5	E17	1	2.5V	Data bits 5
FIFO_D6	F17	1	2.5V	Data bits 6
FIFO_D7	F16	1	2.5V	Data bits 7

3.3 Power Supply

3.3.1 Introduction

The development board is powered by a power adapter. The input parameter is 100-240V~50/60MHz 0.5A, and output is DC +5V 2A.

The input 5V power can generate 3.3v, 2.5v, 1.8v, 1.5v, 1.2v, 1.0v and 0.75v power required by DDR3, 17.4v, +5V and -5v required by MIPI DSI interface and 16V, 10.4v, 9.9v, -7v required by RGB screen interface through the power chip on the development board.

Three NCP3170ADR2G DC-DC power supply chips are used to generate 3.3v, 1.5v and 1.0v, and the maximum output current is 3A.

Three TPS7A7001 LDO power supply chips are used to generate 2.5v, 1.8v and 1.2v, and the maximum output current is 2A.

One TPS51200 power chip is used to generate 0.75v power for DDR3 chip.

One APW7136CCI power chip is used to generate 9.9v power for RGB industry screen.

One RT9284A power chip is used to generate 16V, 10.4v and -7v power for RGB industry screen.

One AAT1541A power chip is used to generate +5V and -5v power for MIPI DSI interface.

One TPS61161A power chip is used to generate 17.4v power for MIPI DSI interface backlight.

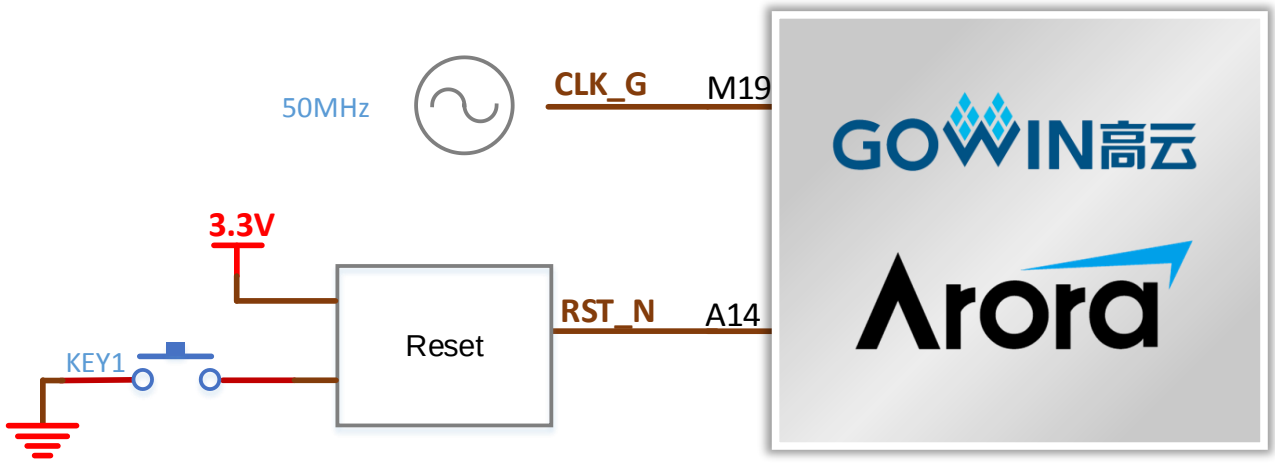
3.4 Clock, Reset

3.4.1 Introduction

The development board offers a 50MHz oscillator, connecting to the global clock pins.

The reset circuit adopts keys and dedicated reset chips. After powered on the device, the reset chip automatically generates a reset signal to reset the FPGA and Ethernet PHY chip. The 3.3V voltage is monitored in real time. The reset signal will be generated once an exception occurs. The reset signal can also be generated via the reset key.

Figure 3-5 Connection Diagram of Clock and Reset



3.4.2 Pins Distribution

Table 3-5 Clock and Reset Pins Distribution

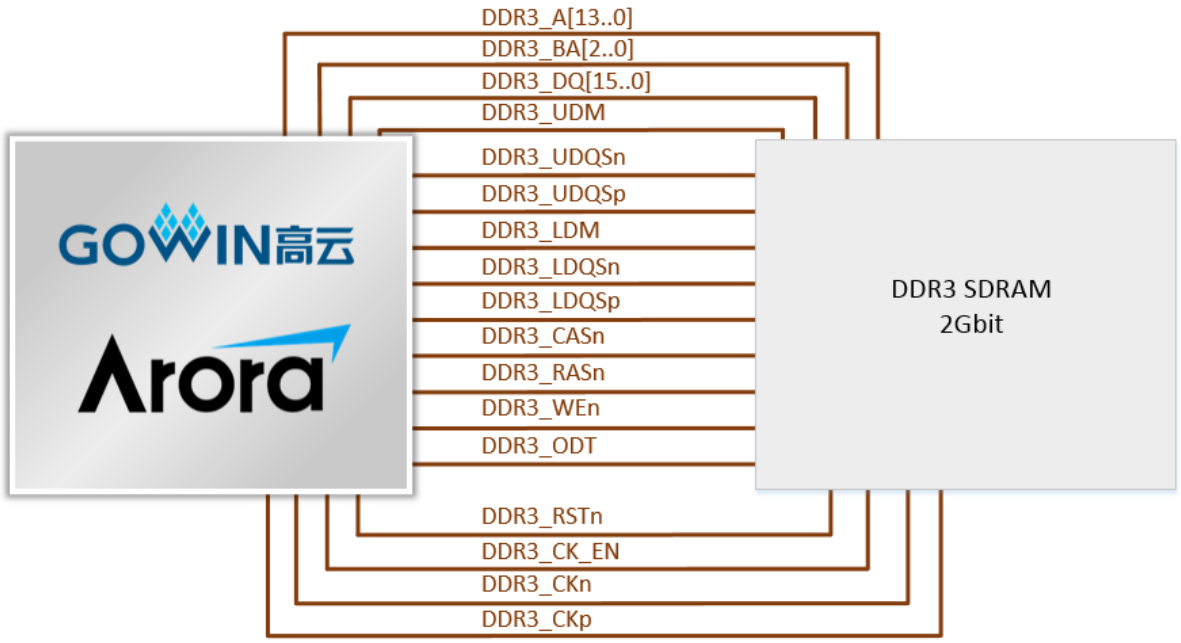
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_G	M19	2	3.3V	50MHz crystal oscillator Input
RST_N	A14	1	2.5V	Reset Signal, Active Low

3.5 DDR3

3.5.1 Introduction

The development board includes a DDR3 chip with 2Gbit storage space, 16 bits data bus width, and the highest data speed of 1600MT/s.

Figure 3-6 Connection Diagram of FPGA and DDR3



3.5.2 Pins Distribution

Table 3-6 DDR3 Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	G1	7	1.5V	Address
DDR3_A1	U5	6	1.5V	Address
DDR3_A2	G5	7	1.5V	Address
DDR3_A3	F5	7	1.5V	Address
DDR3_A4	V3	6	1.5V	Address
DDR3_A5	G2	7	1.5V	Address
DDR3_A6	AA22	3	1.5V	Address
DDR3_A7	H5	7	1.5V	Address
DDR3_A8	AB22	3	1.5V	Address
DDR3_A9	J4	7	1.5V	Address
DDR3_A10	R5	6	1.5V	Address
DDR3_A11	AA21	3	1.5V	Address
DDR3_A12	T5	6	1.5V	Address
DDR3_A13	AA1	6	1.5V	Address
DDR3_BA0	F4	7	1.5V	Bank address
DDR3_BA1	U4	6	1.5V	Bank address
DDR3_BA2	F3	7	1.5V	Bank address
DDR3_CASn	C3	7	1.5V	Column address strobe
DDR3_CK_EN	E3	7	1.5V	Clock Enable
DDR3_CKn	R22	3	1.5V	Differential clock
DDR3_CKp	P22	3	1.5V	Differential clock
DDR3_DQ0	M5	6	1.5V	Data
DDR3_DQ1	T3	6	1.5V	Data
DDR3_DQ2	M3	6	1.5V	Data
DDR3_DQ3	T2	6	1.5V	Data
DDR3_DQ4	Y1	6	1.5V	Data
DDR3_DQ5	U1	6	1.5V	Data
DDR3_DQ6	N3	6	1.5V	Data
DDR3_DQ7	V1	6	1.5V	Data
DDR3_DQ8	T1	7	1.5V	Data
DDR3_DQ9	K3	7	1.5V	Data
DDR3_DQ10	P1	7	1.5V	Data

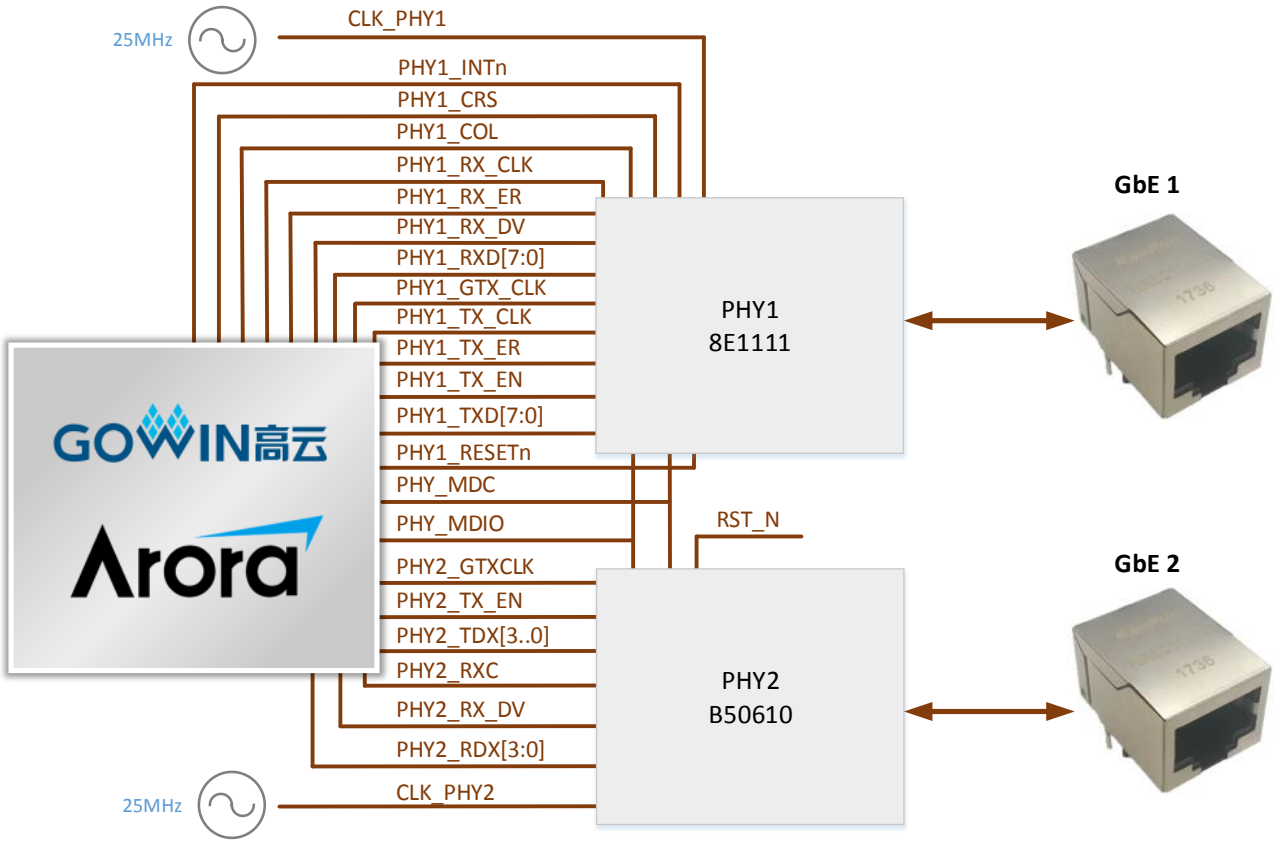
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_DQ11	J1	7	1.5V	Data
DDR3_DQ12	L5	7	1.5V	Data
DDR3_DQ13	H3	7	1.5V	Data
DDR3_DQ14	M1	7	1.5V	Data
DDR3_DQ15	H1	7	1.5V	Data
DDR3_LDM	R3	6	1.5V	Data input mask
DDR3_LDQSn	R4	6	1.5V	Data strobe
DDR3_LDQSp	P4	6	1.5V	Data strobe
DDR3_ODT	B2	7	1.5V	On-Die Termination Enable
DDR3_RASn	D1	7	1.5V	Row address strobe
DDR3_RSTn	W4	6	1.5V	Reset
DDR3_UDM	K4	7	1.5V	Data input mask
DDR3_UDQSn	L1	7	1.5V	Data strobe
DDR3_UDQSp	L2	7	1.5V	Data strobe
DDR3_WEn	C1	7	1.5V	Write enable

3.6 Ethernet Interface

3.6.1 Introduction

The development board has two Ethernet circuits and supports gigabit mode, which can be used to test hardware environment in the LED display applications, and Ethernet data transmission. The interface connected to other devices is RJ45 with the built-in transformer. The connection diagram is shown in Figure 3-7.

Figure 3-7 Connection Diagram of FPGA and Ethernet



3.6.2 Pins Distribution

Table 3-7 Ethernet Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY_MDC	H19	2	3.3V	Manage channel clock
PHY_MDIO	J18	2	3.3V	Manage channel data
PHY1_INTn	J19	2	3.3V	PHY1 interrupt signal
PHY1_CRS	B21	2	3.3V	PHY1 GMII and MII carrier interception
PHY1_COL	B20	2	3.3V	PHY1 GMII and MII conflicting signal
PHY1_RX_CLK	F20	2	3.3V	PHY1 Clock receive
PHY1_RX_ER	G19	2	3.3V	PHY1 error receive
PHY1_RX_DV	E20	2	3.3V	PHY1 receiving data valid
PHY1_RXD0	D20	2	3.3V	PHY1 receiving data channel 0
PHY1_RXD1	F19	2	3.3V	PHY1 receiving data channel 1
PHY1_RXD2	G18	2	3.3V	PHY1 receiving data channel 2
PHY1_RXD3	D19	2	3.3V	PHY1 receiving data channel 3
PHY1_RXD4	F18	2	3.3V	PHY1 receiving data channel 4
PHY1_RXD5	E19	2	3.3V	PHY1 receiving data channel 5
PHY1_RXD6	C20	2	3.3V	PHY1 receiving data channel 6
PHY1_RXD7	G17	2	3.3V	PHY1 receiving data channel 7
PHY1_GTX_CLK	C21	2	3.3V	PHY1 GMII transmitting clock
PHY1_TX_CLK	C22	2	3.3V	PHY1 MII transmitting clock
PHY1_TX_ER	E22	2	3.3V	PHY1 transmitting error
PHY1_TX_EN	D22	2	3.3V	PHY1 transmitting enable
PHY1_TXD0	F21	2	3.3V	PHY1 transmitting data channel 0
PHY1_TXD1	H18	2	3.3V	PHY1 transmitting data channel 1

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
PHY1_TXD2	G20	2	3.3V	PHY1 transmitting data channel 2
PHY1_TXD3	G22	2	3.3V	PHY1 transmitting data channel 3
PHY1_TXD4	G21	2	3.3V	PHY1 transmitting data channel 4
PHY1_TXD5	F22	2	3.3V	PHY1 transmitting data channel 5
PHY1_TXD6	H21	2	3.3V	PHY1 transmitting data channel 6
PHY1_TXD7	H22	2	3.3V	PHY1 transmitting data channel 7
PHY1_RESETn	H20	2	3.3V	PHY1 reset signal
PHY2_GTCLK	N19	2	3.3V	PHY2 transmitting clock
PHY2_TXD0	M21	2	3.3V	PHY2 transmitting data channel 0
PHY2_TXD1	L21	2	3.3V	PHY2 transmitting data channel 1
PHY2_TXD2	L22	2	3.3V	PHY2 transmitting data channel 2
PHY2_TXD3	K22	2	3.3V	PHY2 transmitting data channel 3
PHY2_TX_EN	J22	2	3.3V	PHY2 transmitting data enable
PHY2_RXC	L20	2	3.3V	PHY2 receiving clock
PHY2_RXD0	K20	2	3.3V	PHY2 receiving data channel 0
PHY2_RXD1	L19	2	3.3V	PHY2 receiving data channel 1
PHY2_RXD2	J20	2	3.3V	PHY2 receiving data channel 2
PHY2_RXD3	K19	2	3.3V	PHY2 receiving data channel 3
PHY2_RX_DV	K18	2	3.3V	PHY2 receiving data enable

3.7 LVDS interfaces

3.7.1 Introduction

The LVDS interfaces are the four 20 pins with the pitch of 2.00mm, of

which two are transmitting interface, and the other are receiving interface. Each interface includes five pairs of differential signals. These interfaces can also be used as GPIO, with BANK adjustable voltages of 3.3v, 2.5v and 1.8v. J13 needs to be set to 2.5V when LVDS is used.

Figure 3-8 LVDS TX Interface

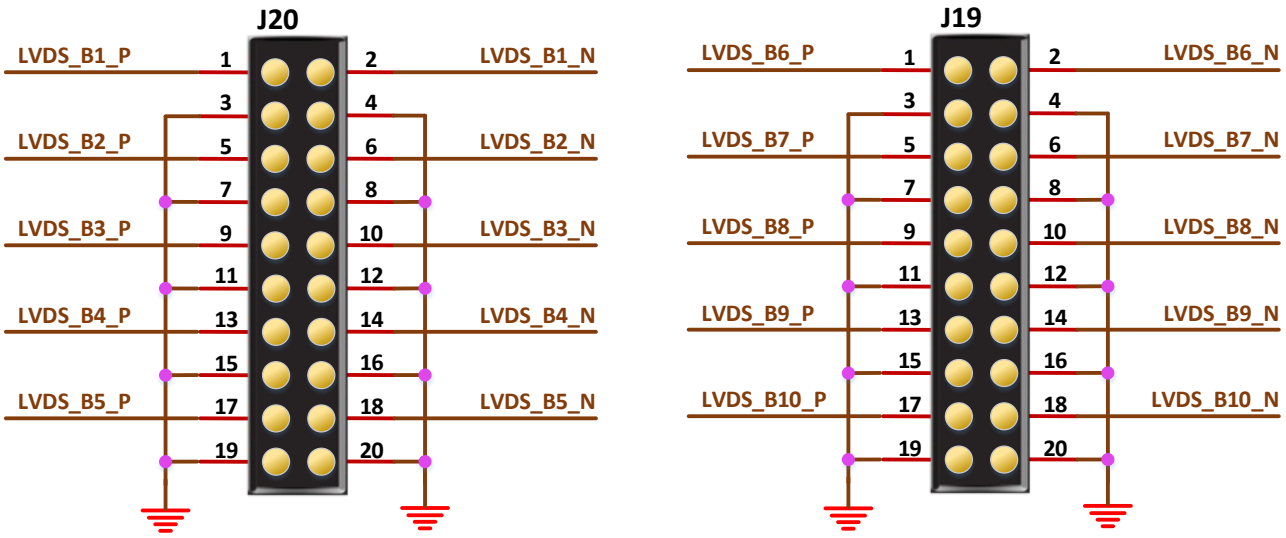
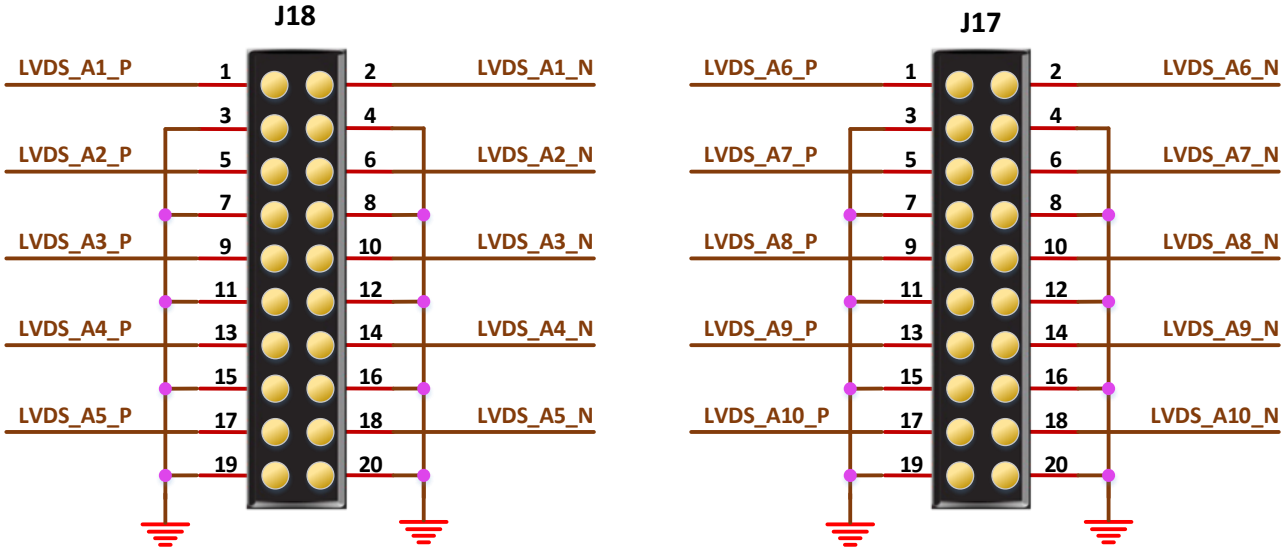


Figure 3-9 LVDS RX Interface



3.7.2 Pins Distribution

Table 3-8 LVDS TX Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS_B1_P	V16	4	2.5V	Differential Channel 1+
2	LVDS_B1_N	U16	4	2.5V	Differential Channel 1-
5	LVDS_B2_P	V17	4	2.5V	Differential Channel 2+
6	LVDS_B2_N	V18	4	2.5V	Differential Channel 2-
9	LVDS_B3_P	Y19	4	2.5V	Differential Channel 3+
10	LVDS_B3_N	Y18	4	2.5V	Differential Channel 3-
13	LVDS_B4_P	AA17	4	2.5V	Differential Channel 4+
14	LVDS_B4_N	Y17	4	2.5V	Differential Channel 4-
17	LVDS_B5_P	AB16	4	2.5V	Differential Channel 5+
18	LVDS_B5_N	AA16	4	2.5V	Differential Channel 5-

Table 3-9 LVDS TX2 Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS_B6_P	AB15	4	2.5V	Differential Channel 6+
2	LVDS_B6_N	AA15	4	2.5V	Differential Channel 6-
5	LVDS_B7_P	Y16	4	2.5V	Differential Channel 7+
6	LVDS_B7_N	W16	4	2.5V	Differential Channel 7-
9	LVDS_B8_P	V14	4	2.5V	Differential Channel 8+
10	LVDS_B8_N	V15	4	2.5V	Differential Channel 8-
13	LVDS_B9_P	AB12	4	2.5V	Differential Channel 9+

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
14	LVDS_B9_N	AA12	4	2.5V	Differential Channel 9-
17	LVDS_B10_P	W12	4	2.5V	Differential Channel 10+
18	LVDS_B10_N	W13	4	2.5V	Differential Channel 10-

Table 3-10 LVDS RX 1 Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS_A1_P	W19	4	2.5V	Differential Channel 1+
2	LVDS_A1_N	V19	4	2.5V	Differential Channel 1-
5	LVDS_A2_P	W17	4	2.5V	Differential Channel 2+
6	LVDS_A2_N	W18	4	2.5V	Differential Channel 2-
9	LVDS_A3_P	AB19	4	2.5V	Differential Channel 3+
10	LVDS_A3_N	AB20	4	2.5V	Differential Channel 3-
13	LVDS_A4_P	AA20	4	2.5V	Differential Channel 4+
14	LVDS_A4_N	Y20	4	2.5V	Differential Channel 4-
17	LVDS_A5_P	AB17	4	2.5V	Differential Channel 5+
18	LVDS_A5_N	AB18	4	2.5V	Differential Channel 5-

Table 3-11 LVDS RX 2 Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
1	LVDS_A6_P	Y14	4	2.5V	Differential Channel 6+
2	LVDS_A6_N	Y15	4	2.5V	Differential Channel 6-
5	LVDS_A7_P	W14	4	2.5V	Differential Channel 7+
6	LVDS_A7_N	W15	4	2.5V	Differential Channel 7-

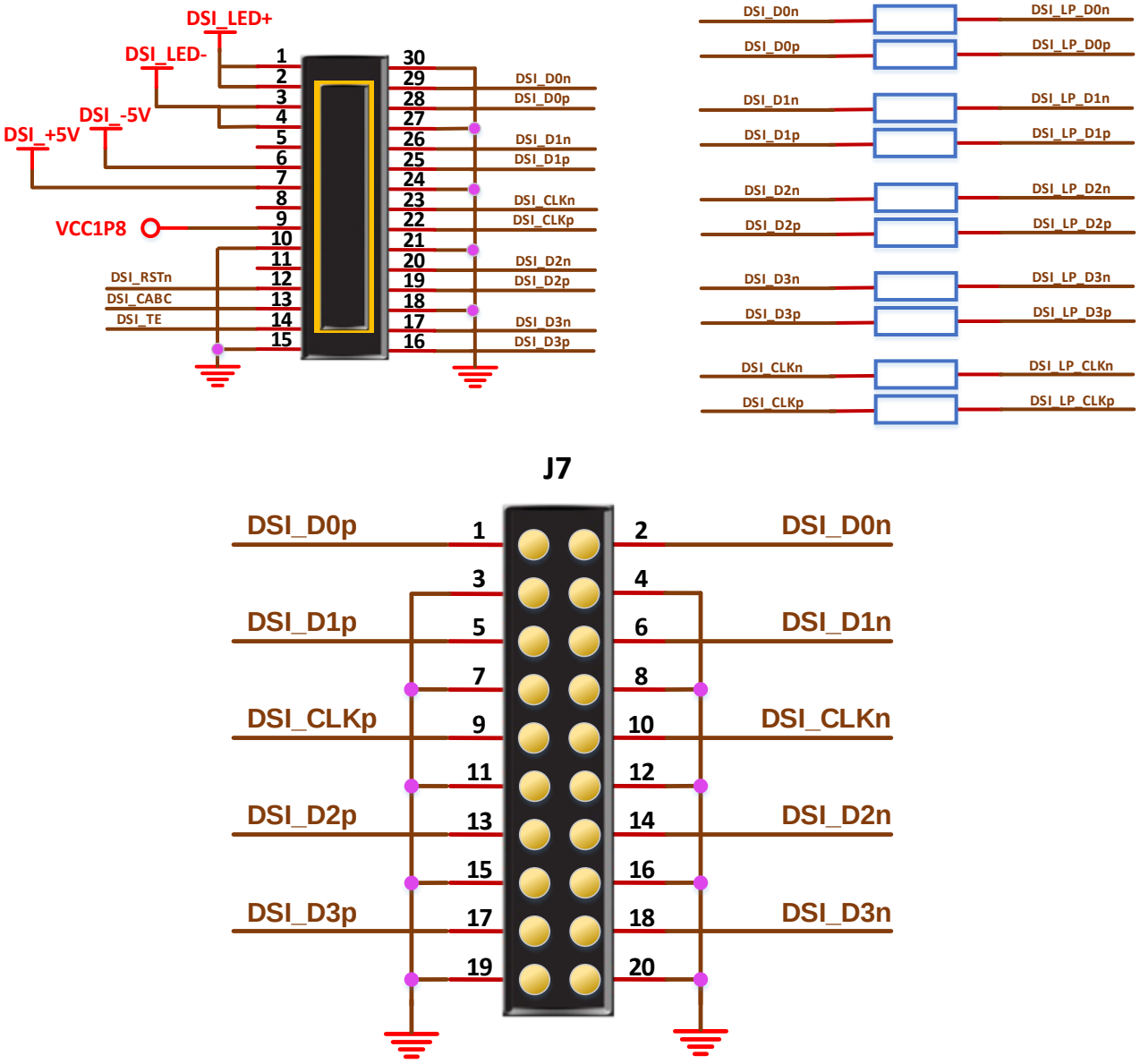
Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
9	LVDS_A8_P	AB13	4	2.5V	Differential Channel 8+
10	LVDS_A8_N	AB14	4	2.5V	Differential Channel 8-
13	LVDS_A9_P	Y12	4	2.5V	Differential Channel 9+
14	LVDS_A9_N	Y13	4	2.5V	Differential Channel 9-
17	LVDS_A10_P	V12	4	2.5V	Differential Channel 10+
18	LVDS_A10_N	V13	4	2.5V	Differential Channel 10-

3.8 MIPI DSI

3.8.1 Introduction

The DSI interface adopts the 30-contact stacked board connector, which channels to 5 pairs of differential signals, including one clock and four data, corresponding to TXD T550UZPA-75 mobile phone screen interface. At the same time, 5 lane DSI signals are channelled to 20pin double row pins with 2.00mm pitch.

Figure 3-10 Connection Diagram of MIPI DSI



3.8.2 Pins Distribution

Table 3-12 MIPI DSI Pins Distribution

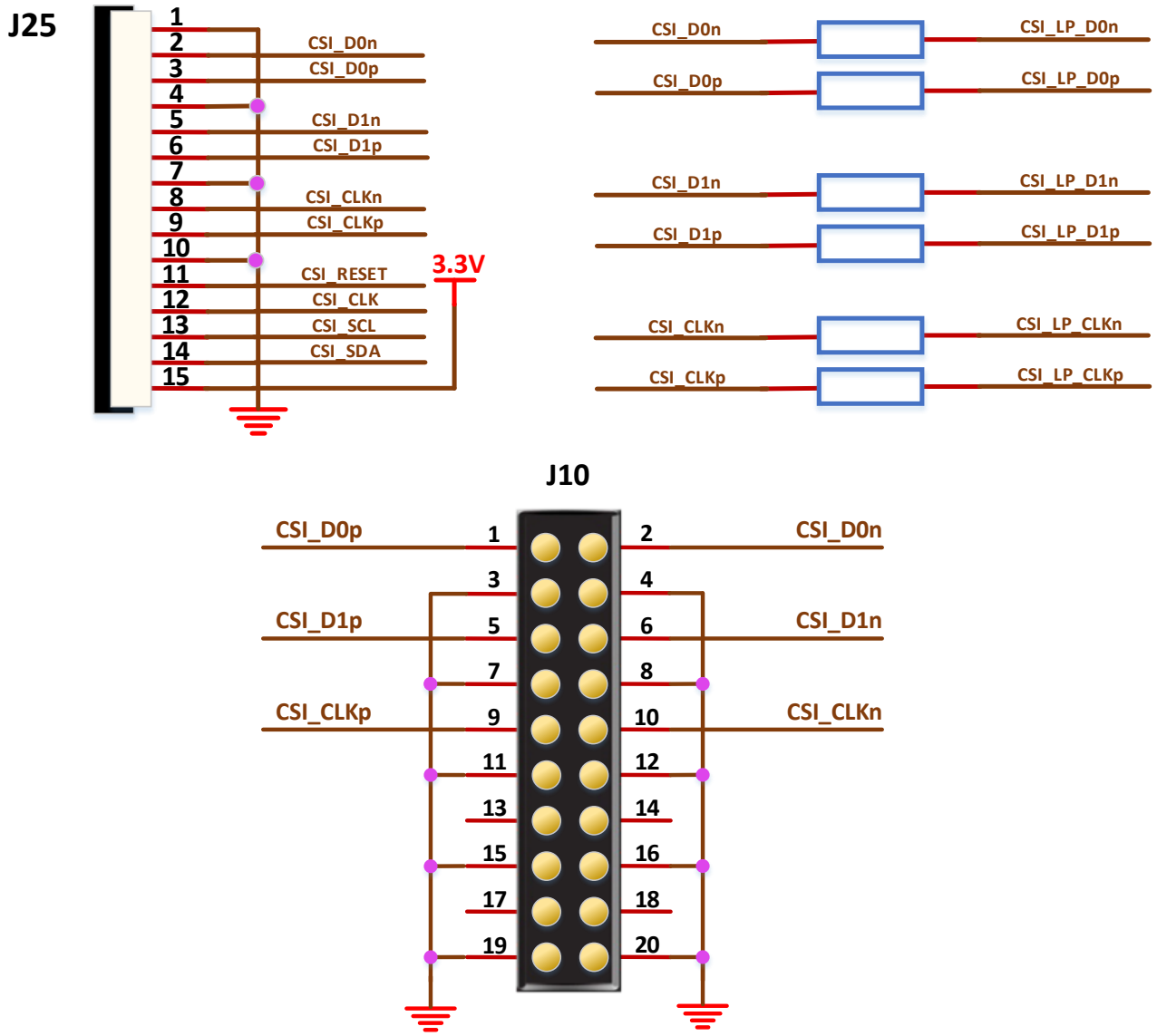
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
DSI_D0n	B22	1	2.5V	HS differential data 0-
DSI_D0p	A22	1	2.5V	HS differential data 0+
DSI_D1n	C19	1	2.5V	HS differential data 1-
DSI_D1p	C18	1	2.5V	HS differential data 1+
DSI_CLKn	A19	1	2.5V	HS Differential clock-
DSI_CLKp	A18	1	2.5V	HS Differential clock+
DSI_D2n	B17	1	2.5V	HS differential data 2-
DSI_D2p	A17	1	2.5V	HS differential data 2+
DSI_D3n	B15	1	2.5V	HS differential data 3-
DSI_D3p	A15	1	2.5V	HS differential data 3+
DSI_LP_D0n	C7	0	1.2V	LP single end data 0
DSI_LP_D0p	A7	0	1.2V	LP single end data 0
DSI_LP_D1n	A6	0	1.2V	LP single end data 1
DSI_LP_D1p	B7	0	1.2V	LP single end data 1
DSI_LP_CLKn	B6	0	1.2V	LP single end clock
DSI_LP_CLKp	D7	0	1.2V	LP single end clock
DSI_LP_D2n	D6	0	1.2V	LP single end data 2
DSI_LP_D2p	C6	0	1.2V	LP single end data 2
DSI_LP_D3n	A4	0	1.2V	LP single end data 3
DSI_LP_D3p	A5	0	1.2V	LP single end data 3
DSI_RSTn	A16	1	2.5V	Reset signal
DSI_CABC	B16	1	2.5V	Backlight control signal
DSI_TE	D16	1	2.5V	Tearing output signal

3.9 MIPI CSI

3.9.1 Introduction

MIPI CSI adopts 15pin connector with 1mm pitch. The interface includes 3 pairs of differential signals, amonng which one clock and two data include. Three lane differential signals are simultaneously channelled to 20pin double row pins with 2.00mm pitch. The connection diagram is shown in Figure 3-11.

Figure 3-11 Connection Diagram of MIPI CSI



3.9.2 Pins Distribution

Table 3-13 MIPI CSI Pins Distribution

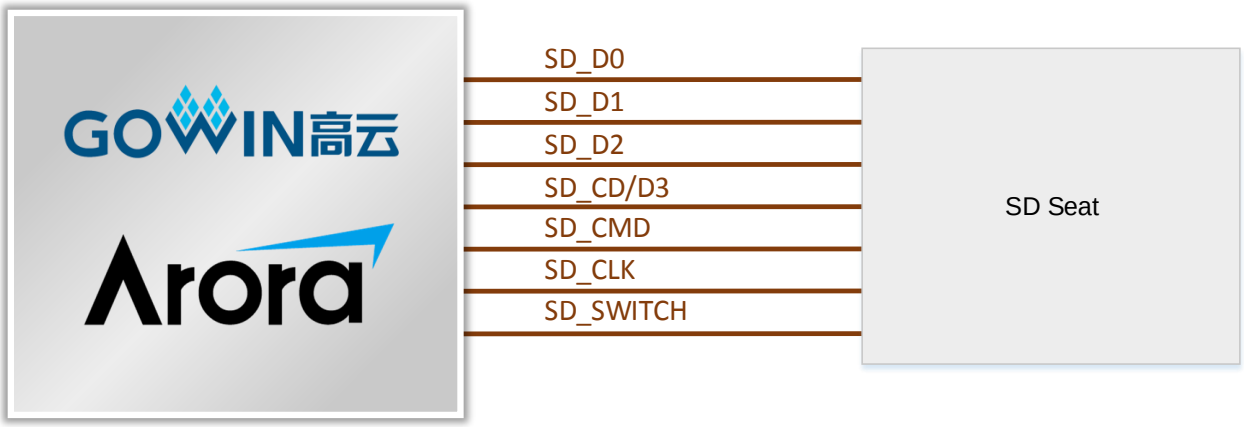
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CSI_D0n	C15	1	2.5V	HS differential data 0-
CSI_D0p	C14	1	2.5V	HS differential data 0+
CSI_D1n	E13	1	2.5V	HS differential data 1-
CSI_D1p	E12	1	2.5V	HS differential data 1+
CSI_CLKn	D12	1	2.5V	HS Differential clock-
CSI_CLKp	D11	1	2.5V	HS Differential clock+
CSI_LP_D0n	A2	0	1.2V	LP single end data 0
CSI_LP_D0p	A3	0	1.2V	LP single end data 0
CSI_LP_D1n	A1	0	1.2V	LP single end data 1
CSI_LP_D1p	B1	0	1.2V	LP single end data 1
CSI_LP_CLKn	C4	0	1.2V	LP single end clock
CSI_LP_CLKp	C5	0	1.2V	LP single end clock
CSI_RESET	E16	1	2.5V	Reset signal
CSI_CLK	C16	1	2.5V	Clock
CSI_SCL	D15	1	2.5V	I2C signal
CSI_SDA	E15	1	2.5V	I2C signal

3.10 SD Card

3.10.1 Introduction

The SD card slot on the board is the push-push type with eight contacts. It offers the detection of the card insertion. The connection diagram is shown in Figure 3-12.

Figure 3-12 Connection Diagram of SD Card



3.10.2 Pins Distribution

Table 3-14 SD Card Pins Distribution

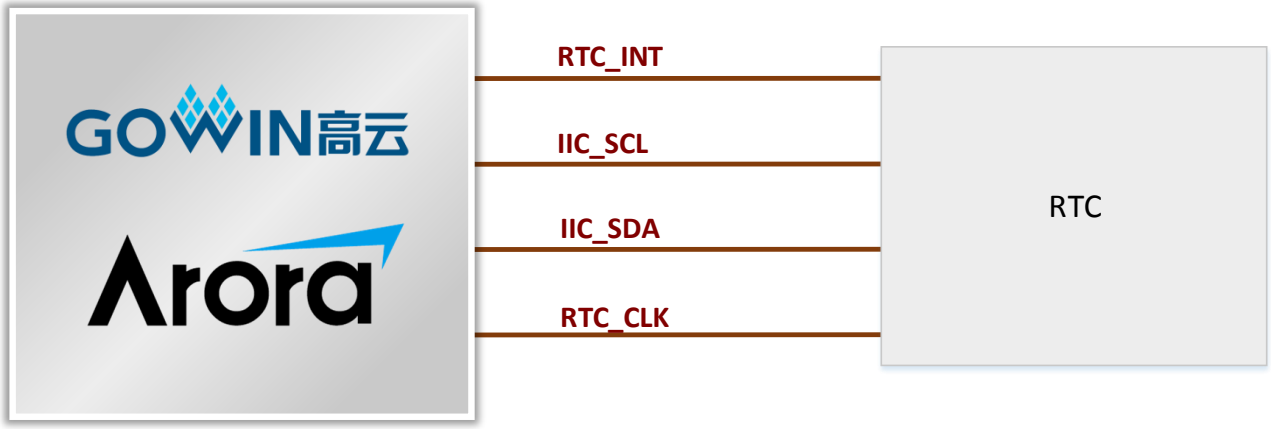
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SD_D0	W5	5	3.3V	Data bits 0
SD_D1	U6	5	3.3V	Data bits 1
SD_D2	Y6	5	3.3V	Data bits 2
SD_CD/D3	U7	5	3.3V	Card detection/Data bits 3
SD_CMD	W6	5	3.3V	Commands/Response
SD_CLK	V6	5	3.3V	Clock
SD_SWITCH	Y22	3	1.5V	Insertion Detection

3.11 RTC

3.11.1 Introduction

The real-time clock module adopts NXP PCF8563 and is externally connected with 32.768kHz quartz crystal. It can be powered by the power supply and the button battery of the development board. The communication interface with the FPGA is I2C. The connection diagram is as shown in the Figure3-13.

Figure3-13 Connection Diagram of RTC



3.11.2 Pins Distribution

Table 3-15 RTC Pins Distribution

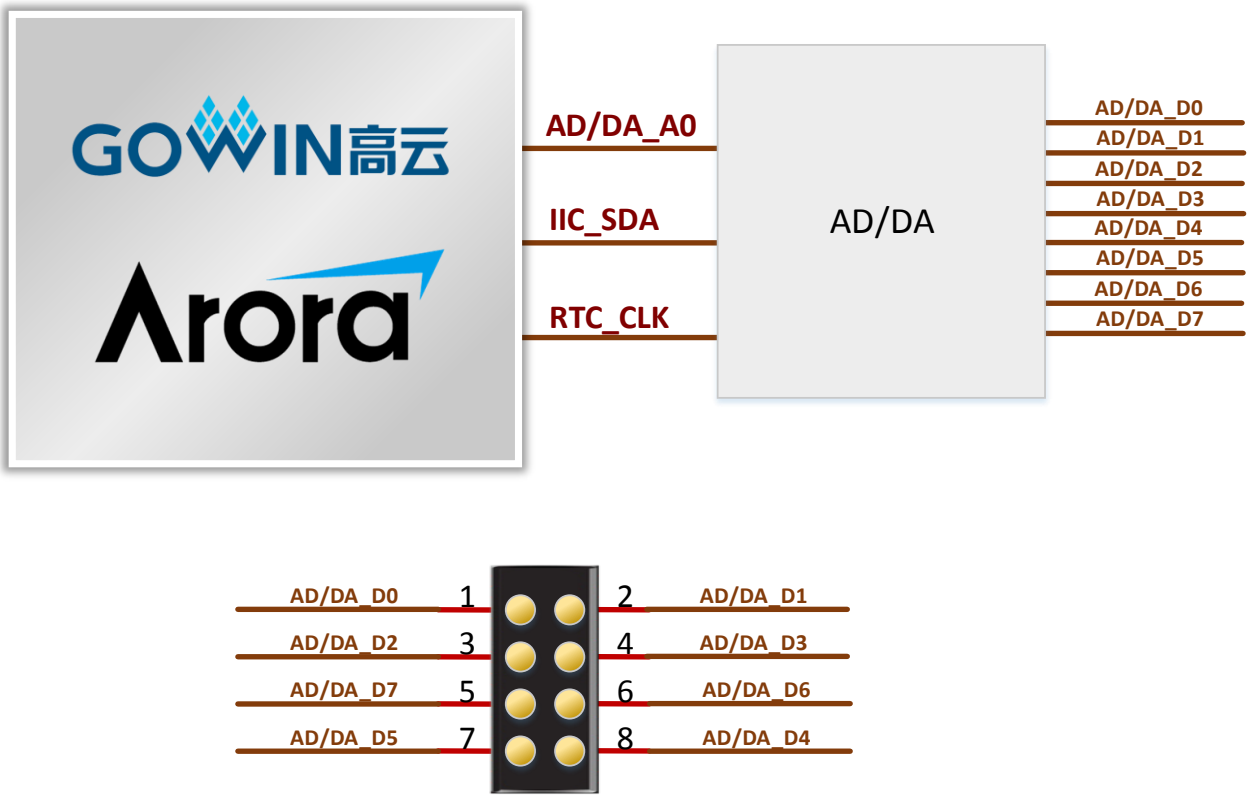
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
RTC_CLK	D13	1	2.5V	Clock signal
RTC_INT	D14	1	2.5V	Interrupt signal output
IIC_SCL	A13	1	2.5V	I2C signal
IIC_SDA	C13	1	2.5V	I2C signal

3.12 AD/DA

3.12.1 Introduction

The AD/DA module adopts ADI AD5593R chip. It is a 12-bit A/D and D/A converter with configurable 8-channel interface, which can be configured as any combination of ADC/DAC/GPIO and shares the I2C bus with the RTC module. The input and output interface adopts 8pin, and the connection diagram is as shown in Figure 3-14.

Figure 3-14 Connection Diagram of AD/DA



3.12.2 Pins Distribution

Table3-16 AD/DA Pins Distribution

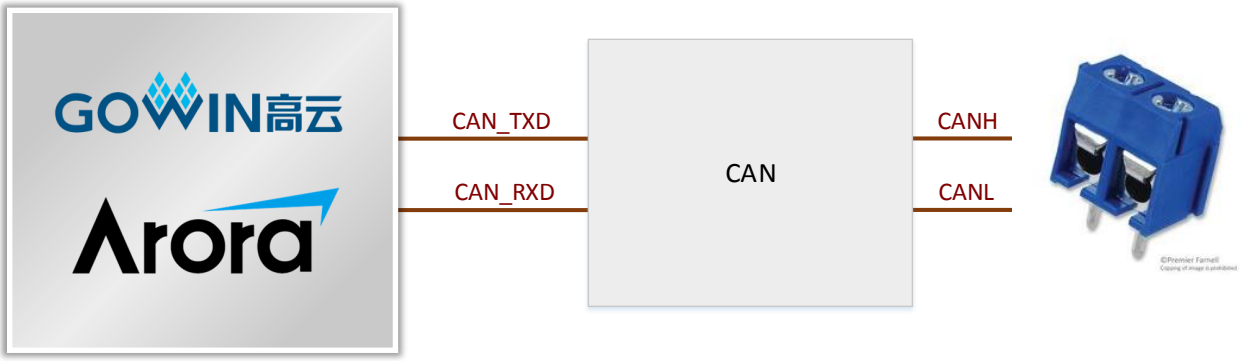
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
AD/DA_A0	E14	1	2.5V	Address input
IIC_SCL	A13	1	2.5V	I2C signal
IIC_SDA	C13	1	2.5V	I2C signal

3.13 CAN

3.13.1 Introduction

NXP TJA1050 transceiver chip is used to design CAN interface. The FPGA communicates with the transceiver through the UART interface, and the maximum transmission rate is 1Mbps. The connection diagram is as follows:

Figure 3-15 Connection Diagram of CAN



3.13.2 Pins Distribution

Table 3-17 CAN Pins Distribution

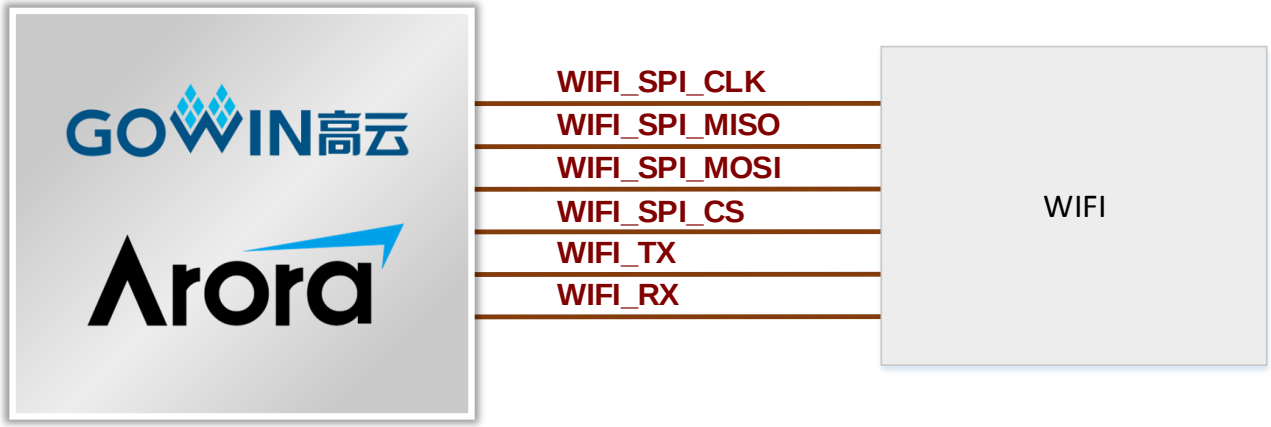
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
CAN_TXD	C11	1	2.5V	Data transmission
CAN_RXD	C12	1	2.5V	Data receive

3.14 WIFI

3.14.1 Introduction

The ESP-WROOM-02 WIFI module of Lexin is adopted to support SPI and UART. SPI transmission rate is 20Mbps. The connection diagram is shown in Figure 3-16.

Figure 3-16 Connection Diagram of WIFI



3.14.2 Pins Distribution

Table 3-18 WIFI Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
WIFI_SPI_CLK	D9	0	1.2V	SPI clock
WIFI_SPI_MISO	A10	0	1.2V	SPI data
WIFI_SPI_MOSI	B8	0	1.2V	SPI data
WIFI_SPI_CS	C8	0	1.2V	SPI Chip select
WIFI_TX	D8	0	1.2V	UART transmit
WIFI_RX	A9	0	1.2V	UART receive

3.15 GPIO

3.15.1 Introduction

Two double-column pins with 2.54mm pitch channelling 34 GPIOs are reserved on the development board for user testing. The 40pin interface is connected to Bank5. The I/O level is 3.3v, and the 20pin interface is reused GPIO with 40pin interface, as shown in Figure 3-17 and Figure 3-18.

Figure 3-17 40pin Interface

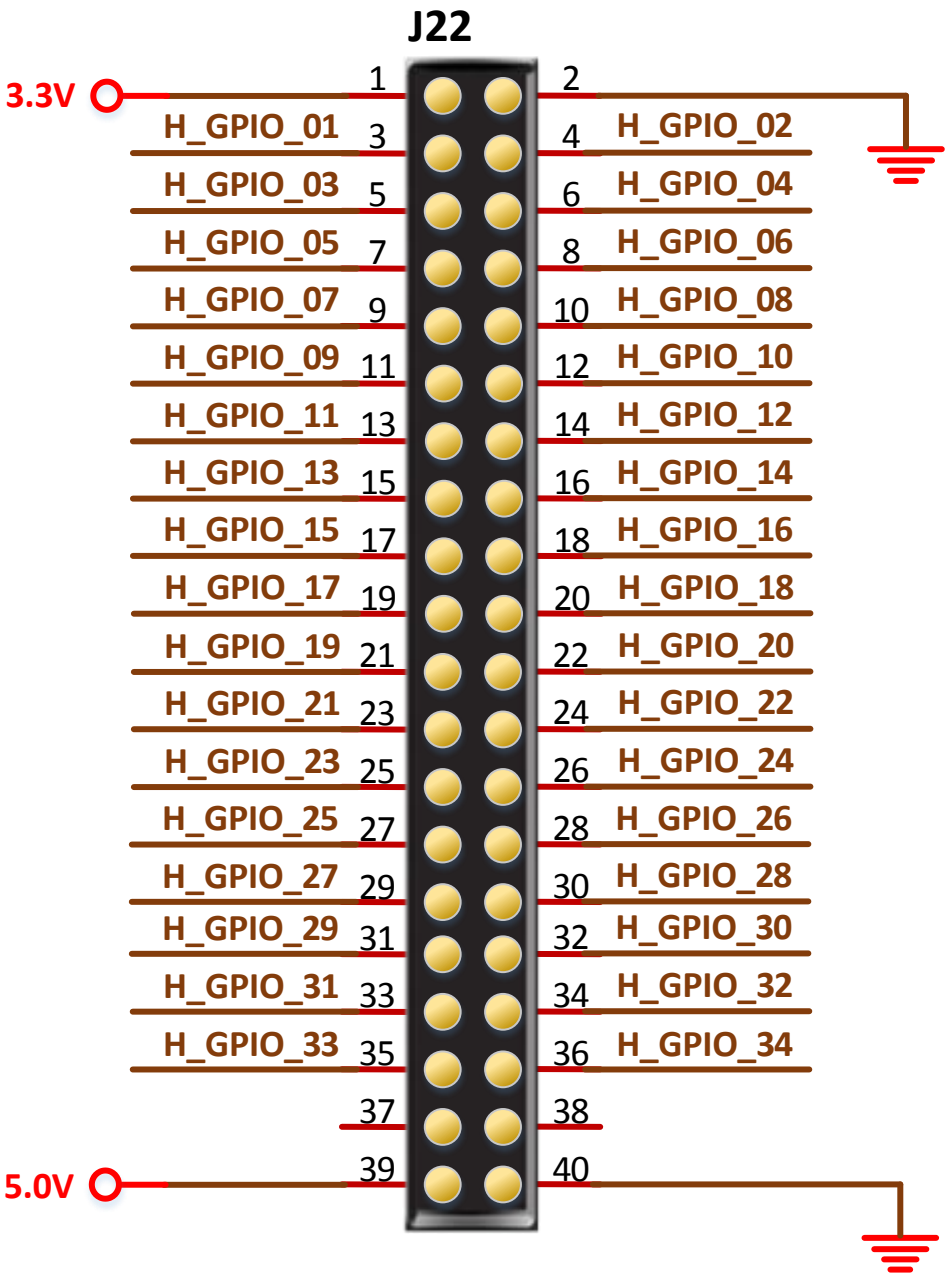
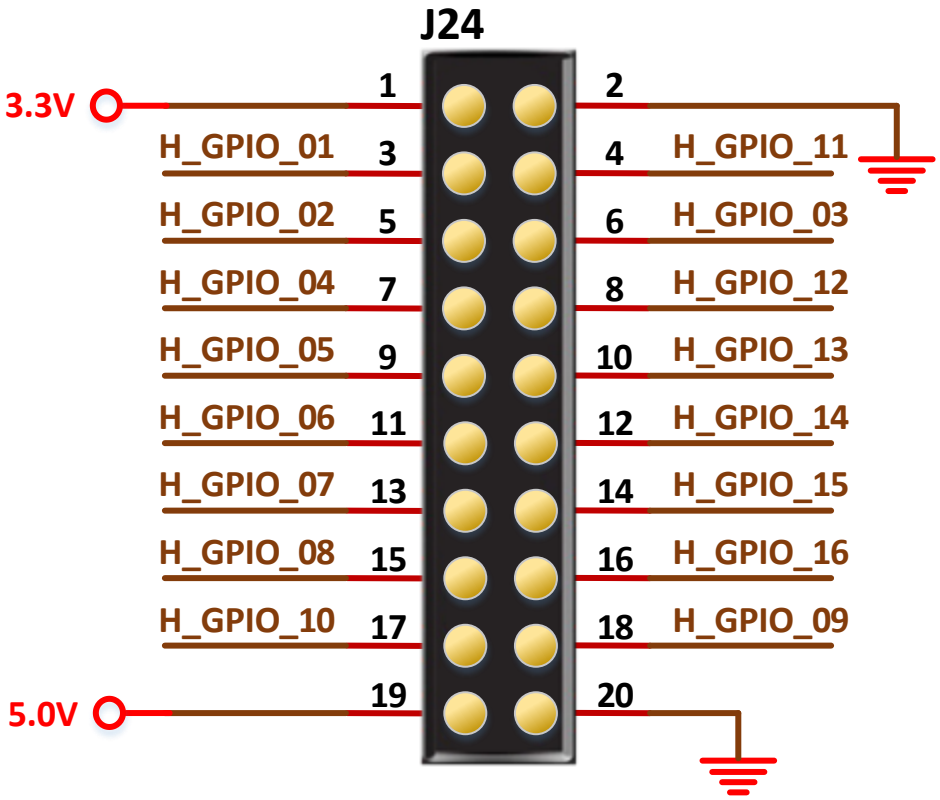


Figure 3-18 20pin Interface



3.15.2 Pins Distribution

Table 3-19 40pin Interface Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
3	H_GPIO_01	AA11	5	3.3V	General I/O
4	H_GPIO_02	V11	5	3.3V	General I/O
5	H_GPIO_03	AB11	5	3.3V	General I/O
6	H_GPIO_04	V9	5	3.3V	General I/O
7	H_GPIO_05	Y11	5	3.3V	General I/O
8	H_GPIO_06	Y3	5	3.3V	General I/O
9	H_GPIO_07	V10	5	3.3V	General I/O
10	H_GPIO_08	W11	5	3.3V	General I/O
11	H_GPIO_09	W10	5	3.3V	General I/O
12	H_GPIO_10	Y10	5	3.3V	General I/O
13	H_GPIO_11	W9	5	3.3V	General I/O
14	H_GPIO_12	Y8	5	3.3V	General I/O
15	H_GPIO_13	Y9	5	3.3V	General I/O
16	H_GPIO_14	AB10	5	3.3V	General I/O
17	H_GPIO_15	V7	5	3.3V	General I/O
18	H_GPIO_16	AB9	5	3.3V	General I/O

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
19	H_GPIO_17	Y7	5	3.3V	General I/O
20	H_GPIO_18	AA8	5	3.3V	General I/O
21	H_GPIO_19	W7	5	3.3V	General I/O
22	H_GPIO_20	AB8	5	3.3V	General I/O
23	H_GPIO_21	V8	5	3.3V	General I/O
24	H_GPIO_22	W8	5	3.3V	General I/O
25	H_GPIO_23	AB7	5	3.3V	General I/O
26	H_GPIO_24	AA7	5	3.3V	General I/O
27	H_GPIO_25	AB6	5	3.3V	General I/O
28	H_GPIO_26	AA6	5	3.3V	General I/O
29	H_GPIO_27	Y5	5	3.3V	General I/O
30	H_GPIO_28	AB5	5	3.3V	General I/O
31	H_GPIO_29	AB4	5	3.3V	General I/O
32	H_GPIO_30	Y4	5	3.3V	General I/O
33	H_GPIO_31	AB3	5	3.3V	General I/O
34	H_GPIO_32	AA3	5	3.3V	General I/O
35	H_GPIO_33	AB2	5	3.3V	General I/O
36	H_GPIO_34	AB1	5	3.3V	General I/O

Table 3-20 20pin Interface Pins Distribution

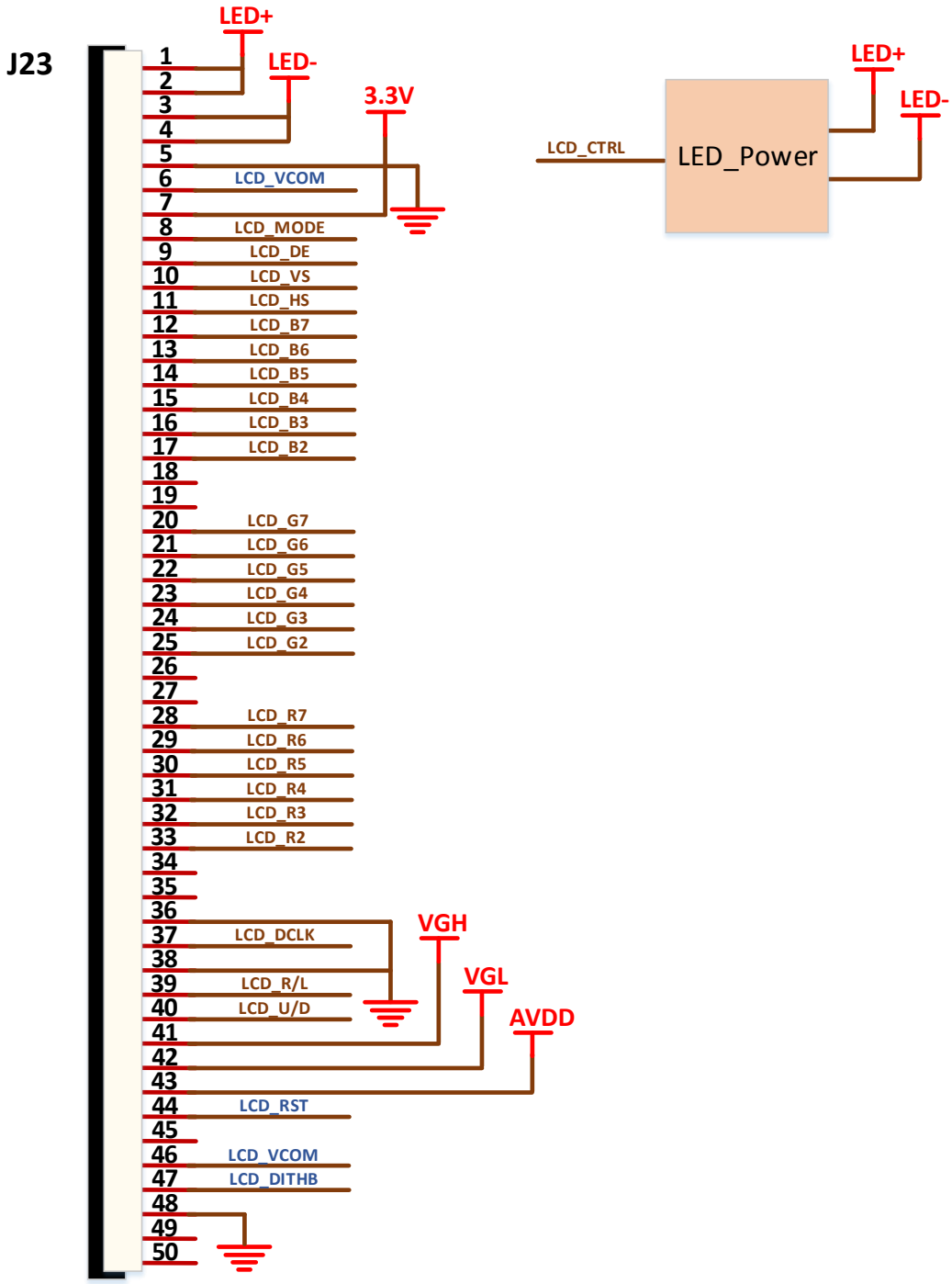
Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
3	H_GPIO_01	AA11	5	3.3V	General I/O
4	H_GPIO_11	W9	5	3.3V	General I/O
5	H_GPIO_02	V11	5	3.3V	General I/O
6	H_GPIO_03	AB11	5	3.3V	General I/O
7	H_GPIO_04	V9	5	3.3V	General I/O
8	H_GPIO_12	Y8	5	3.3V	General I/O
9	H_GPIO_05	Y11	5	3.3V	General I/O
10	H_GPIO_13	Y9	5	3.3V	General I/O
11	H_GPIO_06	Y3	5	3.3V	General I/O
12	H_GPIO_14	AB10	5	3.3V	General I/O
13	H_GPIO_07	V10	5	3.3V	General I/O
14	H_GPIO_15	V7	5	3.3V	General I/O
15	H_GPIO_08	W11	5	3.3V	General I/O
16	H_GPIO_16	AB9	5	3.3V	General I/O
17	H_GPIO_10	Y10	5	3.3V	General I/O
18	H_GPIO_09	W10	5	3.3V	General I/O

3.16 Industry Screen Interface

3.16.1 Introduction

This interface adopts 50pin FPC connector with 0.5mm pitch. The pin definition conforms to the industry screen of AT070TN92 model, and all I/O and 40PIN pin share GPIO of FPGA, as shown in Figure 3-19.

Figure 3-19 50pin FPC Interface



3.16.2 Pins Distribution

Table 3-21 50pin FPC Pins Distribution

Pins Number	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
8	LCD_MODE	W10	5	3.3V	DE or SYNC mode selection
9	LCD_DE	Y8	5	3.3V	Data input enable
10	LCD_VS	W9	5	3.3V	Column synchronization signal
11	LCD_HS	AB10	5	3.3V	Row synchronization signal
12	LCD_B7	Y9	5	3.3V	Blue data bit7
13	LCD_B6	AB9	5	3.3V	Blue data bit6
14	LCD_B5	V7	5	3.3V	Blue data bit5
15	LCD_B4	AA8	5	3.3V	Blue data bit4
16	LCD_B3	Y7	5	3.3V	Blue data bit3
17	LCD_B2	W8	5	3.3V	Blue data bit2
20	LCD_G7	V8	5	3.3V	Green data bit7
21	LCD_G6	AB8	5	3.3V	Green data bit6
22	LCD_G5	W7	5	3.3V	Green data bit5
23	LCD_G4	AA7	5	3.3V	Green data bit4
24	LCD_G3	AB7	5	3.3V	Green data bit3
25	LCD_G2	AA6	5	3.3V	Green data bit2
28	LCD_R7	AB6	5	3.3V	Red data bit7
29	LCD_R6	AB5	5	3.3V	Red data bit6
30	LCD_R5	Y5	5	3.3V	Red data bit5
31	LCD_R4	Y4	5	3.3V	Red data bit4
32	LCD_R3	AB4	5	3.3V	Red data bit3
33	LCD_R2	AB1	5	3.3V	Red data bit2
37	LCD_DCLK	AB2	5	3.3V	Sampling clock
39	LCD_R/L	AA3	5	3.3V	Select left or right
40	LCD_U/D	AB3	5	3.3V	Select up or down

Table 3-22 LCD Screen Brightness Control Pins Distribution

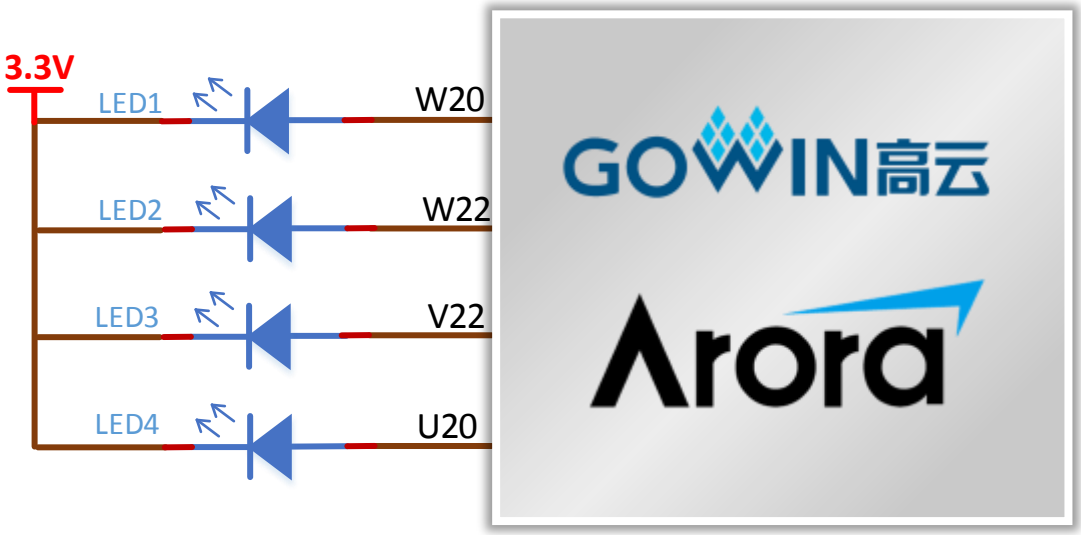
Power chip Pin No.	Signal Name	FPGA Pin No.	BANK	I/O Level	Description
4	LCD_CTR	A12	0	1.2V	LCD screen brightness control

3.17 LED

3.17.1 Introduction

There are four blue LED lights in the development board, which can be used by the user to display the status. When the output signal of FPGA corresponding pin is low, the LED is lit up.When the output signal is high, the LED is off. The connection diagram is shown in Figure 3-20.

Figure 3-20 Connection Diagram of LED



3.17.2 Pins Distribution

Table 3-23 LED Indicator Pins Distribution

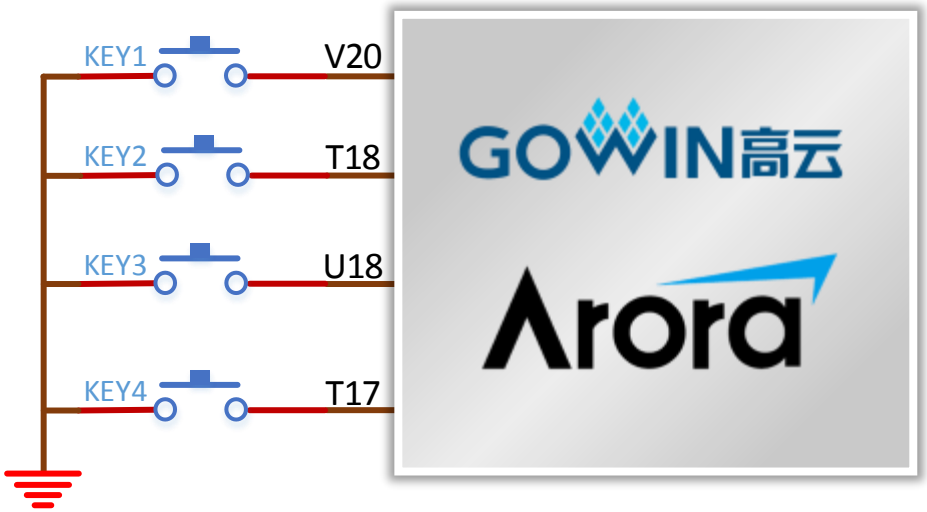
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	W20	3	1.5V	LED indicator 1
LED2	W22	3	1.5V	LED indicator 2
LED3	V22	3	1.5V	LED indicator 3
LED4	U20	3	1.5V	LED indicator 4

3.18 Keys

3.18.1 Introduction

The development board has four key switches that can be used to control input during testing. When the key is pressed, the input is low. The connection diagram is shown in Figure 3-21.

Figure 3-21 Keys Circuit



3.18.2 Pins Distribution

Table 3-24 Keys Pins Distribution

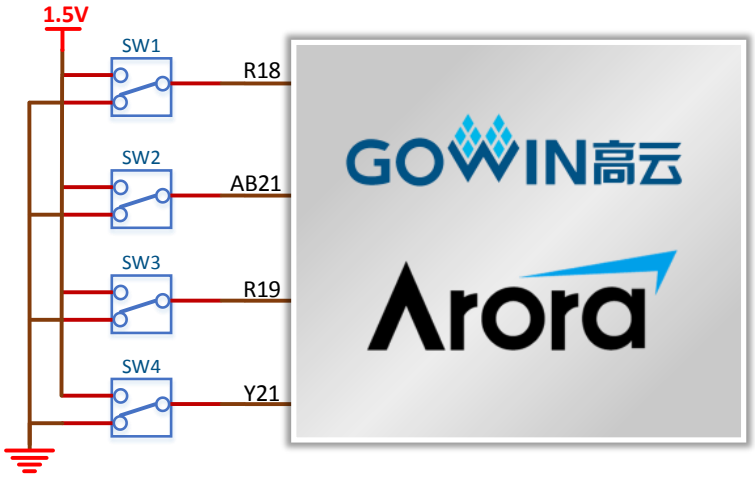
Signal Name	FPGA Pin No.	BANK	I/O Level	Description
KEY1	V20	3	1.5V	KEY1
KEY2	T18	3	1.5V	KEY2
KEY3	U18	3	1.5V	KEY3
KEY4	T17	3	1.5V	KEY4

3.19 Switches

3.19.1 Introduction

There are four slide switches in the development board to control input during testing. The connection diagram is shown in Figure 3-22.

Figure 3-22 Switches Circuit



3.19.2 Pins Distribution

Table 3-25 Switches Pins Distribution

Signal Name	FPGA Pin No.	BANK	I/O Level	Description
SW1	R18	3	1.5V	Slide switch1
SW2	AB21	3	1.5V	Slide switch2
SW3	R19	3	1.5V	Slide switch3
SW4	Y21	3	1.5V	Slide switch4


GOWIN
PROGRAMMING FOR FUTURE