

PRELIMINARY

iChip™

iChip CO110PC

# Data Sheet

Ver. 0.22



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# 1 Introduction

## Description

iChip™ CO110PC Internet Controller™ is a high-performance, firmware-based intelligent peripheral device that provides Internet connectivity solutions for a wide range of embedded devices. The firmware provides Internet communication via dial-up and wireless modems. CO110PC is packaged in a LQFP 48-pin form factor.

Its serial host interface supports up to 230 kbits/second. CO110PC also features a Sleep mode for saving energy. CO110PC operates in the industrial temperature range.

As an embedded, self-contained Internet engine, iChip acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip's domain.

A serial link interfaces iChip CO110PC to a device's host processor via an on-chip UART. iChip CO110PC also directly interfaces a serial data modem, through which it supports independent communications on the Internet via a dial-up or wireless ISP connection. In addition to supporting dial-up modems, iChip CO110PC also supports CDMA, CDMA2000, GPRS, GSM, and TDMA cellular modems.

Future support is planned for General Purpose I/O pins; SPI and I<sup>2</sup>C.

Through its host Application Programming Interface (API), iChip accepts commands formatted in Connect One's AT+i™ extension to the industry-standard Hayes AT command set. iChip supports several levels of status reporting to the host. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data;

The baseline firmware version in CO110PC supports up to 10 simultaneous TCP and UDP sockets to send and receive data over the Internet; and fetch HTML web pages. It also supports two listening sockets.

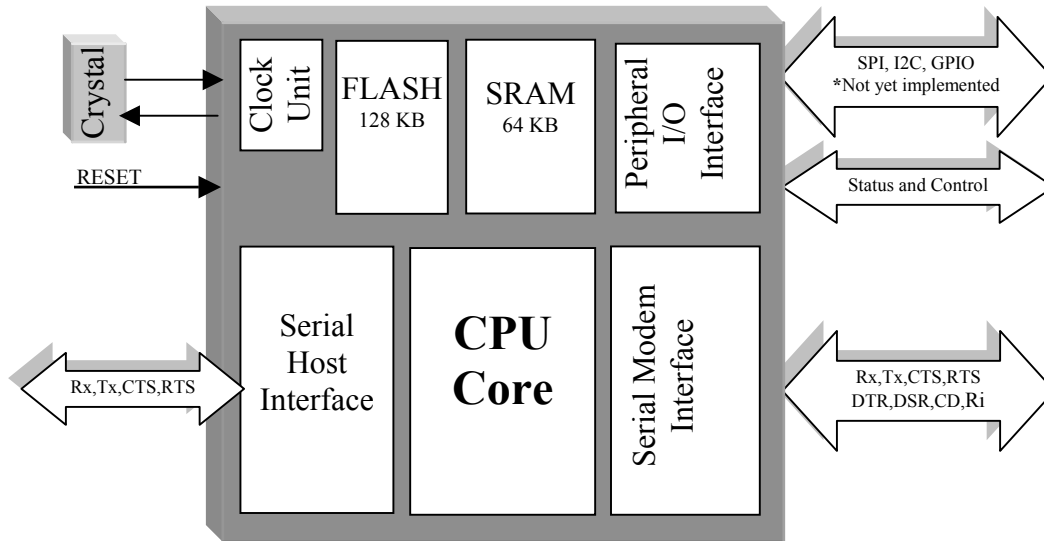
In addition to supporting TCP and UDP sockets, optional firmware versions provide support for:

- (1) Transmitting textual Email messages and manipulate files and directories via FTP; or
- (2) Operating in SerialNET mode, in which iChip automatically routes local serial data to/from the Internet.

When the host CPU issues standard AT commands, iChip gains direct access to the modem, and automatically operates in Transparent mode, emulating a direct host-to-modem environment.

Upon receiving an AT+i command, iChip operates in Internet mode, controls the modem and independently manages a standard Internet connection. iChip provides all the necessary procedures to log onto an ISP, authenticate the user and establish the Internet session.

## Functional Block Diagram



### General Features

- Microprocessor-controllable through a serial connection.
- 128KB flash and 64KB SRAM memory.
- Driven by Connect One's "AT+i" extension to the AT command set.
- Supports transparent direct modem access.
- Stand-alone Internet communication capabilities.
- Opens up to 10 simultaneous TCP or UDP sockets and up to 2 Listen (server) sockets.
- Sleep mode.
- 3.3-volts, CMOS technology for I/O and 1.8 volt for core.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Internal "Watch-Dog" guard circuit.
- Auto baud rate detection.
- Supports up to 230,400 bps in Serial mode.
- Includes hardware and software flow control.
- 48 pin LQFP package (7 x 7 x 1.4mm).

### Dial-up Features

- Supports dial-up Internet Protocols: PPP, LCP, IPCP, with PAP or CHAP authentication.
- Supports data modems up to 56 Kbps.
- Supports CDMA, CDMA2000, GPRS, GSM and TDMA wireless modems.
- RAS support for dial-in PPP connection.
- Stay-on-line feature for multiple send/receive sessions.
- Transparent mode supports direct modem commands.
- "Always Online" mode with communications "watchdog" and automatic reconnect.
- IP Registration.

### Standard Internet Protocols

- Standard version supports: IP, TCP, UDP, DNS, HTTP client, PING

### Optional Internet Protocols

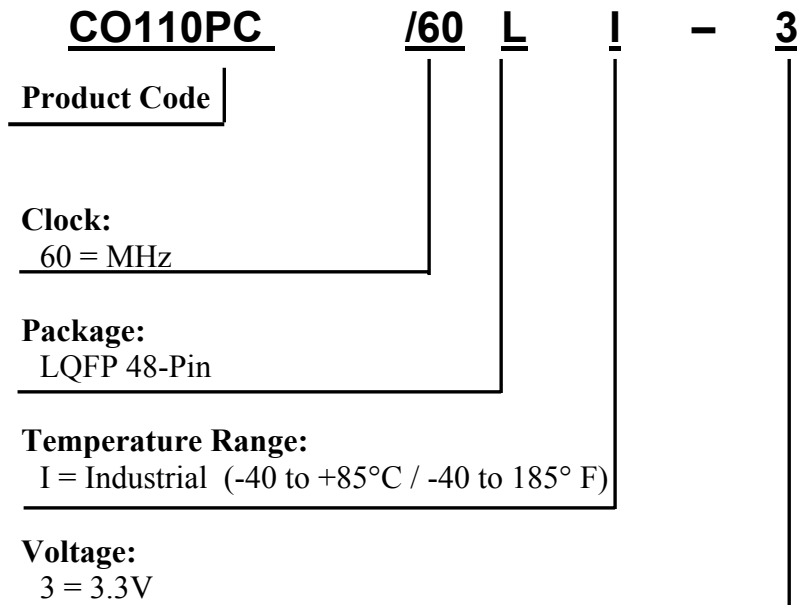
- Optional firmware versions support:
  - SMTP and FTP clients
  - SerialNET mode for serial-to-Internet routing



## 2 Ordering Information

### 2.1 iChip Order Number

Connect One's standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



### 3 Pin Descriptions

#### 3.1 iChip CO110PC Pin Assignments

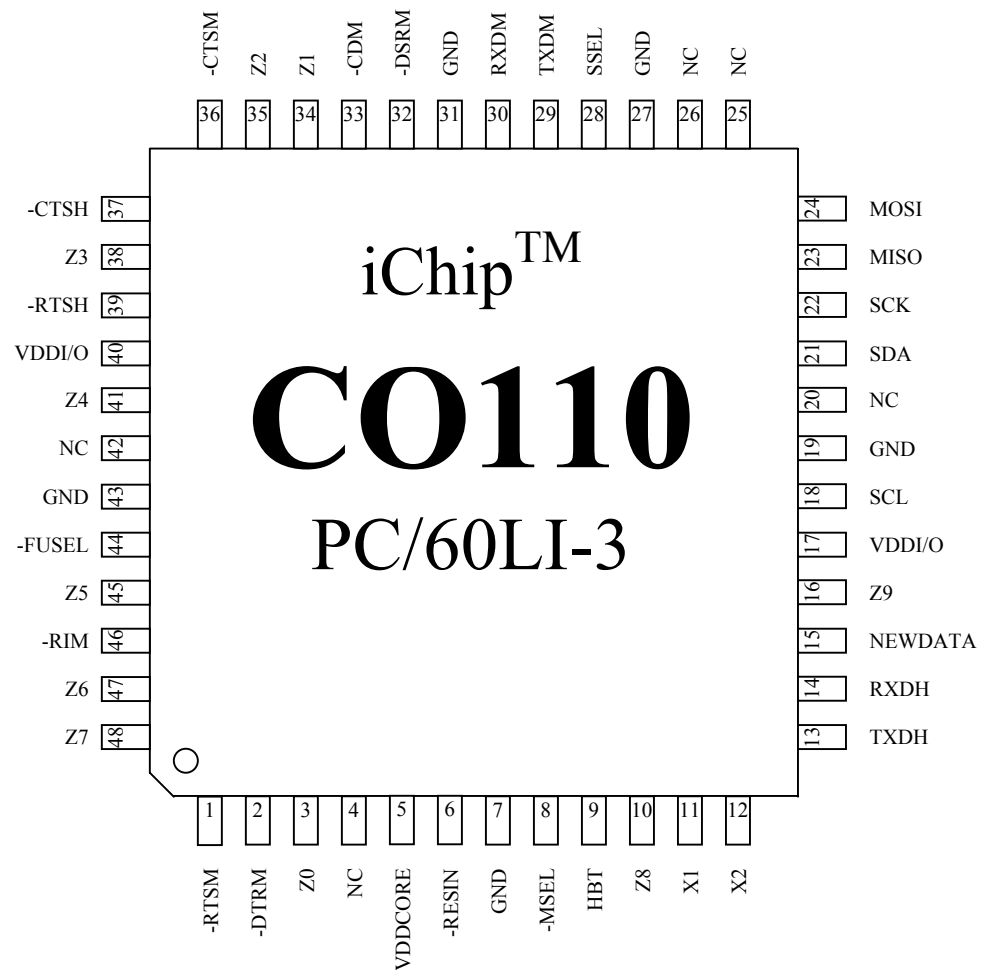


Figure 1: Pin-out for 48-pin LQFP

## 3.2 iChip Pin Functional Descriptions

### 3.2.1 Miscellaneous Signals

Signal	Type	Pin No.	Description
-MSEL	I	8	<p>Mode Select: When held LOW during power-up:</p> <ol style="list-style-type: none"> <li>1. Forces iChip into auto baud rate detection.</li> <li>2. If iChip is in SerialNET mode – iChip exits SerialNET mode.</li> </ol> <p>When not used <b>must</b> be pulled up to VDDi/o.</p>
-RESIN	I	6	<p>-RESET INPUT: When -RESIN is LOW, iChip immediately terminates its present activity and clears its internal logic.</p> <p>-RESIN must be held LOW for at least 10 ms after power reaches 90%.</p> <p>This input is provided with a Schmidt trigger to facilitate power-on reset generation via an RC network.</p>
X1	I	11	<p>Crystal Input: This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.</p> <p>To provide iChip with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.</p> <p>The crystal must be 14.7546MHz.</p>
X2	O	12	<p>Crystal Output: This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit.</p>
HBT	O	9	<p>Heart Beat: Provides a 50% duty cycle, 40 mSec period square wave, when iChip firmware is properly running.</p>

Signal	Type	Pin No.	Description
NEWDATA	O	15	NEWDATA: This signal is raised when new data in one or more sockets is available, or when a remote browser has changed a Web parameter. It is lowered when <i>any</i> socket or Web parameter is read.
-FUSEL	I	44	F/U SELECT: When LOW during power-up, iChip enters Firmware Update mode. When not used <b>must</b> be pulled up to VDDi/o.
Z[9-0]	I/O	16,10,48, 47,45,41, 38,35,34,3	General Purpose I/O (GPIO) – reserved for future use. These pins should be left NC (Not Connected).
GND	P	7,19,27, 31,43	Ground: iChip Ground signal.
VDDcore	P	5,	Power Supply: This pin supplies power (+1.8V) to iChip's core.
VDD I/O	P	17,40	Power Supply: This pin supplies power (+3.3V) to iChip's I/O pins.
NC	---	4,20,25, 26,42	NC (Not Connected) Pins.

### 3.2.2 Host Serial Interface Signals

Signal	Type	Pin No.	Description
TXDH	O	13	Transmit Data Host: This pin supplies asynchronous serial transmit data to the host.
RXDH	I	14	Receive Data Host: This pin supplies asynchronous serial receive data from the host. When not used, this pin should be pulled up to VDDi/o.
-CTSH	I	37	Clear-to-Send Host: -CTSH is active only when host hardware flow control is enabled. When -CTSH is LOW, flow control is enabled for the host serial port, i.e., iChip may transmit to the host. When -CTSH is HIGH, iChip will stop transmitting to the host. -CTSH is sampled only at the beginning of a transmission frame. If -CTSH is raised while a character frame is being transmitted, that frame will be completed. Connect -CTSH to -RTSH when not in use.
-RTSH	O	39	Ready-to-Send Host: -RTSH is active only when host hardware flow control is enabled. When -RTSH is LOW, flow control is enabled for the host serial port, i.e., the host may transmit to iChip. When -RTSH is HIGH, iChip indicates that its receiver is busy and cannot receive data from host. Connect -RTSH to -CTSH when not in use.

### 3.2.3 iChip Serial Modem Signals

Signal	Type	Pin No.	Description
TXDM	O	29	Transmit Data Modem: This pin provides asynchronous serial transmit data to the modem from the modem serial port.
RXDM	I	30	Receive Data Modem: This pin provides asynchronous serial receive data from the modem to the modem serial port. When not used, this pin should be pulled up to VDDi/o.
-CTSM	I	36	Clear-to-Send Modem: -CTSM is active only when modem hardware flow control is enabled. When -CTSM is LOW, flow control is enabled for the modem serial port, i.e., iChip may transmit to the modem. When -CTSM is HIGH, iChip stops transmitting to the modem. Connect -CTSM to -RTSM when not in use.
-RTSM	O	1	Ready-to-Send Modem: -RTSM is active only when modem hardware flow control is enabled. When -RTSM is LOW, flow control is enabled for the modem serial port, i.e., the modem may transmit to iChip. When -RTSM is HIGH, iChip indicates that its receiver is busy and cannot receive data from modem. Connect -RTSM to -CTSM when not in use.
-DSRM	I	32	Data Set Ready Modem: When -DSRM is LOW, it indicates that the modem is attached and ready to communicate with iChip. Connect -DSRM to GND when not in use.
-DTRM	O	2	Data Terminal Ready Modem: When -DTRM is LOW, it indicates to the modem that iChip is attached and ready to communicate.
-CDM	I	33	Carrier Detect Modem: This pin indicates to iChip that the modem detects a carrier signal. When not used, this pin should be pulled down to GND.
-RIM	I	46	Ring Indicator Modem: this pin indicates to iChip that modem is ringing. When not used, this pin should be pulled down to GND.

## 3.2.4 iChip SPI Signals (For Future Use)

Signal	Type	Pin No.	Description
<i>SCK</i>	I/O	22	<i>Serial Clock: Clock signal used to synchronize the transfer of data across the SPI interface. The SPI is always driven by the master and received by the slave. The clock is programmable to be active high or active low. The SPI is only active during a data transfer. Any other time, it is either in its inactive state, or tri-stated.</i>
<i>MISO</i>	I/O	23	<i>Master In Slave Out: The MISO signal is a unidirectional signal used to transfer serial data from the slave to the master. When a device is a slave, serial data is output on this signal. When a device is a master, serial data is input on this signal. When a slave device is not selected, the slave drives the signal high impedance.</i>
<i>MOSI</i>	I/O	24	<i>Master Out Slave In: The MOSI signal is a unidirectional signal used to transfer serial data from the master to the slave. When a device is a master, serial data is output on this signal. When a device is a slave, serial data is input on this signal.</i>
<i>SSEL</i>	I	28	<i>Slave Select: The SPI slave select signal is an active low signal that indicates which slave is currently selected to participate in a data transfer. Each slave has its own unique slave select signal input. The SSEL must be low before data transactions begin and normally stays low for the duration of the transaction. If the SSEL signal goes high any time during a data transfer, the transfer is considered to be aborted. In this event, the slave returns to idle, and any data that was received is thrown away. There are no other indications of this exception. This signal is not directly driven by the master. It could be driven by a simple general purpose I/O under software control.</i>

### 3.2.5 iChip I2C Signals (For Future Use)

Signal	Type	Pin No.	Description
<i>SCL</i>	I/O	18	<i>Serial Clock: I2C clock input and output. The associated port pin has an open drain output in order to conform to I2C specifications. This signal must be pulled up to VCCi/o with 1KΩ resistor.</i>
<i>SDA</i>	I/O	21	<i>Serial Data :I2C data input and output. The associated port pin has an open drain output in order to conform to I2C specifications. This signal must be pulled up to VCCi/o with 1KΩ resistor.</i>



## 4 Electrical Specifications

### 4.1 Environmental Specifications

#### 4.1.1 Absolute Maximum Ratings

Parameter	Rating
VDDcore	-0.5 to +2.5 Volts
VDDi/o	-0.5 to +3.6 Volts
Vin <sup>1</sup>	-0.5 to +VDDi/o+0.5 Volts
Vin <sup>2</sup>	-0.5 to +6.0 Volts
Operating temperature	-40° to +85°C (-40° to 185° F)
Storage temperature	-40°C to 125°C (-40° to 257°F)

<sup>1</sup> For -RESIN, X1 pins.

<sup>2</sup> For all other Input pins.

Table 4-1 Environmental Specifications – Maximum Ratings

#### 4.1.2 DC Operating Characteristics

Parameter	Min	Typical	Max	Units
VDDi/o	3.0	3.3	3.6	Volts
VDDcore	1.65	1.8	1.95	Volts
X1 input, -RESIN	0		VDDcore	Volts
Vinput <sup>1</sup>	0		5.5	Volts
Voutput	0		VDDi/o	Volts
High-level Input <sup>1</sup>	2.0			Volts
Low-level Input <sup>1</sup>			0.8	Volts
High-level Output @4mA	VDDi/o-0.4			Volts
Low-level Output @4mA			0.4	Volts
Input leakage current			3	μA
Power supply current from VDDcore (Operating Mode)		20	30	mA
Power supply current from VDDcore (Sleep Mode)		10		uA
Power supply current from VDDi/o (Operating Mode)		TBD		uA
Power supply current from VDDi/o (Power Save Mode)		TBD		uA
Input Capacitance		TBD		pF

Table 4-2 DC Operating Characteristics

**Notes:** <sup>1</sup> all other pins.

## 5 Mechanical Dimensions

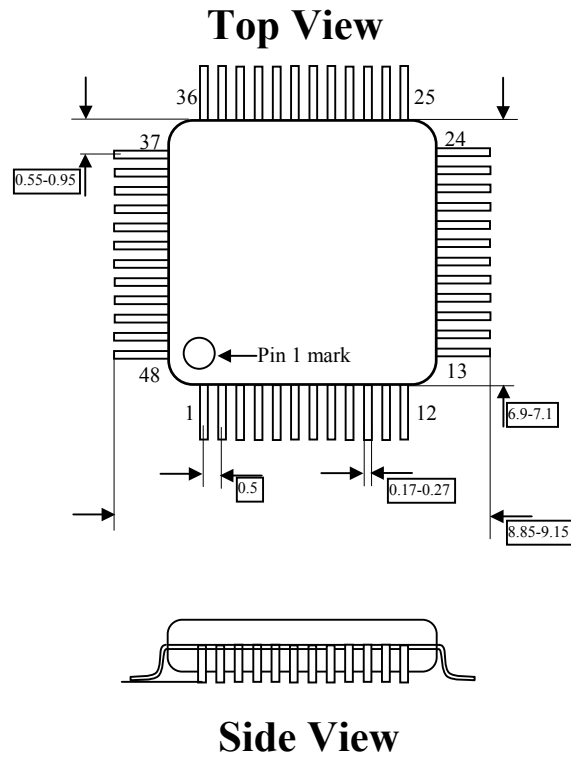


Figure 2: Mechanical Dimensions

**Note:** All measurements in millimeters.