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PATENTED: THIS PRODUCT IS COVERED BY U.S. PATENT 5,736,910



DOCUMENT / PART NO.: SI-35003-F

TITLE: 10/100BT, STACK JACK, SHIELDED

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RJ45

J1 TX+

J2 TX-

J3 RX+

J6 RX-

J4

J5

J7

J8

ELECTRICAL CHARACTERISTICS @ 25°C

OPERATING TEMPERATURE RANGE: : -40°C TO +85°C

1.0 TURNS RATIO:

(P1-P2-P3) : (J1-J2)(P4-P5-P6): (J3-J6)· 1CT · 1 +3%

2.0 INDUCTANCE:

(P6-P4) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias, -40°C TO +85°C : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias, -40°C TO +85°C (P3-P1)

3.0 LEAKAGE INDUCTANCE:

P6-P4 (WITH J6 AND J3 SHORT) P3-P1 (WITH J2 AND J1 SHORT) : 0.3uH MAX. @ 1MHz

4.0 INTERWINDING CAPACITANCE:

(P6,P5,P4) TO (J6,J3) (P3,P2,P1) TO (J2,J1)

5.0 DC RESISTANCE: (J6-J3)=(J1-J2) (P6-P4)

(P3-P1)

6.0 RETURN LOSS: 1MHz TO 30MHz

30MHz TO 80MHz

7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P2) (J3, J6) TO (P3, P6)

8.0 INSERTION LOSS: 100KHz TO 100MHz

9.0 RISE TIME: OUTPUT VOLTAGE = 1 V peak PULSE WIDTH= 112nS

10.0 CROSS TALK: 1-100 MHz

11.0 COMMON TO COMMON MODE ATTENUATION: 1MHz TO 100MHz

TITLE

PINS

TD+ P1

TCT P2

TD- P3

RD+ P4

TCT P5

RD- P6

: 1CT : 1 ±3%

: 0.3uH MAX. @ 1MHz

: 40pf MAX @ 1MHz : 40pf MAX @ 1MHz

: 1.2 ohms Max. : 0.7 ohms Max. : 0.7 ohms Max.

: 18dB MIN.

: 12dB MIN.

: 1500 Vrms

: 1500 Vrms

: 1.1 dB TYP

: 3.0 nS MAX

: 35dB TYP

: 3.0 nS MAX

: 40 dB TYP

NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

1000pF 2kV

4X 75 DHMS

SCHEMATIC

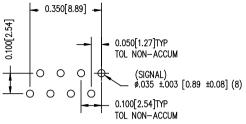
ORIGINATED BY DATE 2011-08-18 Zeng Xiao Chun DRAWN BY DATE 2011-08-18 Zhang Ru Sheng

10/100BT STACK JACK, SHIELDED **PATENTED**

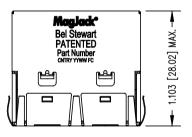
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SI-35003-F	TOL. IN INCH		UNIT : INCH [mm]	REV.: 01		
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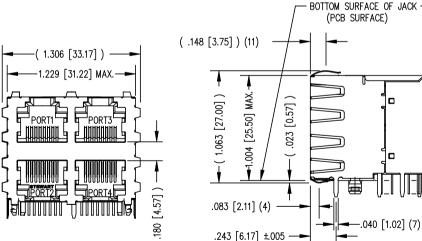


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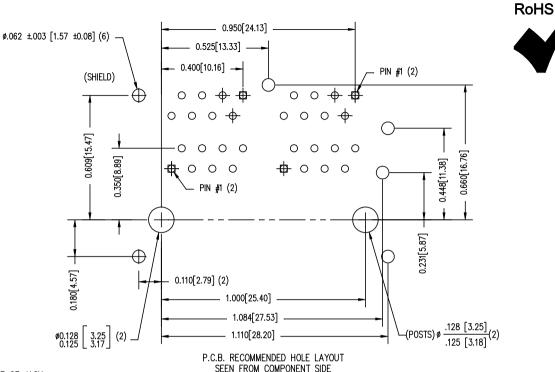


TYPICAL HOLE LAYOUT (4 POSITIONS)





TITLE



ALL CENTERLINE DIMENSIONS ARE BASIC.

NOTES:

- 1. CONNECTOR MATERIALS: HOUSING: THERMOPLASTIC UL94 V-0 CONTACT/SHIELD: COPPER ALLOY SHIELD PLATING: NICKEL OR TIN CONTACT PLATING: SELECTIVE GOLD,
 50 MICRO-INCHES MIN. IN CONTACT AREA.
- 2. PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED. SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- 3. TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- 4. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ±.005 [0.13]
- 5. WAVE SOLDER COMPATIBLE PREHEAT 125°C/90SECS.

ORIGINATED BY	DATE
Zeng Xiao Chun	2011-08-18
DRAWN BY	DATE
Zhang Ru Sheng	2011-08-18

10/100BT

STACK JACK, SHIELDED **PATENTED**

PART NO. / DRAWING NO.	STANDA	RD DIM.	[] METRIC DIM. AS REFERENCE			
SI-35003-F	TOL. IN INCH		UNIT : INCH [mm]	REV.: 01		
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SI-35003-F.DWG	.XXX	±0.005		PAGE: 3		

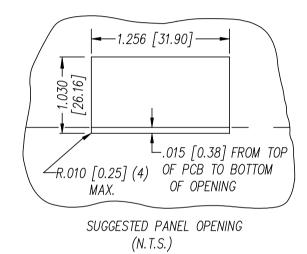


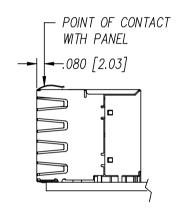
-.040 [1.02] (7) ±.005

[3.18] ±.010 [.0.25] (32)

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- 1. THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.
- 2. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ±.005 [0.13]

ORIGINATED BY	DATE	TITLE
Zeng Xiao Chun	2011-08-18	
DRAWN BY	DATE	
Zhang Ru Sheng	2011-08-18	

MagJack®
10/100BT
STACK JACK, SHIELDED
PATENTED

PART NO. / DRAWING NO.	STANDA	RD DIM.	[] METRIC DIM. AS REFERENCE			
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