AS5510

Linear Hall Sensor with I²C Output

General Description

The AS5510 is a Linear Hall Sensor with 10 bit resolution and I²C interface. It can measure absolute position of lateral movement of a simple 2-pole magnet. Depending on the magnet size, a lateral stroke of 0.5~2mm can be measured with air gaps around 1.0mm. To conserve power, the AS5510 may be switched to a power down state when it is not used. It is available in a WLCSP and SOIC8 package and qualified for an ambient temperature range from -30°C to +85°C.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5510, Linear Hall sensor with I²C output are listed below:

Figure 1:
Added Value of using AS5510

Benefits	Features
Highest reliability and durability	Contactless position measurement
Ideal for battery powered devices	Power down mode
Easy to use	Simple configuration over the I²C interface
High-resolution output	10bit resolution
Operates in wide magnetic range	Programmable sensitivity
Smallest form factor	Available in two different packages: WLCSP & SOIC8

Applications

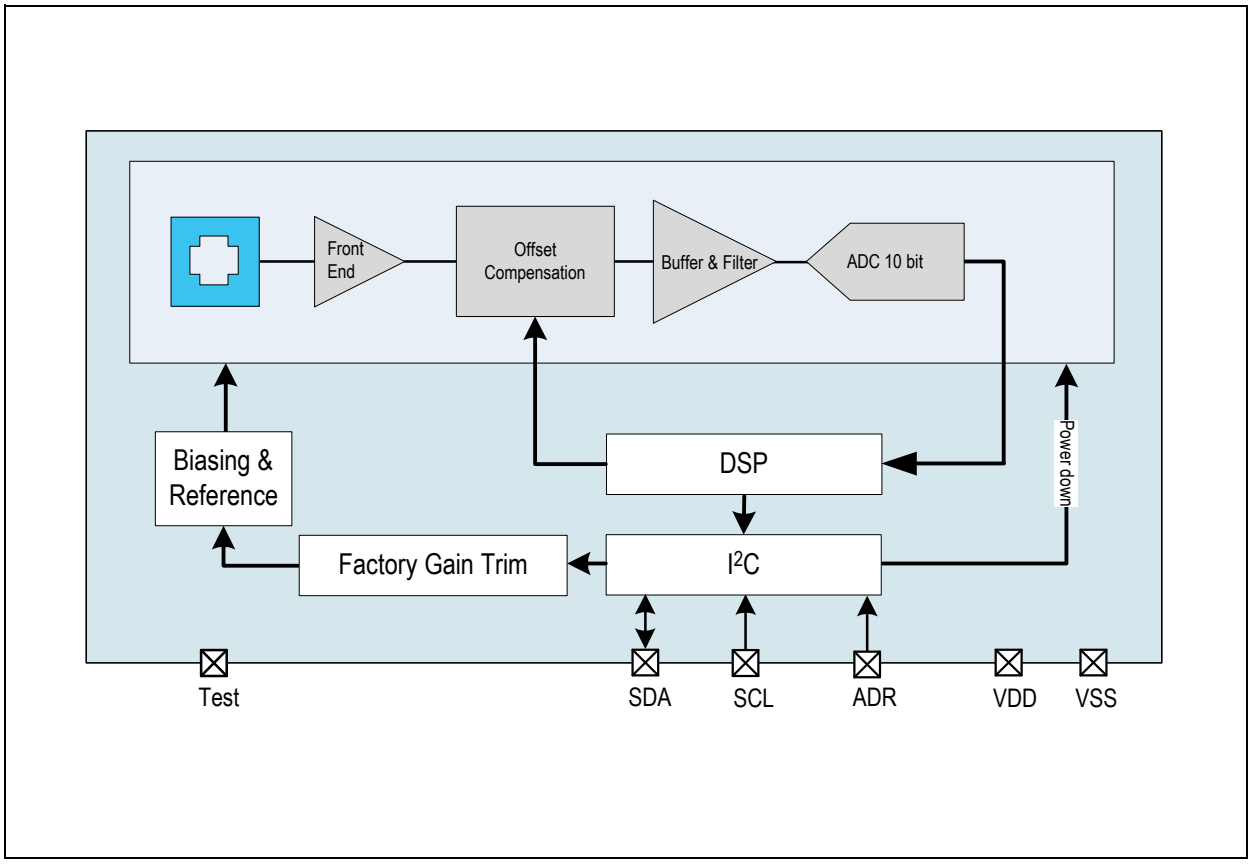
The AS5510 is ideal for:

- Position sensing
- Servo drive feedback
- Camera lens control
- Closed loop position control.

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS5510 Block Diagram

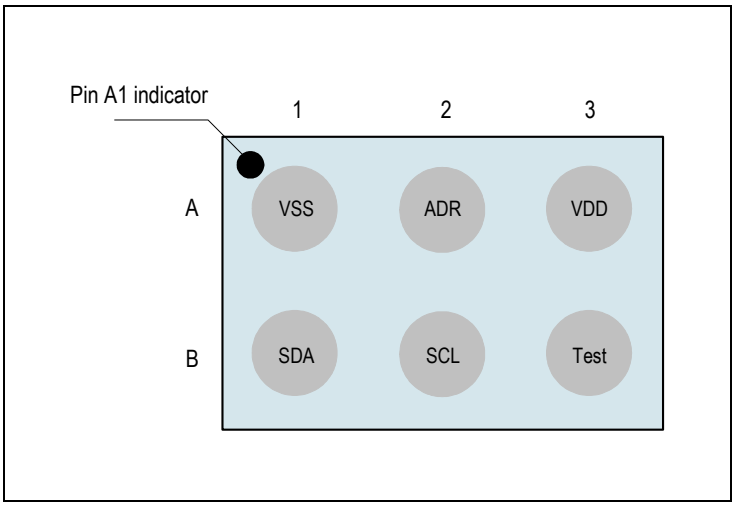


Pin Assignment

The AS5510 pin assignments are described below.

Pin Configuration of AS5510 in WLCSP Package(Top view):
The AS5510 is available in a 6-pin Chip Scale Package with a ball pitch of 400µm.

Figure 3:
Pin Diagram for WLCSP Package



Pin Configuration of AS5510 in SOIC8 Package(Top view):
Package drawing not to scale.

Figure 4:
Pin Diagram for SOIC8 Package

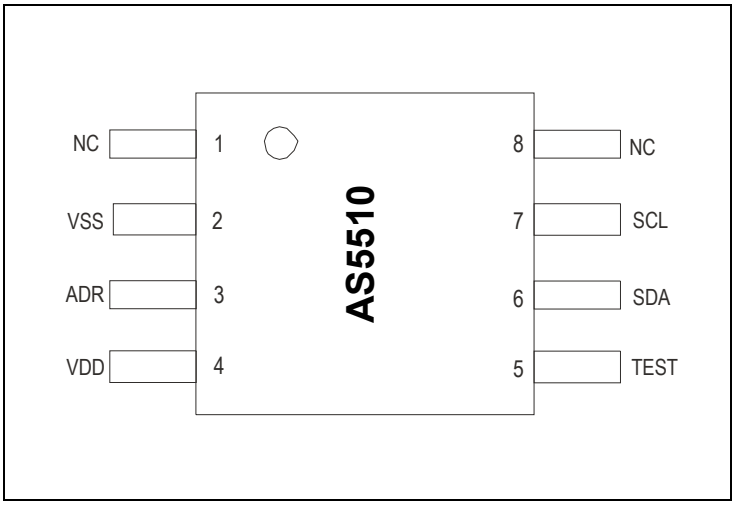


Figure 5:
Pin Description

Pin Name	Pin Number		Pin Type	Description
	WLCSP	SOIC8		
NC	-	1	-	Not Connected
VSS	A1	2	Supply pin	Negative supply pin, analog and digital ground
ADR	A2	3	Digital input	I^2C address selection pin Connect to either VSS (56h) or VDD (57h)
VDD	A3	4	Supply pin	Positive supply pin. A capacitor of 100nF should be connected to this pin and VSS
Test	B3	5	Digital input/output	Test pin, must be connected to VSS during operation
SDA	B1	6	Digital input / Digital output open drain	I^2C data I/O, 20mA driving capability
SCL	B2	7	Digital input	I^2C clock
NC	-	8	-	Not Connected

Absolute Maximum Ratings

Stresses beyond those listed in Figure 6 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in "Electrical Characteristics" on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
DC supply voltage at pin VDD	-0.3	5	V	
Input pin voltage	-0.3	VDD+0.3	V	
Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge		±2	kV	Norm: MIL 883 E method 3015
Storage temperature	-55	+125	°C	
Body temperature (Lead-free package) for WLCSP	T_{Body}	+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".
Body temperature (Lead-free package) for SOIC8		+260		
Humidity non-condensing	5	85	%	
Moisture Sensitive Level for WLCSP	1			Represents a max. floor life time of unlimited
Moisture Sensitive Level for SOIC8	3			

Electrical Characteristics

Figure 7:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD	Supply voltage at pin VDD		2.5	3	3.6	V
I_{supp}	Supply current	@ 25°C ambient temperature		3.5		mA
I_{pd}	Power down current			25		µA
T_{amb}	Ambient temperature		-30		85	°C

DC Characteristics for Digital Inputs and Outputs

CMOS Input: ADR

Operating conditions: T_{amb} = -30°C to +85°C, VDD = 2.5V to 3.6V (3V operation) unless otherwise noted.

Figure 8:
Electrical Characteristics ADR Input

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High level input voltage	0.7 * VDD		VDD	V
V_{IL}	Low level input voltage	0		0.3 * VDD	V
I_{LEAK}	Input leakage current	-1		1	µA

CMOS I²C: SDA, SCL

Operating conditions: Tamb = -30°C to +85°C, VDD = 2.5V to 3.6V (3V operation) unless otherwise noted.

Figure 9:
Electrical Characteristics I²C

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	LOW-level input voltage		-0.5	0.3 * VDD	V
V_{IH}	HIGH-level input voltage		0.7 * VDD	VDD +0.5V	V
V_{hys}	Hysteresis of Schmitt Trigger inputs	VDD > 2.5V	0.05 * VDD		V
V_{OL}	LOW-level output voltage (open-drain or open-collector) at 3mA sink current	VDD > 2.5V		0.4V	V
I_{OL}	LOW-level output current	VOL = 0.4V	20		mA
t_{of}	Output fall time from V_{IHmax} to V_{ILmax}			120 (1)	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			50 (2)	ns
I_i	Input current at each I/O pin		-10	+10 (3)	µA
C_B	Total capacitive load for each bus line			550	pF
$C_{I/O}$	I/O capacitance (SDA, SCL) (4)			10	pF

Note(s) and/or Footnote(s):

1. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
3. I/O pins of Fast-mode and Fast-mode plus devices must not obstruct the SDA and SCL lines if VDD is switched off.
4. Special purpose devices such as multiplexers and switches may exceed this capacitance due to the fact that they connect multiple paths together.

Electrical and Magnetic Specifications

Figure 10:
Electrical and Magnetic Specifications

Symbol	Parameter	Conditions	Typ	Max	Units
RES	Resolution		10		bit
Bin	Magnetic Input Range	Default Setting	±50		mT
		Configurable via I²C or factory trimming option	±25		mT
			±12.5		mT
			±18.75		mT
$Offset_{inp}$	Input related offset (1)			0.45	mT
	Linearity error (2)			3	%
t_{PwrUp}	Initial Power up time from cold start (3)	This time is needed for the first power-up of the device until the offset compensation is finished; Includes readout of the PPROM fuses		1.5	ms
t_{PwrOn}	Power-on time (4)	Time after switching from power-down mode into active mode until the offset compensation is finished	250		µs

Symbol	Parameter	Conditions	Typ	Max	Units
Fast Mode (Default setting)					
f_S	ADC sampling frequency	After offset compensation finished		50	KHz
t_{delay}	System propagation delay			20	µs
$Noise_{inp}$	Input related noise (5)	Equivalent to 8 * rms		0.8	mTpp
Slow mode (I^2C command option)					
f_S	ADC sampling frequency	After offset compensation finished		12.5	KHz
t_{delay}	System propagation delay			50	µs
$Noise_{inp}$	Input related noise (5)	Equivalent to 8 * rms		0.5	mTpp

Note(s) and/or Footnote(s):

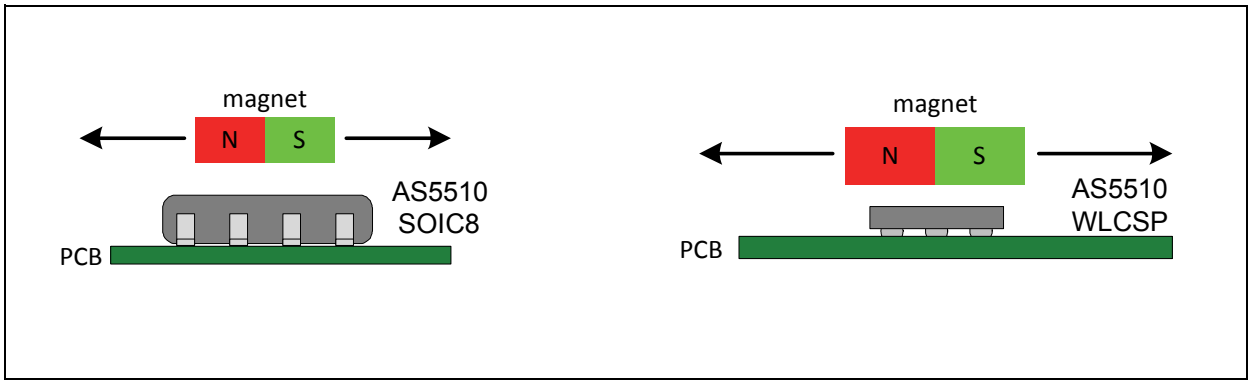
1. $Offset_{inp}$ = 0.35mT residual offset + 0.1mT earth magnetic field.

2. Linearity error = $$\text{lin_error} = 1 - \left(\frac{\text{adc_out(maxB)} - \text{adc_out(zeroB)}}{2 \times \left(\text{adc_out}\left(\frac{\text{maxB}}{2}\right) - \text{adc_out(zeroB)} \right)} \right) \times 100$$

3. This time is needed for the first power-up of the device until the offset compensation is finished; Includes readout of the PPROM fuses; It depends on the sensitivity setting.
4. Time after switching from power-down mode into active mode until the offset compensation is finished.
5. Input related Noise ($Noise_{Inp}$) is the repeatability of the measurement.

Detailed Description

Figure 11:
Linear Position Sensor AS5510 + Magnet

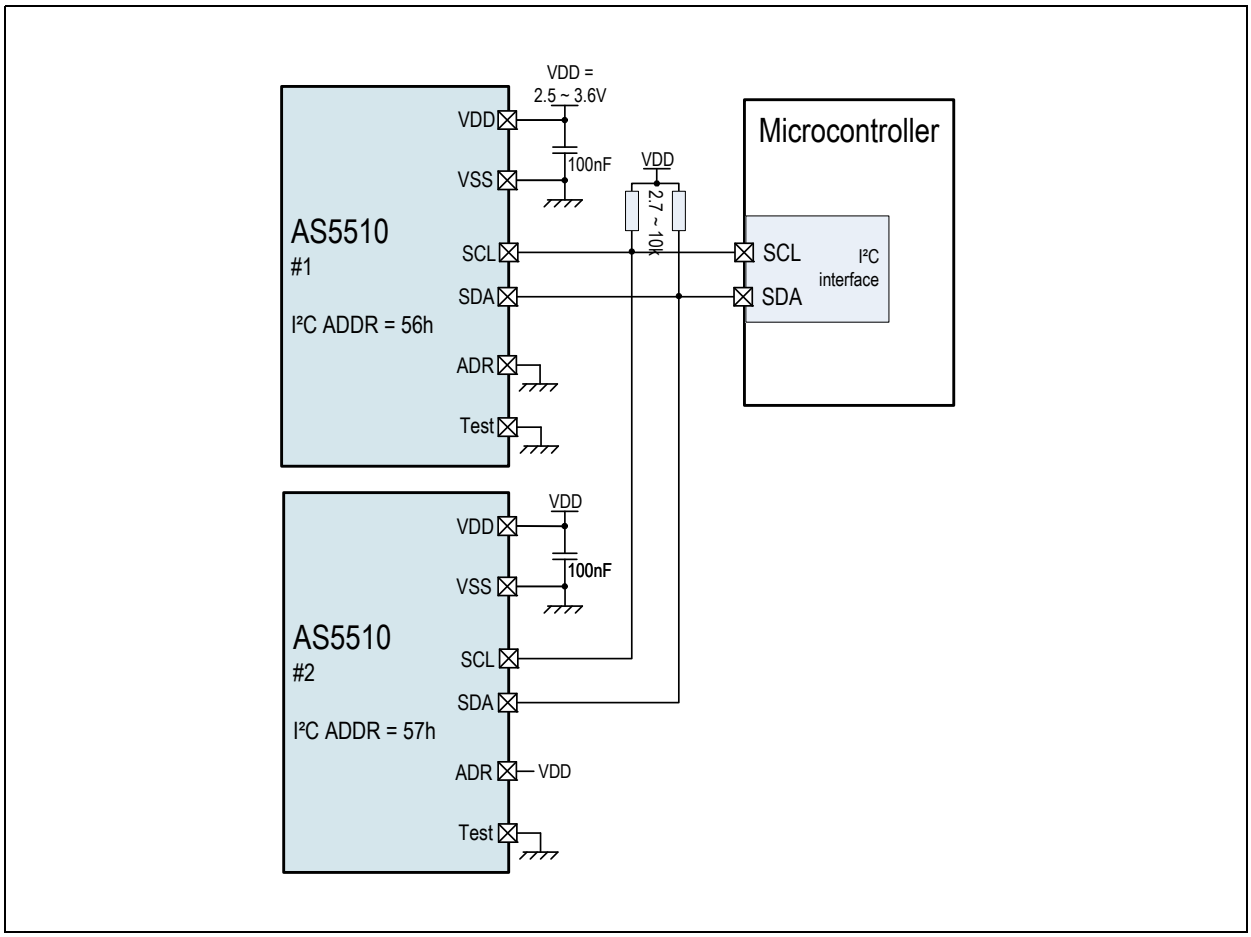


Linear Position Sensor AS5510 + Magnet: The AS5510 can measure the absolute position of lateral movement in combination with a diametrical two pole magnet.

Typical Application

The typical application circuit of AS5510 is shown below:

Figure 12:
Typical Application Circuit



I²C Interface

The AS5510 includes an I²C slave according to the NXP specification UM10204.

- 7-bit slave address **101011x**, the last address bit x is set by the ADR pin (0 or 1)
- Random/Sequential Read
- Byte/Page Write
- Fast-mode plus with 20mA SDA drive strength
- Internal hold time of 120ns for SDA signal is included (Start/Stop detection)

Not implemented:

- 10-bit Slave Address
- Clock Stretching
- General Call Address
- General Call – Software Reset
- Read of Device ID

The communication from the AS5510 includes:

- Reading the magnetic field strength in 10-bit data
- Reading the status bits

Note(s): The I²C address of the chip is selected by hardware (pin ADR). Depending on the state of this pin, the I²C address is either:

- Pin ADR = LOW → I²C address = 1010110b(56h)
- Pin ADR = HIGH → I²C address = 1010111b(57h)

I²C Interface Data

Operating conditions: Tamb = -30 to +85°C, VDD=2.5 to 3.6V (3V operation) unless otherwise noted.

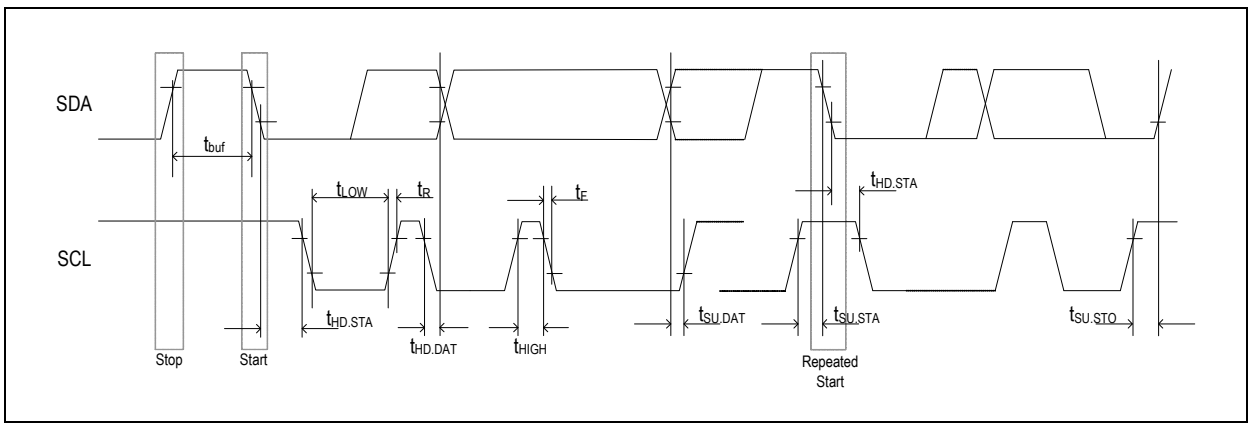
Figure 13:
I²C Timings

Symbol	Parameter	Min	Typ	Max	Units
f_{SCLK}	SCL clock frequency			1	MHz
t_{BUF}	Bus free time; time between STOP and START condition	0.5			µs
$t_{HD.STA}$	Hold time; (repeated) START condition (1)	0.26			µs
t_{LOW}	LOW period of SCL clock	0.5			µs
t_{HIGH}	HIGH period of SCL clock	0.26			µs
$t_{SU.STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD.DAT}$	Data hold time (2)			0.45	µs
$t_{SU.DAT}$	Data setup time(3)	50			ns
t_R	Rise time of SDA and SCL signals			120	ns
t_F	Fall time of SDA and SCL signals (4)			120	ns
$t_{SU.STO}$	Setup time for STOP condition	0.26			µs

Note(s) and/or Footnote(s):

1. After this time the first clock is generated.
2. A device must internally provide a hold time of at least 120ns (Fast-mode Plus) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
3. A fast-mode device can be used in standard-mode system, but the requirement $t_{SU.DAT}$ = 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + T_{SU.DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
4. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.

Figure 14:
I²C Timing Diagram



I²C Modes

The AS5510 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions must control the bus. The AS5510 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100 kHz maximum clock rate) a fast mode (400 kHz maximum clock rate) and fast mode plus (1MHz maximum clock rate) are defined. The AS5510 works in all three modes. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as start or stop signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

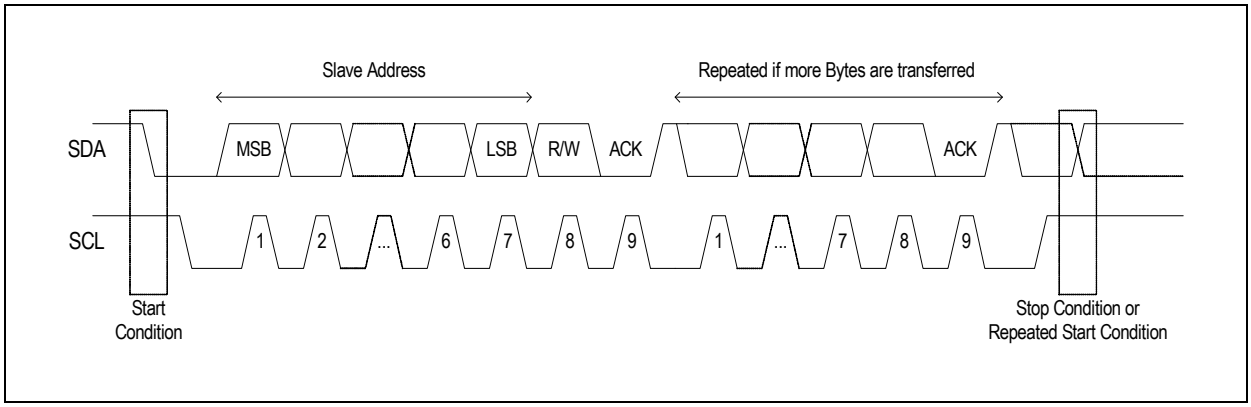
Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 15:
Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Depending upon the state of the R/W bit, two types of data transfer are possible:

Data transfer from a Master Transmitter to a Slave Receiver.

The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a “not acknowledge”. Data is transferred with the most significant bit (MSB) first.

Data transfer from a Slave Transmitter to a Master Receiver.

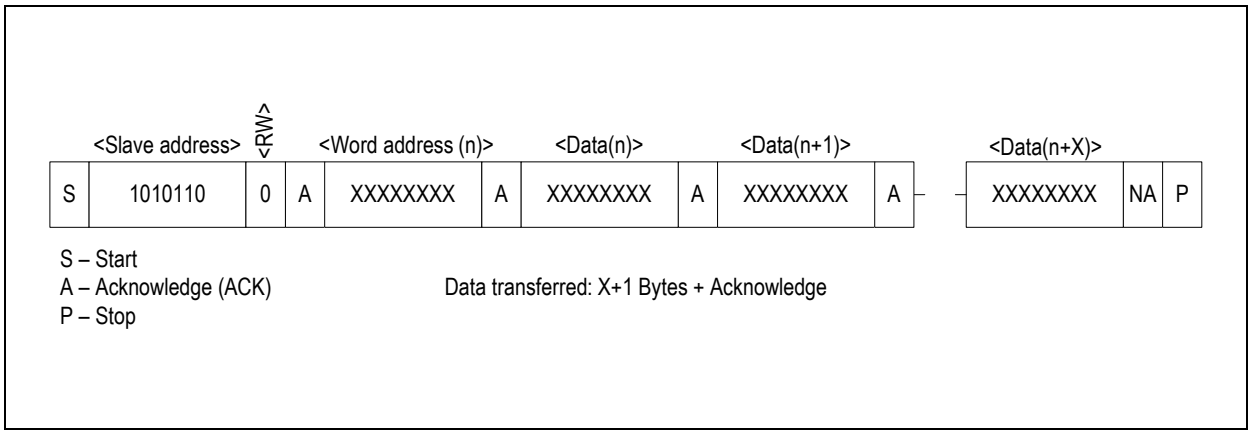
The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS5510 can operate in the following two modes:

Slave Receiver Mode (Write Mode)

Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit (or by a not acknowledge depending on the address-pointer pointing to a valid position). START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 16). The slave address byte is the first byte received after the START condition. The slave address byte contains the 7-bit AS5510 address. The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA. After the AS5510 acknowledges the slave address + write bit, the master transmits a register address to the AS5510. This sets the address pointer on the AS5510. If the address is a valid readable address the AS5510 answers by sending an acknowledge. If the address-pointer points to an invalid position a “not acknowledge” is sent. The master may then transmit zero or more bytes of data. In case of the address pointer pointing to an invalid address the received data are not stored. The address pointer will increment after each byte transferred independent from the address being valid. If the address-pointer reaches a valid position again, the AS5510 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the data write.

Figure 16:
Data Write - Slave Receiver Mode



Slave Transmitter Mode (Read Mode)

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS5510 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 17 and Figure 18). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5510 address. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS5510 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS5510 must receive a "not acknowledge" to end a read.

Figure 17:
Data Read (from Current Pointer Location) - Slave Transmitter Mode

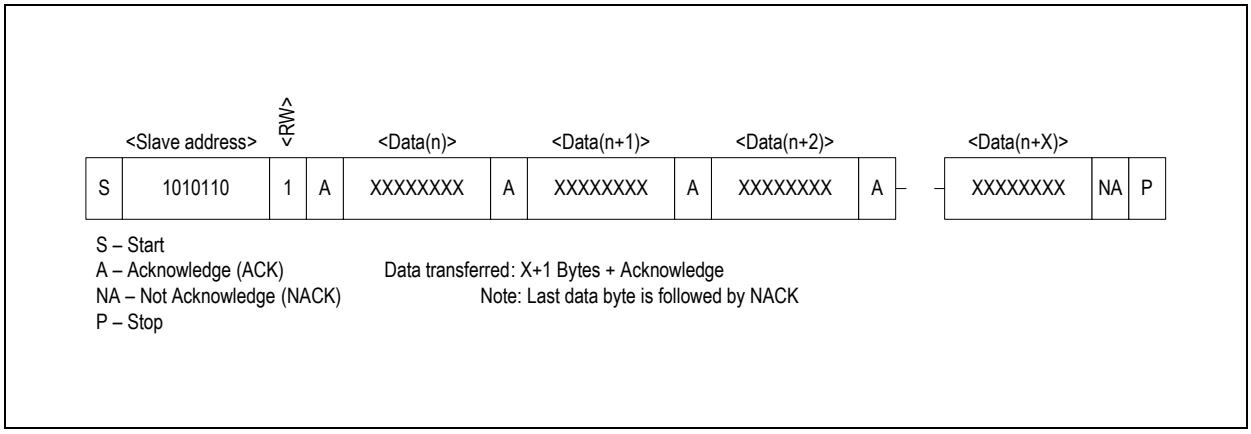
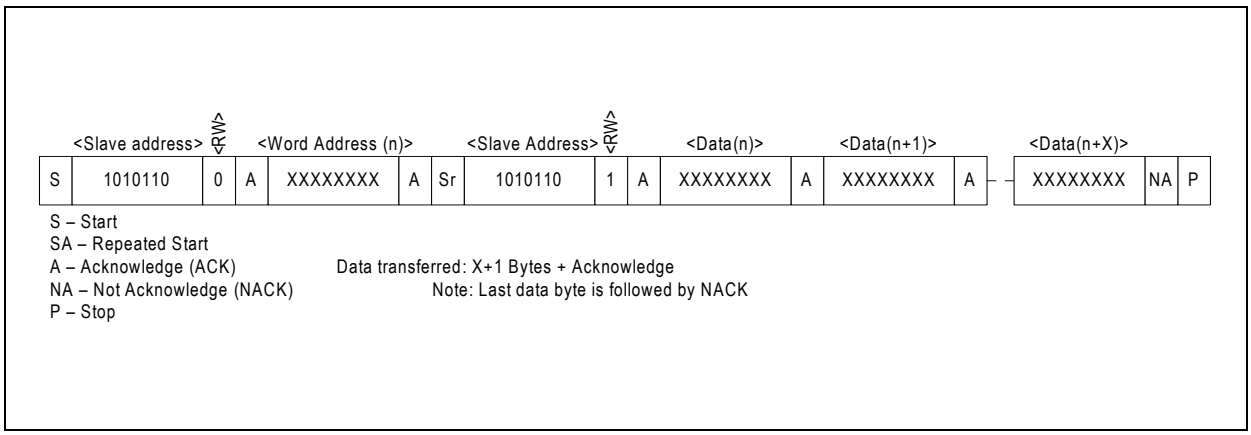


Figure 18:
Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Automatic increment of Address Pointer

The AS5510 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses

If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading

When reading from a wrong address, the AS5510 slave returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Write

A write to a wrong address is not acknowledged by the AS5510 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

SDA, SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns. Furthermore the SDA line is delayed by 120ns to provide an internal hold time for Start/Stop detection to bridge the undefined region of the falling edge of SCL. The delay needs to be smaller than tHD.STA 260ns. For Standard-mode and Fast-mode an internal hold time of 300ns is required, which is not covered by the AS5510 slave.

Register Description

Figure 19:
Register Map

Register Address	Bit								Access Type
	7	6	5	4	3	2	1	0	
00h	D7	D6	D5	D4	D3	D2	D1	D0	R
01h					OCF	Parity (even)	D9	D8	R
02h						Fast(0) Slow mode (1)	Polarity(0)	PD(0)	R/W
03h	Offs7	Offs6	Offs5	Offs4	Offs3	Offs2	Offs1	Offs0	R/W
04h							Offs9	Offs8	R/W
05h	Reserved for factory testing								R/W
06h									
07h									
0Bh							Sens 1	Sens 0	R/W

Figure 20:
Register Description

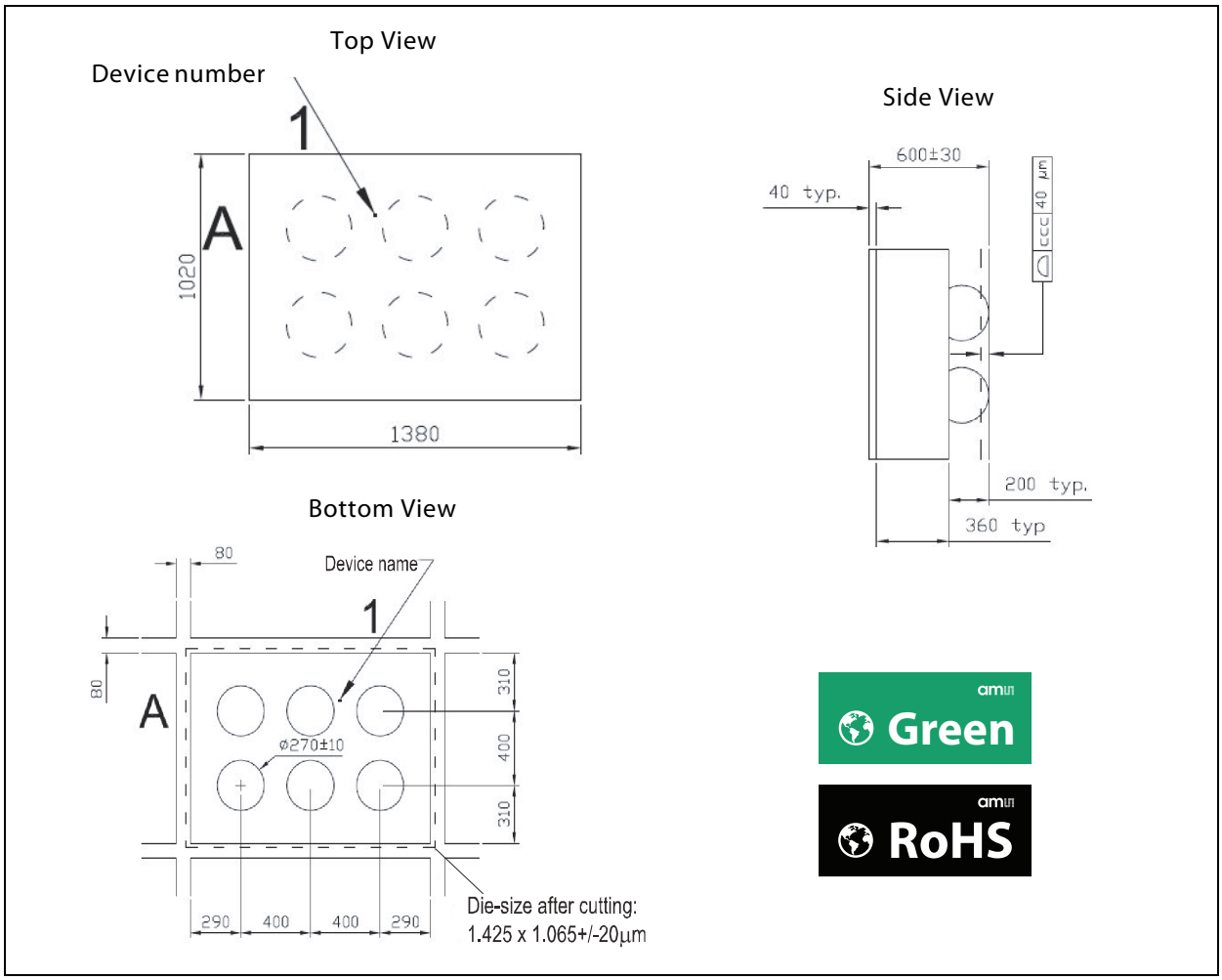
Register Address	Name	Description
00h, 01h	D9 to D0	10 Bit ADC output value that corresponds to the magnetic field input
01h	Parity	Even parity bit calculated from D9 to D0
01h	OCF	Offset compensation loop status 0 = Offset compensation loop in use 1 = Offset compensation loop has finished
02h	PD	Power down mode 0 = Normal operation (Default) 1 = Power Down mode.
02h	Polarity	Output signal polarity 0 = Normal polarity (Default) 1 = Reversed polarity (reversed magnet)
02h	Fast / Slow mode	0 = Fast mode (Default) 1 = Slow mode. Enables averaging of the output values (reduced noise, better repeatability slower sampling frequency. See Electrical and Magnetic Specifications
03h, 04h	Offs9 to Offs0	10 Bit value of the offset compensation. This register is factory trimmed
05h, 06h, 07h	Test	These registers are reserved for factory testing
0Bh	Sensitivity	Sensitivity setting 0h = Input range ± 50mT →Sensitivity = 97.66µT/LSB (Default) 1h = Input range ± 25mT →Sensitivity = 48.83µT/LSB 2h = Input range ± 12.5mT →Sensitivity = 24.41µT/LSB 3h = Input range ± 18.75mT →Sensitivity = 36.62µT/LSB

Package Drawings & Markings

WLCSP Package

The WLCSP package drawings and markings are shown below:

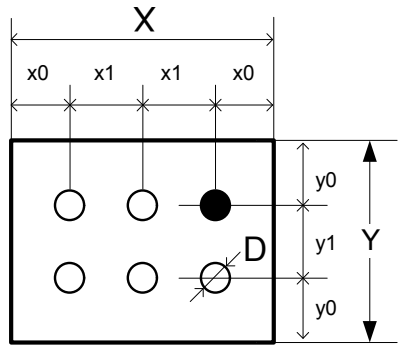
Figure 21:
Package Dimensions (WLCSP)



Note(s) and/or Footnote(s):

1. ccc Coplanarity
2. All dimensions in µm

Figure 22:
Recommended Footprint



Package Dimensions		
Symbol	**Typ**	**Unit**
X	1460	µm
x0	330	µm
x1	400	µm
Y	1100	µm
y0	350	µm
y1	400	µm
D	270	µm

Figure 23:
Markings (WLCSP)

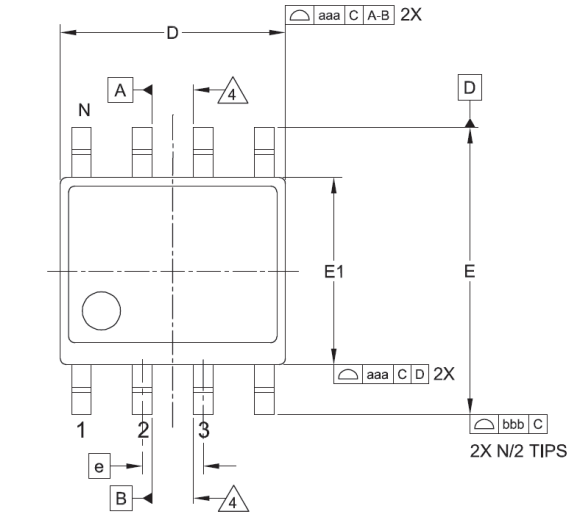
Figure 24:
Package Code XXXX

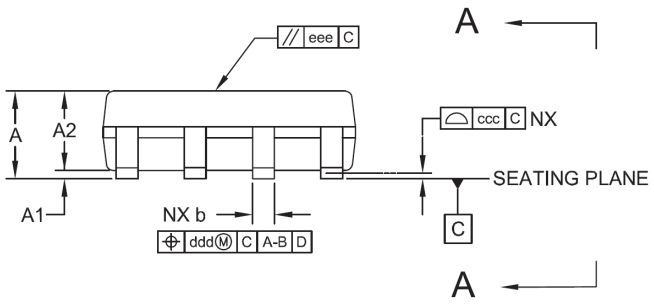
XXXX
Encoded datecode year

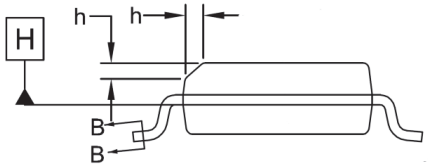
SOIC8 Package

The SOIC8 package drawings and markings are shown below:

Figure 25:
Package Dimensions SOIC8







Symbol	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	-	4.90 BSC	-
E	-	6.00 BSC	-
E1	-	3.90 BSC	-
e	-	1.27 BSC	-
L	0.40	-	1.27
L1	-	1.04 REF	-
L2	-	0.25 BSC	-
R	0.07	-	-
R1	0.07	-	-
h	0.25	-	0.50
Θ	0°	-	8°
Θ1	5°	-	15°
Θ2	0°	-	-
aaa	-	0.10	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.25	-
eee	-	0.10	-
fff	-	0.15	-
ggg	-	0.15	-
N		8	

Figure 26:
Markings (SOIC8)

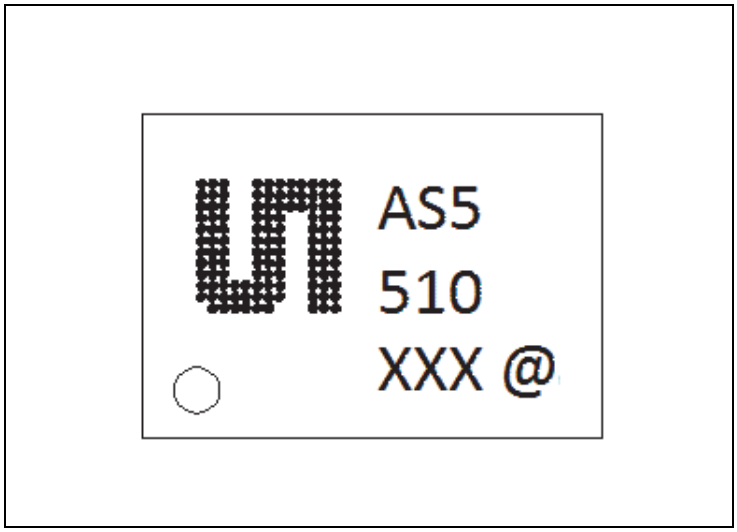


Figure 27:
Package Code

XXX	@
Encoded datecode year	Sublot Identifier

Ordering & Contact Information

The devices are available as the standard products shown in the figure below.

Figure 28:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5510-DWLT	WLCSP-6	AS5510	Tape & Reel	12.000pcs
AS5510-DSOT	SOIC-8	AS5510	Tape & Reel	2.500pcs
AS5510-DSOM	SOIC-8	AS5510	Mini Reel	500pcs

D → Temperature Range: -30°C to +85°C

WL → Package: WL-CSP Wafer Level - Chip Scale Package

SO → Package: SOIC 8

T → Delivery Form: Tape & Reel

M → Delivery Form: Mini Reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Updated Figure 27	23
Updated Figure 28	24

Note(s) and/or Footnote(s):

1. Page numbers for the previous version may differ from page numbers in the current revision

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