AS1545

Dual, 12-Bit, 1MSPS, SAR ADC

1 General Description

The AS1545 is a dual, 12-bit, 6-channel, 1 MSPS, high speed, successive approximation (SAR) analog-to-digital converters (ADCs). The AS1545 is designed to operate with a single +2.7V to +5.25V supply and a sampling rate of up to 1 MSPS.

The device contains two ADCs, each preceded by a 6-channel multiplexer and a high-bandwidth track/hold amplifier. Data access is made via standard control inputs in support of wide range of microprocessors and DSPs.

The device requires very low supply-current at the 1MSPS maximum sampling speed, and features flexible power-down modes to reduce power consumption at slower throughput rate.

The AS1545 contains an internal 2.5V reference and integrated reference buffer that can be over driven when an external reference is required.

Superior AC characteristics, low power consumption, and highly reliable packaging makes the AS1545 perfect for portable battery-powered remote sensors and data-acquisition devices.

The AS1545 is available in a 32-lead TQFN package.

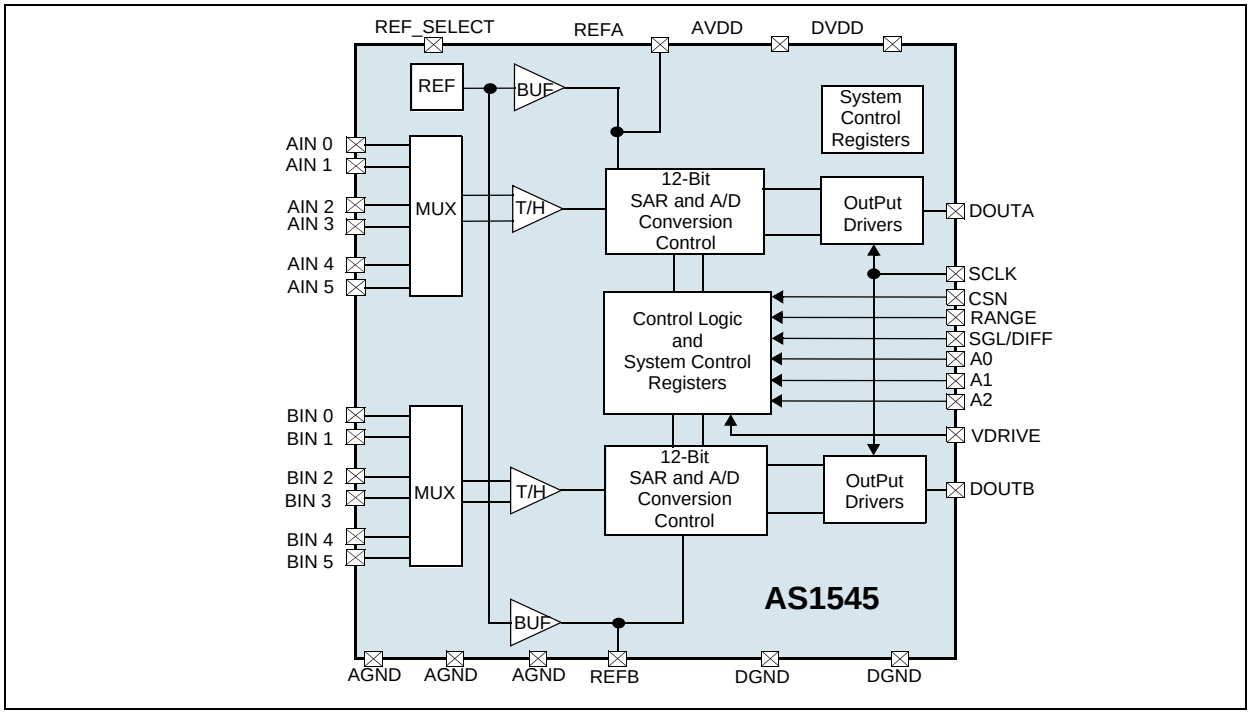
2 Key Features

- Sampling Rate: 1MSPS per ADC
- Dual 12-bit serial interface
- Software Configurable Analog Input Types:
  - 12-Channel Single-Ended
  - 6-Channel Pseudo-Differential
  - 6-Channel Fully Differential
- Internal +2.5V Reference or External: 1V to V_{DD}
- Rail to Rail Common Mode Input Range
- Low-Power Consumption
  - 15mW max. at 1MSPS with 2.7V supplies
  - 37mW max. at 1MSPS with 5.25V supplies
- Dual conversion with read at 20 MHz SCLK
- Single-Supply Operation: +2.7V to +5.25V
- Motor Control Registers: Difference of Inputs, Quadrature Signal Phases, Direction and Step Down Counter
- 32-lead TQFN Package

3 Applications

The device is ideal for motor control like encoder feed-back or current sense, motion control such as robotics, sonar, or for any other radio frequency identification.

Figure 1. AS1545 - Block Diagram



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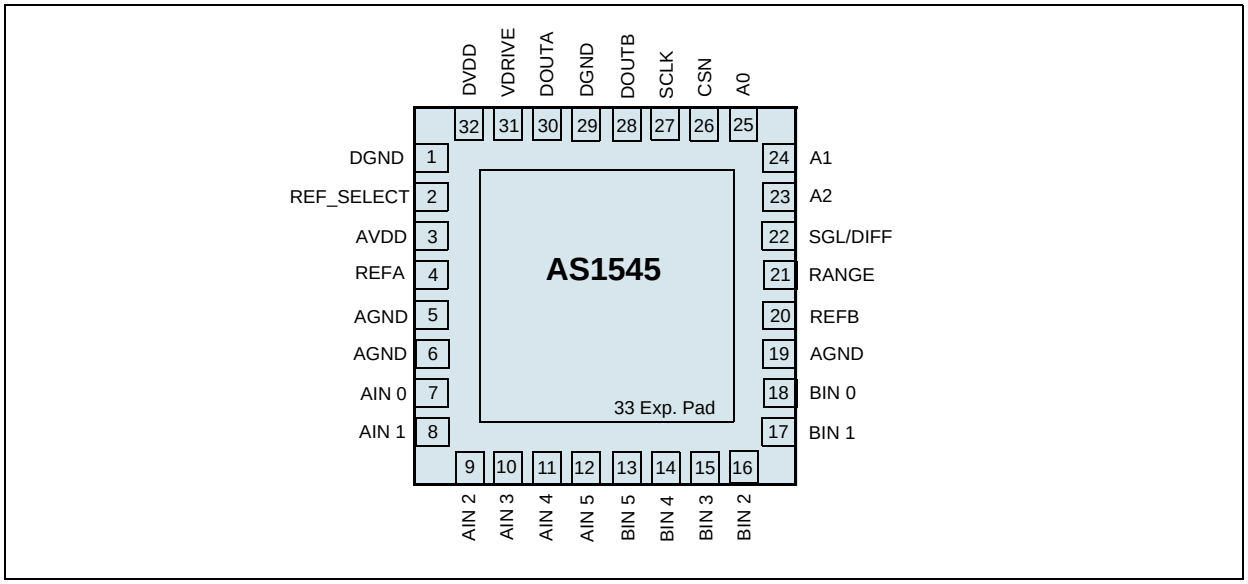
4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 1. Pin Description

Pin Number	Pin Name	Description
1, 29	DGND	**Digital Ground.** Ground reference point for the digital portion of the AS1545.
2	REF_SELECT	**Reference select pin.** Internal/External Reference Selection. Logic input. If this pin is tied to DGND, the on-chip 2.5V reference is used as the reference source for both ADC A and ADC B. In addition, Pin REFA and Pin REFB must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the AS1545 through the REF_A or REF_B pins.
3	AV_{DD}	**Analog Supply Voltage.** 2.7V to 5.25V.
4, 20	REF_A, REF_B	**Reference Input/Output.** These pins are connected to the internal reference through a series resistor and is the reference source for the AS1545. The nominal reference voltage is 2.5V and appears at the pin. This pin can be over-driven by an external reference or can be taken as high as AV_{DD}. Decoupling capacitors (4.7 uF recommended) are connected to these pins to decouple the reference buffer for each respective ADC.
5	AGND	**Analog Ground.** Decouple point for AV_{DD}. Ground reference for track/hold, reference, and DAC circuits.
6, 19	AGND	**Analog Ground.** Decouple point for V_{REF} capacitors and analog input filters. Pin 6 is the decoupling point for REFA, pin 19 for REFB. Ground reference for track/hold, reference, and DAC circuits.
7 to 12	AIN0 to AIN5	**Analog Inputs of ADC A.** These may be programmed as six single-ended channels, three pseudo-differential or three true-differential analog input channel pairs.

Table 1. Pin Description

Pin Number	Pin Name	Description
13 to 18	BIN0 to BIN5	**Analog Inputs of ADC B.** These may be programmed as six single-ended channels, three pseudo-differential or three true-differential analog input channel pairs. (see Table 5 on page 20).
21	RANGE	**Analog Input Range Selection.** Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic low, the analog input range is 0V to V_{REF}. If this pin is tied to a logic high when CSN goes low, the analog input range is 2 × V_{REF}.
22	SGL/DIFF	**Logic Input.** This pin selects whether the analog inputs are configured as differential pairs or single ended. A logic low selects differential operation while a logic high selects single-ended operation.
23 to 25	A2 to A0	**Multiplexer Select.** Logic inputs. These inputs are used to select the pair of channels to be simultaneously converted, such as Channel 1 of both ADC A and ADC B, Channel 2 of both ADC A and ADC B, and so on.
26	CSN	**Chip Select.** Active low logic input. This input provides the dual function of initiating conversions on the AS1545 and framing the serial data transfer.
27	SCLK	**Serial Clock Input.** A serial clock input provides the SCLK for accessing the data from the AS1545. This clock is also used as the clock source for the conversion process.
28, 30	D_{OUTB}, D_{OUTA}	**Serial Data Outputs.** The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input and 15 SCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of three leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If CSN is held low for 16 SCLK cycles rather than 15, then single trailing zero appears after the 12bits of data. If CSN is held low for a further 16 SCLK cycles on either D_{OUTA} or D_{OUTB}, futher data is clocked out according to the timing diagram.
31	V_{DRIVE}	**Logic Power Supply Input.** The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different than that at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3V.
32	DV_{DD}	**Digital Supply Voltage.** 2.7V to 5.25V. This is the supply voltage for all digital circuitry on the AS1545. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to DGND.
33	Exp. Pad	**Exposed Pad.** This pin can be not connected or connected AGND. The exposed pad must not be connected to V_{DD}.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{DD} to AGND	-0.3	+7	V	
DV_{DD} to DGND	-0.3	+7	V	
V_{DRIVE} to DGND	-0.3	DV_{DD}	V	
V_{DRIVE} to AGND	-0.3	AV_{DD}	V	
AV_{DD} to DV_{DD}	-0.3	+0.3	V	
AGND to DGND	-0.3	+0.3	V	
Analog Input Voltage to AGND	-0.3	AV_{DD} + 0.3	V	
Digital Input Voltage to DGND	-0.3	+7	V	
Digital Output Voltage to DGND	-0.3	V_{DRIVE} + 0.3	V	
REFA, REFB to AGND	-0.3	AV_{DD} + 0.3	V	
Input Current to All Pins Except AV_{DD} or DV_{DD}		±10	mA	
Electro-Static Discharge		2	kV	
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

AV_{DD} = DV_{DD} = 2.7V to 5.25V, V_{DRIVE} = 2.7 V to AV_{DD}/DV_{DD}, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_{AMB} = -40 to +85°C, external reference = 2.5V, RANGE = 0, Typical values at 5.25V and 25°C with external reference; Unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic Specifications 50kHz sinewave input						
SINAD	Signal to Noise + Distortion Ratio	Fully Differential Mode	70	72		dB
SNR	Signal-to-Noise Ratio		71	72.5		
THD	Total Harmonic Distortion			-81	-77	
SFDR	Spurious-Free Dynamic Range			-83	-75	
SINAD	Signal to Noise + Distortion	Single Ended or Pseudo Differential Mode	68	72		dB
SNR	Signal-to-Noise Ratio		69	72.5		
THD	Total Harmonic Distortion			-81	-73	
SFDR	Spurious-Free Dynamic Range			-83	-75	
IMD	Intermodulation Distortion	Second Order Terms		-75		dB
		Third Order Terms		-100		
	Channel-to-Channel Isolation			-90		
Sample and Hold						
	Aperture Delay				13	ns
	Aperture Jitter			30		ps
	Aperture Delay Matching				200	ps
	Full Power Bandwidth	3 dB, V_{DD} = 5V		39		MHz
		3 dB, V_{DD} = 3V		35		
		0.1 dB, V_{DD} = 5V		3.1		MHz
		0.1 dB, V_{DD} = 3V		2.9		
DC Accuracy						
	Resolution				12	Bits
	Integral Nonlinearity	Fully Differential Mode		±0.4	±0.99	LSB
		Single-Ended and Pseudo Differential Modes		±0.4	±0.99	
	Differential Nonlinearity	Differential mode		±0.25	±0.99	LSB
		Single-Ended and Pseudo Differential Modes		±0.25	±0.99	
	Straight Binary Output Coding					
	Offset Error	Single-Ended and Pseudo-Differential Mode		±0.5	±6	LSB
	Offset Error Match			±0.5		
	Gain Error			±0.75	±2.5	LSB
	Gain Error Match			±0.5		

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Twos Complement Output Coding						
	Positive Gain Error	Fully Differential Mode			±2	LSB
	Positive Gain Error Match			±0.5		
	Zero Code Error			±0.5	±5	LSB
	Zero Code Error Match			±0.5		
	Negative Gain Error				±2	LSB
	Negative Gain Error Match			±0.5		
Analog Input						
V_{INx}	Single Ended Input Voltage Ranges	Bit RANGE = 0	0		V_{REF}	V
		Bit RANGE = 1	0		$2xV_{REF}$	
V_{INx} - V_{INy}	Pseudo Differential Input Voltage Ranges	Bit RANGE = 0	V_{CM}		$V_{CM}+V_{REF}$	V
		Bit RANGE = 1	V_{CM}		$V_{CM}+2xV_{REF}$	
V_{INx} & V_{INy}	Differential Input Voltage Ranges	Bit RANGE = 0	$V_{CM}-V_{REF}/2$		$V_{CM}+V_{REF}/2$	V
		Bit RANGE = 1	$V_{CM}-V_{REF}$		$V_{CM}+V_{REF}$	
V_{CM}	Common Mode Voltage		0		V_{DD}	V
	Leakage Current				±1	µA
	Absolute Analog Input Voltage		0		V_{DD}	V
	Input Capacitance	Track Mode		15		pF
		Hold Mode		8		pF
Reference Input/Output						
REFIN	Input Voltage Range		1		V_{DD}	V
REFOUT	Output Reference Voltage		2.475	2.5	2.525	V
I_{LEAK}	Leakage Current				±1	µA
	Input Capacitance			30		pF
	REFA, REFB Output Impedance			5		Ω
REFOUT TEMPCO	Reference Temperature Coefficient			30		ppm/ºC
Logic Inputs						
V_{IH}	Input High Voltage	V_{DD} < 5V	0.7x V_{DRIVE}			V
		V_{DD} > 5V	2.8			
V_{IL}	Input Low Voltage				0.4	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{DRIVE}	-1		+1	µA
C_{IN}	Input Capacitance			5		pF
Logic Outputs						
V_{OH}	Output High Voltage	I_{SOURCE} = 200µA	V_{DRIVE} - 0.2			V
VOL	Output Low Voltage	I_{SINK} = 200µA			0.4	V

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Floating State Leakage Current	D_{OUT} = GND or V_{DD}			±1	µA
	Floating State Output Capacitance			7		pF
	Output Coding	Straight binary (Single-Ended & Pseudo-Differential)				
		Two's complement (Fully Differential)				
Conversion Rate						
t_{CONV}	Conversion Time	Exclusive of t_{ACQ}			$15t_{SCLK}$	
t_{ACQ}	Track/Hold Acquisition Time	Full-scale step input; V_{DD} = 5V			90	ns
		Full-scale step input; V_{DD} = 3V			110	
	Throughput Rate				1	MSPS
Power Requirements						
V_{DD}	Positive Supply Voltage	AV_{DD} = DV_{DD}	2.7		5.25	V
V_{DRIVE}	Interface Supply Voltage		2.7		AV_{DD}/ DV_{DD}	V
I_{DDA}+I_{DDD}	Normal Mode (Static)	V_{DD} = 5.25V, internal Ref. on		4	5	mA
	Operational, f_S = 1 MSPS	V_{DD} = 5.25V, internal Ref. on		6.5	7	mA
		V_{DD} = 2.7V, internal Ref. on		5.2	5.5	mA
	Partial Power-Down Mode	V_{DD} = 5.25V, internal Ref. on, Static			500	µA
	Full Power-Down Mode				1	µA
P_D	Operational, f_S = 1 MSPS	V_{DD} = 5.25V, internal Ref. on			36.75	mW
	Partial Power-Down	V_{DD} = 5.25V, internal Ref. on			2.6	mW
	Full Power-Down				5.25	µW

Timing Characteristics

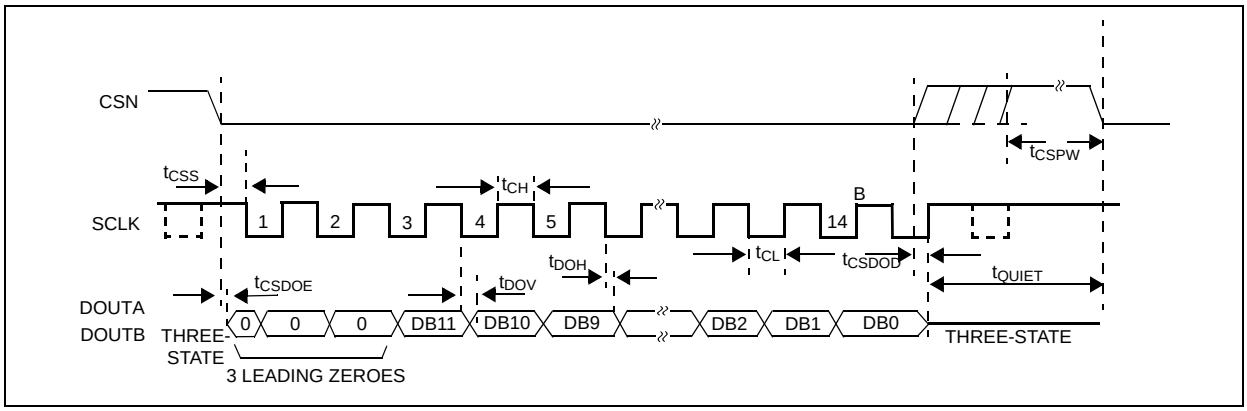
AV_{DD} = DV_{DD} = 2.7V to 5.25V, V_{DRIVE} = 2.7V to AV_{DD}/DV_{DD}, internal/external reference = 2.5V, T_A = -40 to +85°C (unless otherwise specified).

Table 4. Timing Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Master Clock Frequency	f_{SCLK}		1		20	MHz
Conversion Time	$t_{CONVERT}$	$t_{SCLK} = 1/f_{SCLK}$			15 x t_{SCLK}	ns
		f_{SCLK} = 20 MHz			750	
Quiet Time	t_{QUIET}	Minimum time between end of serial read and next falling edge of CSN	30			ns
CSN Fall to SCLK Fall Setup Time	t_{CSS}	V_{IL} of CSN to V_{IL} of SCLK	10			ns
CSN Fall to D_{OUT} Enable	t_{CSDOE}	V_{IL} of CSN to Corner of D_{OUT}			15	ns
SCLK Fall to D_{OUT} Valid[2]	t_{DOV}	V_{DD} = 2.7V			40	ns
		V_{DD} = 5.25V			10	
SCLK Fall to D_{OUT} Hold[3]	t_{DOH}	V_{DD} = 2.7V	10			ns
		V_{DD} = 5.25V	5			
SCLK Low Pulse Width	t_{CL}	V_{IL} to V_{IL} of SCLK	0.4 t_{SCLK}		0.6 t_{SCLK}	
SCLK High Pulse Width	t_{CH}	V_{IH} to V_{IH} of SCLK	0.4 t_{SCLK}		0.6 t_{SCLK}	
CSN Rise to D_{OUT} Disable	t_{CSDOD}	V_{IH} of CSN to corner of D_{OUT} to Tristate			20	ns
CSN Minimum Pulse Width	t_{CSPW}	V_{IH} to V_{IH} of CSN	30			ns
SCLK Fall to D_{OUT} Disable	t_{DOD}	V_{IH} of SCLK to corner of D_{OUT} to Tristate	5		50	ns

1. Based on simulation and characterised samples.
2. V_{IL} of SCLK to V_{OH} of D_{OUT} (rising edge) / V_{OL} of D_{OUT} (falling edge)
3. V_{IL} of SCLK to V_{OL} of D_{OUT} (rising edge) / V_{OH} of D_{OUT} (falling edge)

Figure 3. Timing Diagram



7 Typical Operating Characteristics

V_{DD} = 5.25V, V_{REF} = 2.5V, f_{SCLK} = 20MHz (50% duty), f_{SAMPLE} = 1MSPS, C_{REF} = 4.7µF, RANGE = 0, SGL/DIFF = 1, T_{AMB} = +25ºC (unless otherwise specified).

Figure 4. Integral Nonlinearity vs. Digital Output Code;

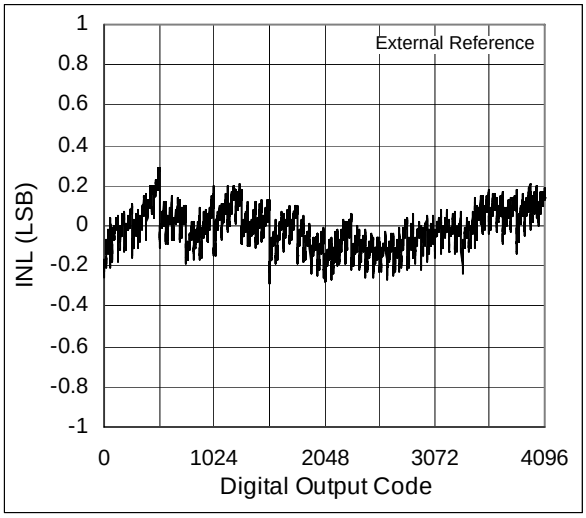


Figure 5. Diff. Nonlinearity vs. Digital Output Code;

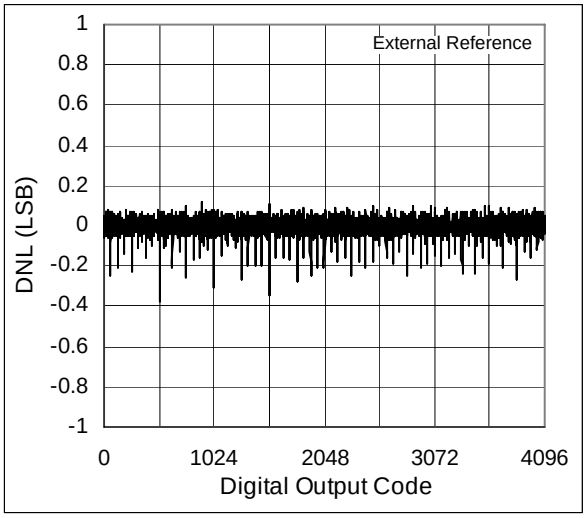


Figure 6. Integral Nonlinearity vs. Digital Output Code;

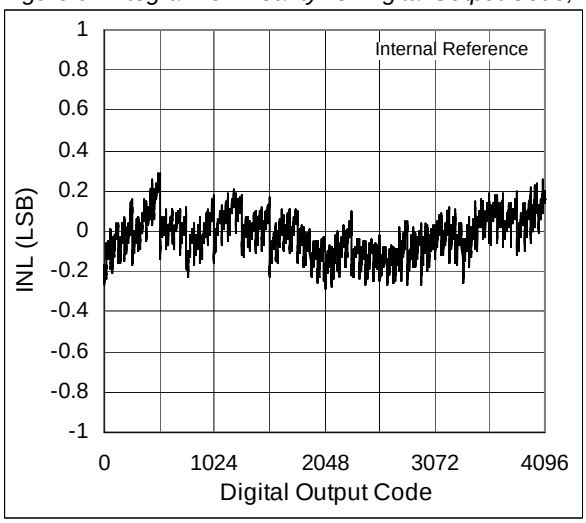


Figure 7. Diff. Nonlinearity vs. Digital Output Code;

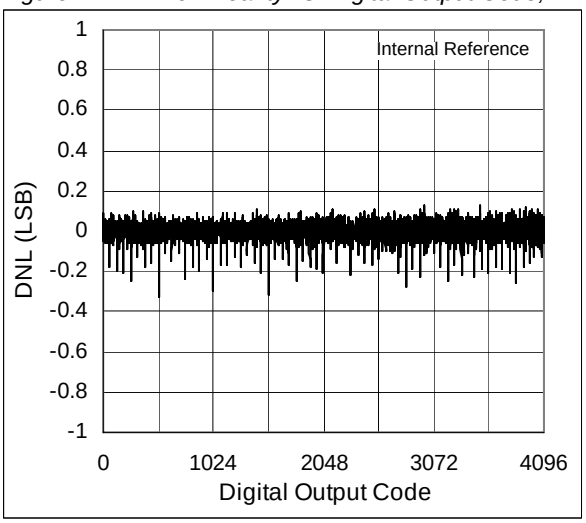


Figure 8. FFT @ 50kHz, External Reference;

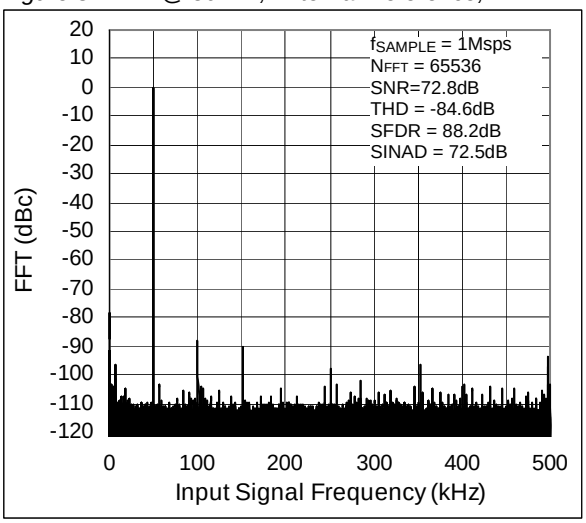


Figure 9. FFT @ 50kHz, Internal Reference;

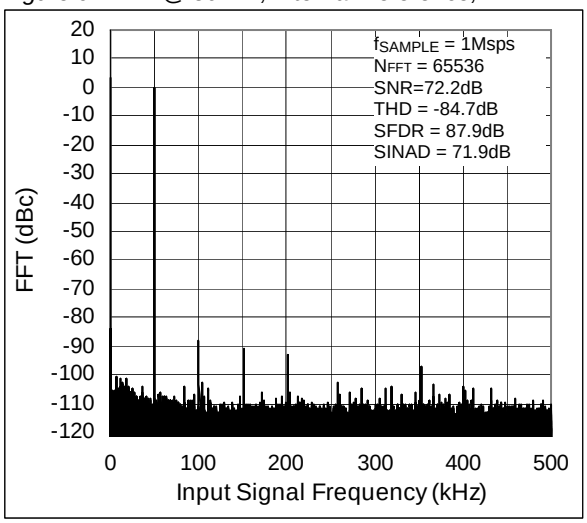


Figure 10. Supply Current vs. Sampling Rate;

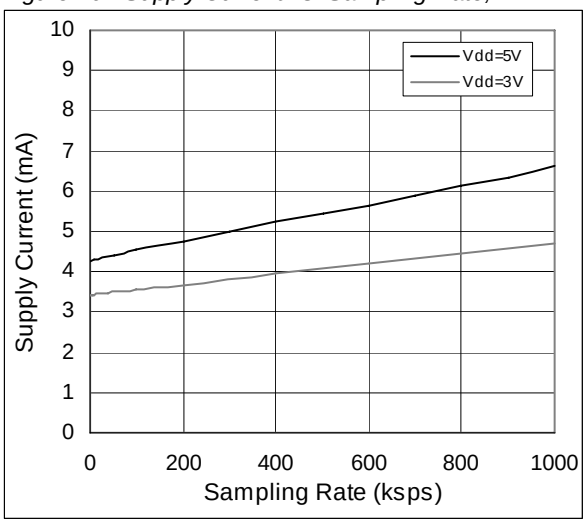


Figure 11. Supply Current vs. Supply Voltage;

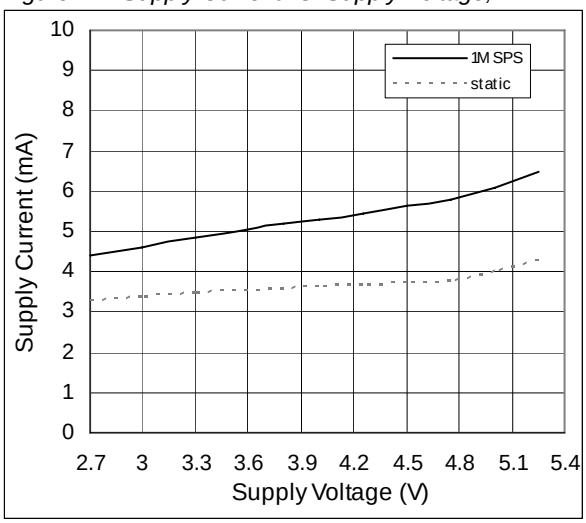


Figure 12. Supply Current vs. Temperature;

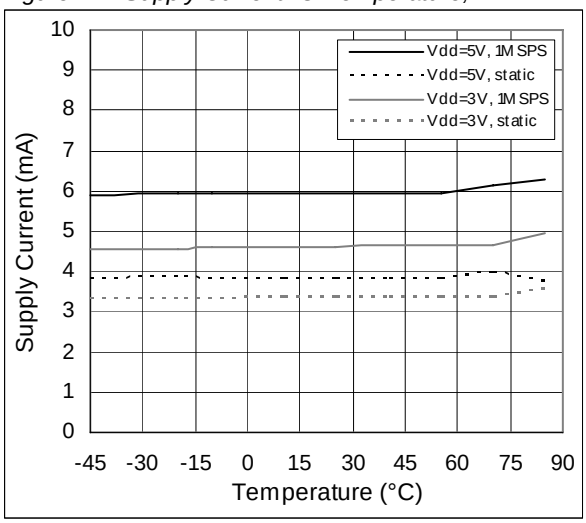


Figure 13. Full Power-Down Current vs. V_{IN};

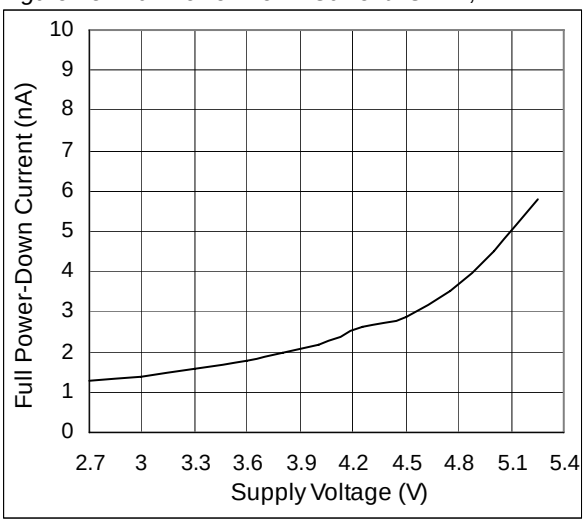


Figure 14. Full Power-Down Current vs. Temperature;

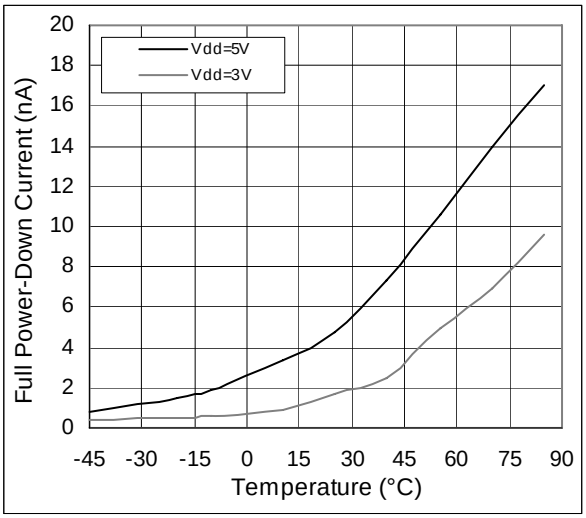


Figure 15. Partitial Power-Down Current vs. Temp.;

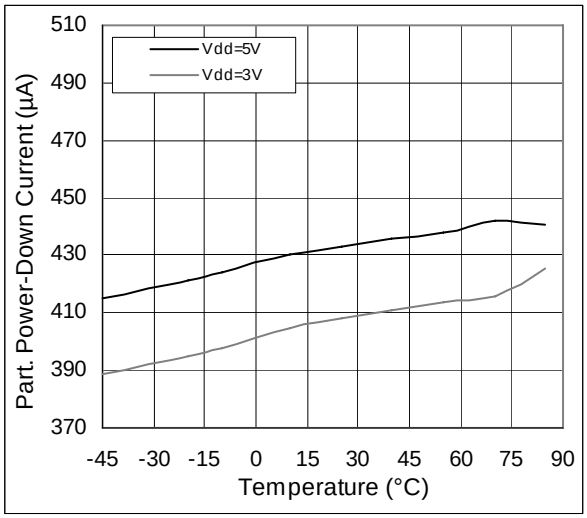


Figure 16. Part. Power-Down vs. Temperature;

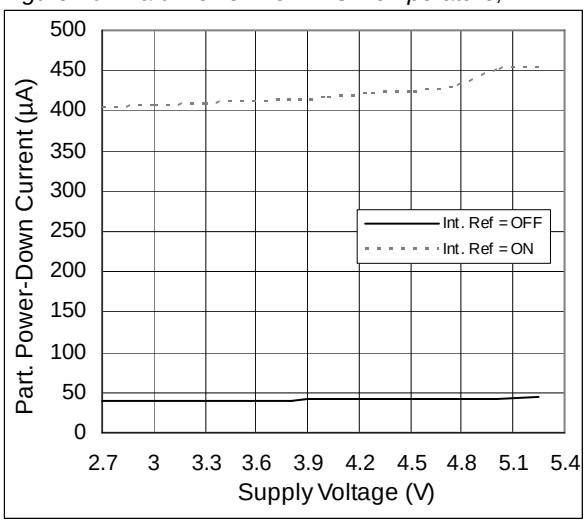


Figure 17. Dynamic Performance vs. Supply Voltage;

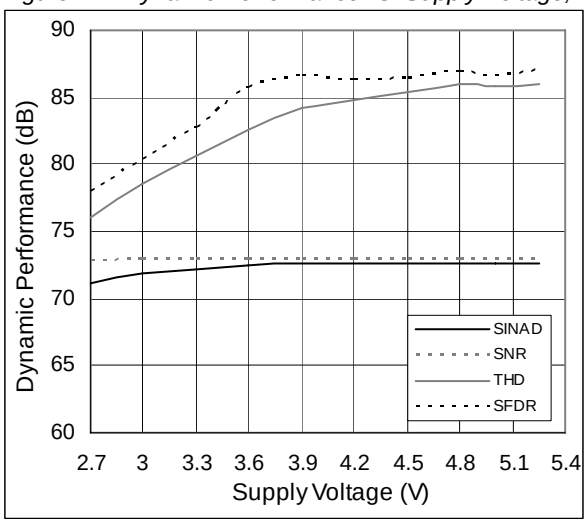


Figure 18. Gain & Offset Error vs. Supply Voltage;

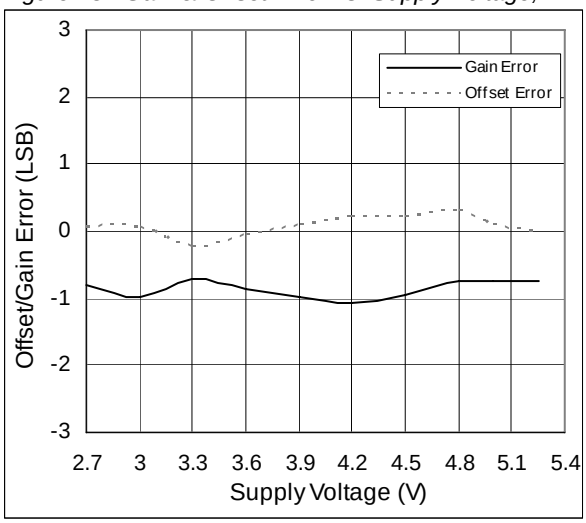


Figure 19. SINAD vs. Input Frequency, Single-Ended;

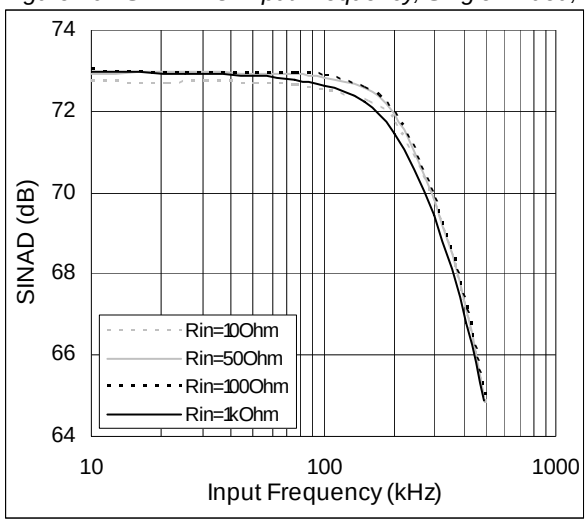


Figure 20. SINAD vs. Input Frequency, Single-Ended;

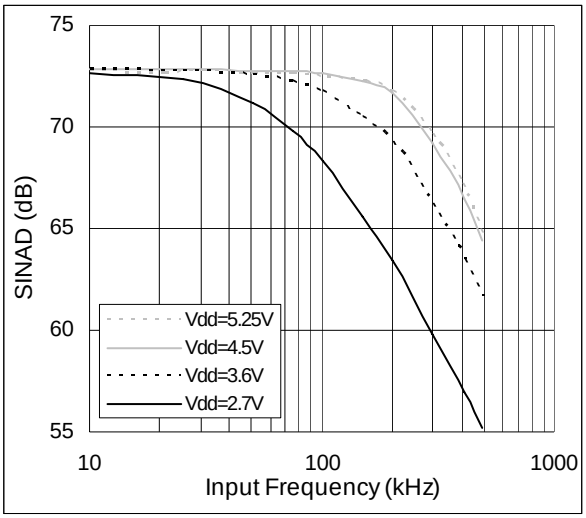


Figure 21. SINAD vs. Input Frequency, Differential;

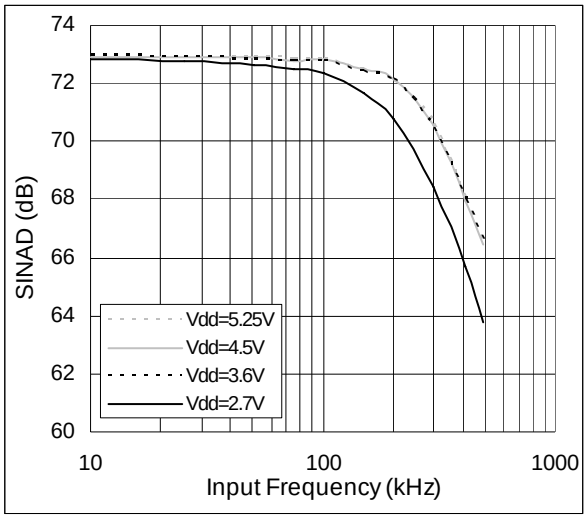


Figure 22. ENOB vs. ReferenceVoltage;

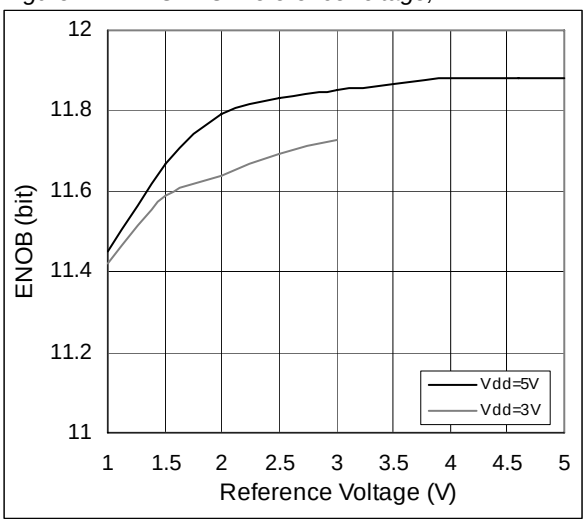


Figure 23. THD vs. Input Frequency, Single-Ended;

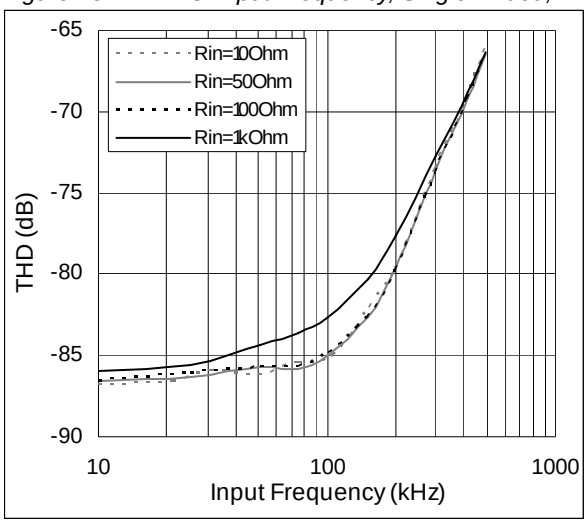


Figure 24. THD vs. Input Frequency, Single-Ended;

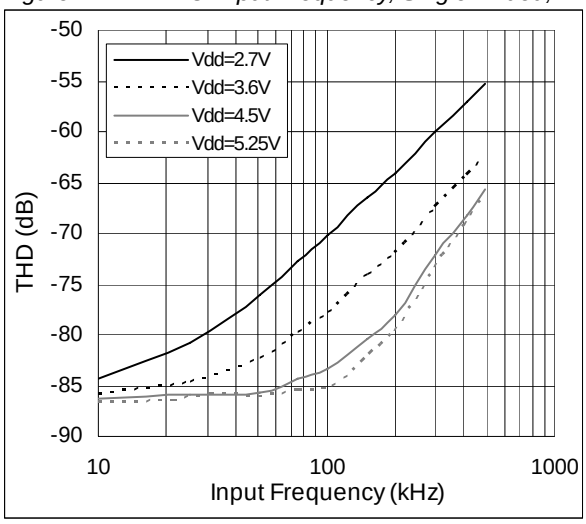


Figure 25. THD vs Input Frequency, Differential;

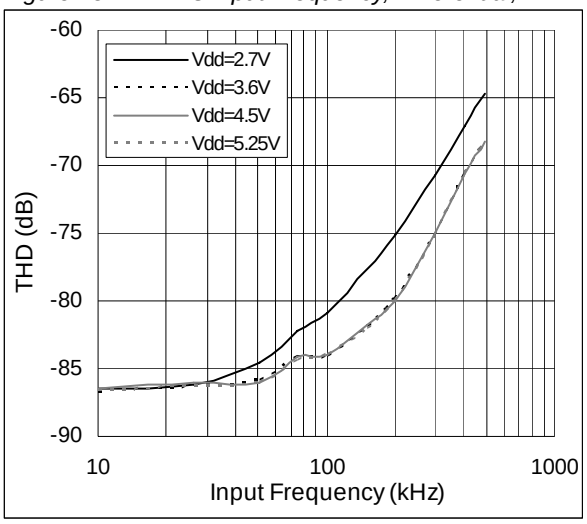


Figure 26. ENOB vs. Input Frequency, Single-Ended;

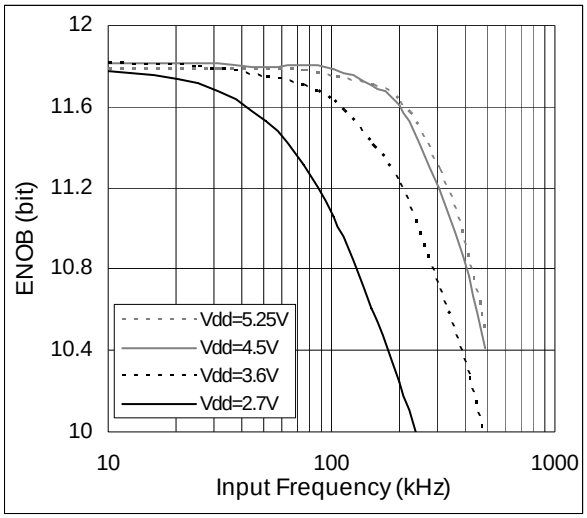


Figure 27. ENOB vs. Input Frequency, Differential;

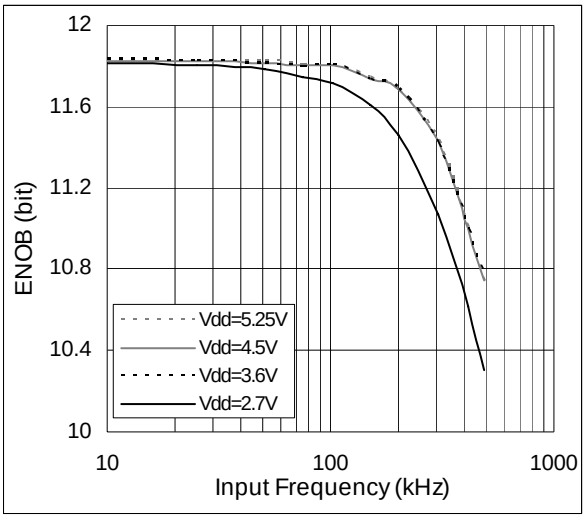


Figure 28. SNR vs. Input Frequency, Single-Ended;

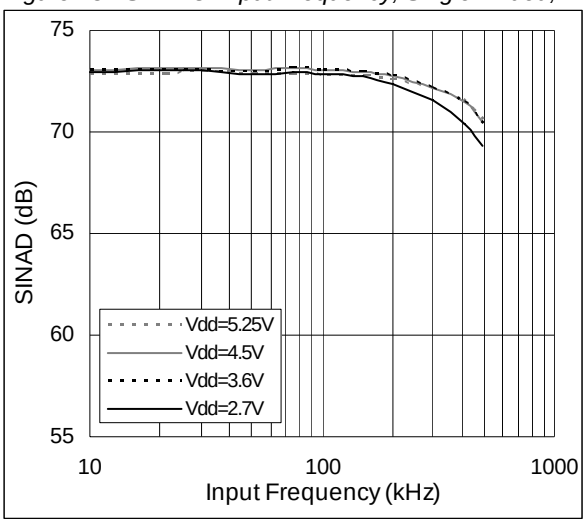


Figure 29. SNR vs. Input Frequency, Differential;

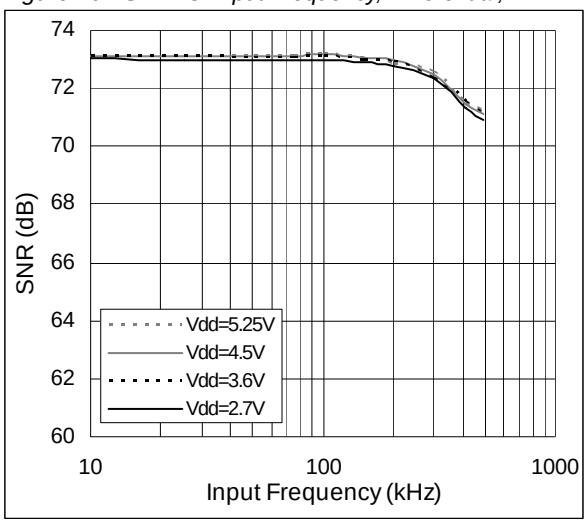


Figure 30. INL/DNL vs. Reference Voltage, V_{DD} = 3V;

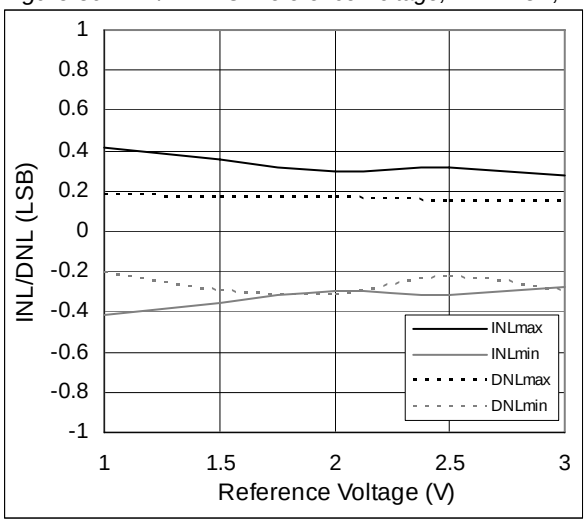
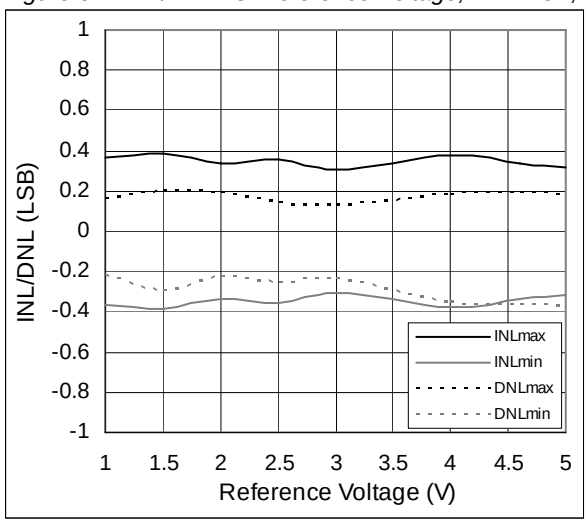


Figure 31. INL/DNL vs. Reference Voltage, V_{DD} = 5V;



8 Terminology

Acquisition Time

The Acquisition time is the time needed by the ADC to accurately acquire the analog input voltage in the internal sampling capacitor. During this time the ADC is in track mode.

Conversion Time

The Conversion Time is the time that the ADC needs to convert an acquired analog input into a corresponding digital code. A Successive Approximation Register ADC usually needs a number of clocks dependant on the resolution. During this time the ADC is in hold mode.

Throughput / Sample Rate

The Throughput or Sample Rate is the number of conversions performed by an ADC per second. It is usually specified in Samples Per Second (SPS). The Throughput or Sample Rate is the reciprocal of the sum of Acquisition Time and Conversion Time.

Aperture Delay

The Aperture Delay defines the time between the falling edge of CSN and the actual Sampling Instant. The Aperture Delay Matching defines the maximum deviation of Aperture Delays across all 6 channels of one ADC.

Aperture Jitter

The Aperture Jitter is the deviation of the actual Sampling Instant. This deviation is totally random and the standard deviation of the distribution is calculated with one sigma.

Differential Nonlinearity (DNL)

The Differential Nonlinearity is the deviation between the actual code widths to the ideal code widths of 1 LSB, comparing all contiguous codes in the ADC. The ADC is specified according to its maximum and minimum DNL values across all codes. A DNL value equal to -1 indicates a missing code in the transfer function.

Integral Nonlinearity (INL)

The Integral Nonlinearity measures the deviation from the actual transfer function to the best straight line that minimizes the INL worst case values.

Offset Error

The Offset Error defines the absolute deviation of the first code transition (0x000h) to (0x001h) from the ideal input voltage (AGND + 0.5 LSB) in Single Ended and Pseudo Differential Mode (binary output coding).

Offset Error = $\left[\frac{VIN}{VREF} \times 4096\right] - AVG(MeasuredCodes)$

Offset Error Match

The Offset Error Match defines the maximum deviation of the Offset Errors across all 6 channels of V_{IN} in Single Ended and Pseudo Differential Mode (binary output coding).

Gain Error

The Gain Error defines the absolute deviation of the last code transition (0xFFEh) to (0xFFFh) from the ideal input voltage (V_{REF} – 1.5 LSB) in Single Ended and Pseudo Differential Mode. The Offset Error is compensated.

Gain Error = $OffsetError - \left[AVG(MeasuredCodes) - \frac{VIN}{VREF} \times 4096\right]$

Gain Error Match

The Gain Error Match defines the maximum deviation of the Gain Errors across all 6 channels of V_{IN} in Single Ended and Pseudo Differential Mode (binary output coding).

Zero Code Error

The Zero Code Error is the deviation of the midscale transition (all 0xFFFh to all 0x000h in 2's complement output coding) from the ideal input voltage (V_{IN+} - V_{IN-} = 0V) in Fully Differential Mode.

$$\text{Zero Code Error} = \left[\frac{VINP - VINN}{VREF} \times 4096 + 2048\right] - AVG(MeasuredCodes)$$

Zero Code Error Match

The Zero Code Error Match defines the maximum deviation of the Zero Code Errors across all 6 channels of V_{IN} in Fully Differential Mode (2's complement output coding).

Positive Gain Error

The Positive Gain Error is the deviation last code transition (0x7FEh) to (0x7FFh) in 2's complement output coding from the ideal input voltage (V_{IN+} - V_{IN-} = +V_{REF} - 0.5LSB @ Range=1 and +V_{REF}/2 - 0.5LSB @ Range=0) in Fully Differential Mode.

$$\text{Positive Gain Error} = \text{Zero Code Error} - \left\{\left[\frac{VINP - VINN}{VREF} \times 4096 + 2048\right] - AVG(MeasuredCodes)\right\}$$

Negative Gain Error

The Negative Gain Error is the deviation first code transition (0x800h) to (0xFFFh) in 2's complement output coding from the ideal input voltage (V_{IN+} - V_{IN-} = -V_{REF} + 0.5LSB @ Range=1 and -V_{REF}/2 + 0.5LSB @ Range=0) in Fully Differential Mode.

$$\text{Negative Gain Error} = \left\{\left[\frac{VINP - VINN}{VREF} \times 4096 + 2048\right] - AVG(MeasuredCodes)\right\} - ZeroCodeError$$

Positive / Negative Gain Error Match

The Positive / Negative Gain Error Match defines the maximum deviation of the Positive / Negative Gain Errors across all 6 channels of V_{IN} in Fully Differential Mode (2's complement output coding).

Signal-to-Noise Plus Distortion (SINAD)

The Signal to Noise Plus Distortion Ratio defines the ratio between the RMS value of the fundamental (input signal) and the equivalent RMS value of all other spectral components below one-half the sampling frequency, including harmonics but excluding DC. SINAD will be equal to SNR in an distortion free ADC.

Effective Number of Bits (ENOB)

The Effective Number of Bits indicates the actual resolution of the converter. The ENOB can be calculated from the Signal to Noise Plus Distortion Ratio (SINAD).

$$\text{ENOB} = \frac{SINAD - 1{,}76}{6{,}02}$$

Signal-to-Noise Ratio (SNR)

The Signal to Noise Ratio defines the ratio between the RMS value of the fundamental (input signal) to the RMS value of the sum of all other spectral components below one-half of the sampling frequency, excluding harmonics and DC.

The theoretical SNR for an ideal N bit ADC is limited by the quantization error and is described by the formula:

SNR = 6.02*N +1.76 (dB)

Therefore, for a 12-bit ADC, the maximum SNR is 74dB.

Total Harmonic Distortion (THD)

The Total Harmonic Distortion is the ratio between the RMS value of the fundamental (input signal) to the RMS value of the first five harmonics.

$$THD(dBc) = 20*\log\sqrt{\frac{V2^2 + V3^2 + V4^2 + V5^2 + V6^2}{V1}}$$

Where:
V1 is the RMS power of the input frequency (fundamental)
V2 to V6 are the RMS values of the first five harmonics

Spurious Free Dynamic Range (SFDR)

The Spurious Free Dynamic Range defines the ratio between the RMS value of the fundamental to the RMS value of the largest peak off all spectral components below one-half of the sampling frequency, including harmonics but excluding DC.

Channel to Channel Isolation

The Channel to Channel Isolation (Crosstalk) defines the coupling of energy from one channel into the other channel in the ADC. It is measured by applying a 40kHz sine wave to all unselected channels and the attenuation to a 50kHz input sine wave is determined.

Intermodulation Distortion (IMD)

The Intermodulation Distortion measures the creations of additional spectral components that are caused by nonlinearities when applying a two tone sine wave on the input of the ADC. IMD is the ration of the RMS power in either the second or the third intermodulation products to the sum of both input frequencies.

2nd order intermodulation products (IM2): f1+f2, f2-f1

3rd order intermodulation products (IM3): 2*f1-f2, 2*f2-f1, 2*f1+f2, 2*f2+f1

Full Power Bandwidth / Full Linear Bandwidth

The Full Power Bandwidth defines the frequency at which the reconstructed input signal amplitude drops 3dB from the actual amplitude of the input signal, when applying a full scale signal.

The Full Linear Bandwidth defines the frequency at which the reconstructed input signal amplitude drops 0.1dB from the actual amplitude of the input signal, when applying a full scale signal.

9 Detailed Description

The AS1545 is a dual, 6-channel (six single-ended, three pseudo-differential or three fully-differential for each multiplexer), 12-bit, 1 MSPS, high speed, successive approximation (SAR) analog-to-digital converter (ADC). The AS1545 is designed to operate with a single +2.7V to +5.25V supply and a sampling rate of up to 1 MSPS. The serial interface provides easy interfacing to microprocessors.

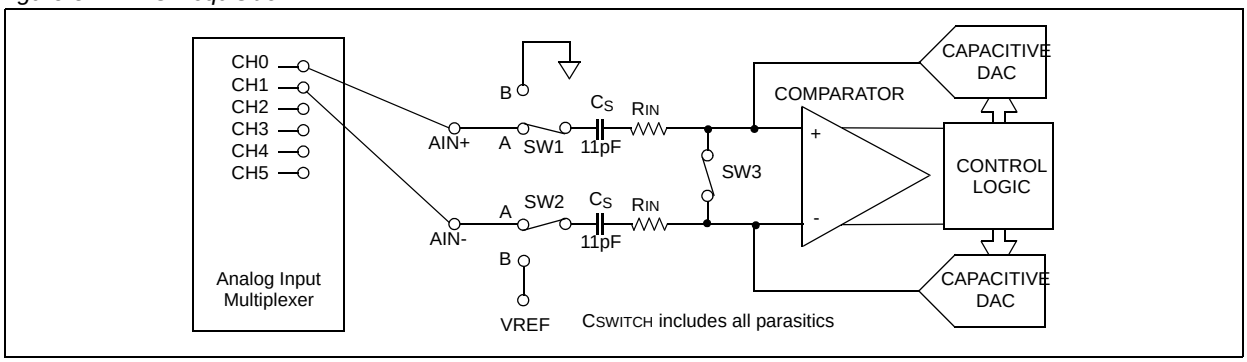
The AS1545 feature two on-chip, differential track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins on a single die. The AS1545 is available in a 32-lead TQFN package, offering the user considerable space-saving advantage.

The AS1545 can convert analog input signals in the range [0V to V_{REFIN}] or [0V to 2 x V_{REFIN}] in single-ended or pseudo-differential mode or [-V_{REFIN}/2 to +V_{REFIN}/2] or [-V_{REFIN} to +V_{REFIN}] in fully differential mode. The AS1545 has an on-chip 2.5V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used then the output needs to be buffered first. The AS1545 also features power-down options to allow power saving between conversions. The power-down feature is implemented via the standard serial interface.

Analog Input

The AS1545 consists of successive approximation ADCs, each around two capacitive DACs and 12 analog inputs. Each on-board ADC has six analog inputs that can be configured as six single-ended channels, three pseudo differential channels, or three fully differential channels. Figure 32 and Figure 33 shows one of these ADCs in acquisition and conversion phase, respectively. The ADC consists of a control logic, a SAR, and two capacitive DACs.

Figure 32. ADC Acquisition



Acquisition Time

During data acquisition time (t_{ACQ}) SW3 is closed, SW1 and SW2 are in track position, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input. At the raising edge of the CSN signal, SW3 opens and SW1 and SW2 go into hold position, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the AIN+ and AIN- pins must be matched. Otherwise, the two inputs will have different settling times, resulting in errors.

Figure 33. ADC Conversion Phase

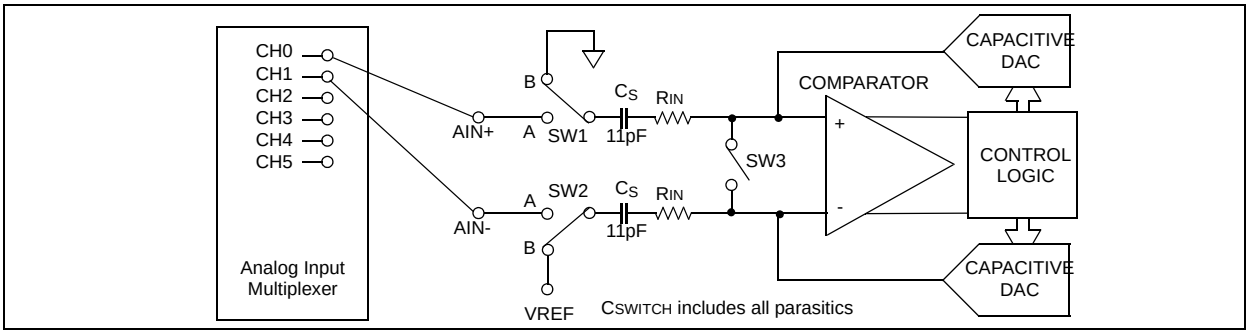
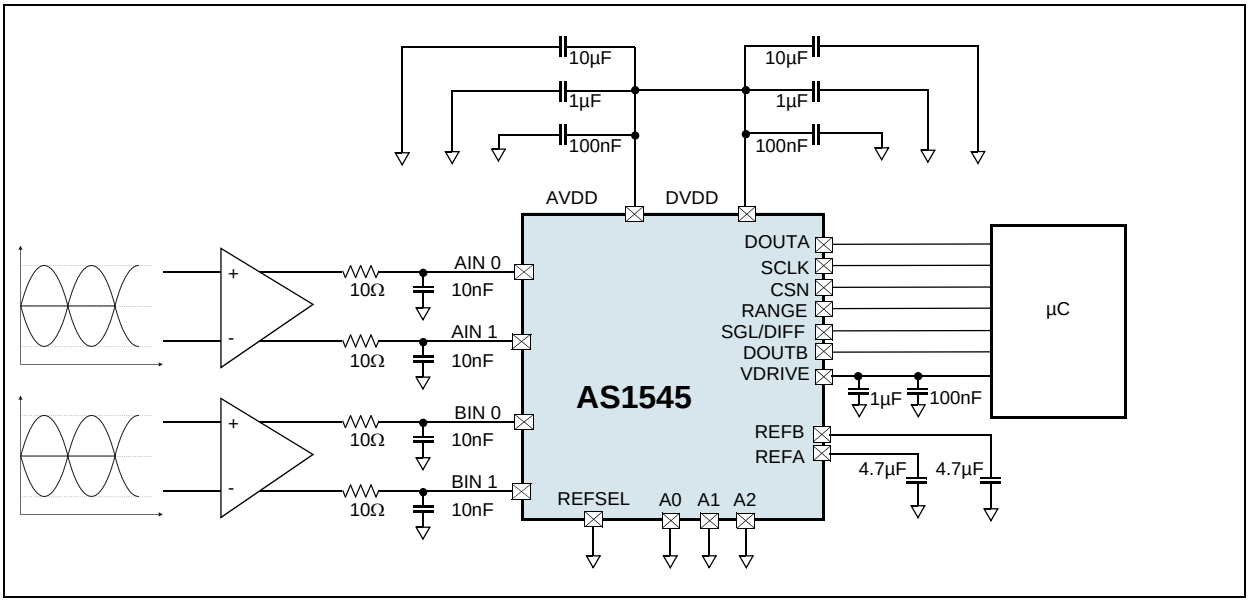


Figure 34. Typical Application



Analog Input Composition

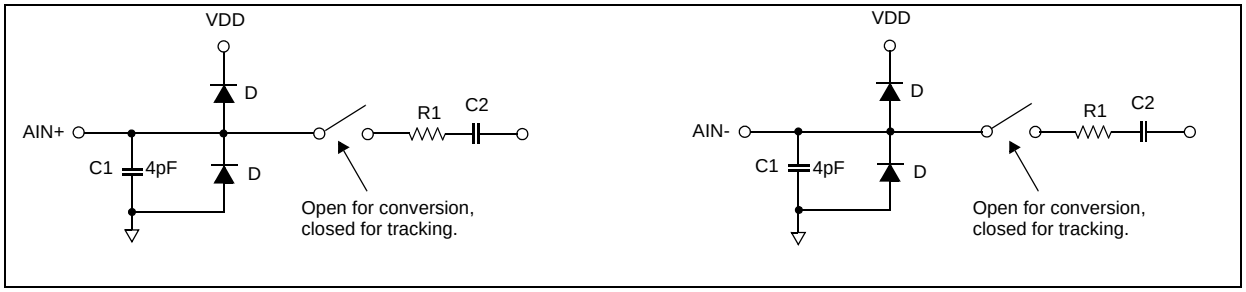
The equivalent circuit of analog input structure of the AS1545 in differential/pseudo differential modes is shown in the Figure 35. In single-ended mode, AIN- is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. These diodes can conduct up to 10mA without causing irreversible damage to the part.

Note: Make sure that the analog input signals never exceed the supply rails by more than 300mV. This causes the diodes to become forward-biased and starts conducting into the substrate.

The C1 capacitors in Figure 35 are of 4pF and can be attributed to pin capacitance. The value of these resistors is typically about 100Ω. The C2 capacitors are the ADC's sampling capacitors with a capacitance of 20pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins with optimum values of 10Ω and 10nF. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

Figure 35. Equivalent Analog Input Circuit



When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades.

Figure 23 on page 13 shows a graph of the THD vs. the analog input signal frequency for various supplies in single-ended mode, while Figure 25 shows the THD vs. the analog input signal frequency for various supplies in differential mode.

Figure 22 on page 13 shows a graph of the THD vs. the analog input frequency for different source impedances.

Analog Input Modes

Table 5. Address Map

Address Map								
SGL/ DIFF	A2	A1	A0	ADC A		ADC B		Comments
				AIN+	AIN-	BIN+	BIN-	
1	0	0	0	AIN0	GND	BIN0	GND	Single Ended
1	0	0	1	AIN1	GND	BIN1	GND	Single Ended
1	0	1	0	AIN2	GND	BIN2	GND	Single Ended
1	0	1	1	AIN3	GND	BIN3	GND	Single Ended
1	1	0	0	AIN4	GND	BIN4	GND	Single Ended
1	1	0	1	AIN5	GND	BIN5	GND	Single Ended
0	0	0	0	AIN0	AIN1	BIN0	BIN1	Fully Differential
0	0	0	1	AIN0	AIN1	BIN0	BIN1	Pseudo Differential
0	0	1	0	AIN2	AIN3	BIN2	BIN3	Fully Differential
0	0	1	1	AIN2	AIN3	BIN2	BIN3	Pseudo Differential
0	1	0	0	AIN4	AIN5	BIN4	BIN5	Fully Differential
0	1	0	1	AIN4	AIN5	BIN4	BIN5	Pseudo Differential
0	1	1	0	AIN0	AIN1	BIN0	BIN1	Pseudo Differential Difference – A/B Phases – Counter

Table 6. Input Range

SGL/DIFF	Range	Ain+ - Ain- Range	Coding	Example
1	0	0 to V_{REF}	Straight	AIN+ - AIN- = 1.766 V Output Decimal = 2894 Output Binary = 1011 0100 1110
1	1	0 to $2V_{REF}$	Straight	AIN+ - AIN- = 1.766V Output Decimal = 1447 Output Binary = 0101 1010 0111
0	0	0 to V_{REF}	Straight	AIN+ - AIN- = 1.666 V Output Decimal = 2703 Output Binary = 1010 1010 1010
0	1	0 to $2V_{REF}$	Straight	AIN+ - AIN- = 1.666 V Output Decimal = 1365 Output Binary = 0101 0101 0101
0	0	$-V_{REF}/2$ to $+V_{REF}/2$	2's comp	AIN+ - AIN- = 1.666 V Output Decimal = 4095 Output Binary = 0111 1111 1111 (its 2's comp)
0	1	$-V_{REF}$ to $+V_{REF}$	2's comp	AIN+ - AIN- = 1.666 V Output Decimal= 3413 Output Binary= 0101 0101 0101 (its 2's comp)

Single-Ended Mode

The AS1545 consists of 12 single-ended analog input channels with range that can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}.

Note: In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC.

If the sampling analog input is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it correctly formatted for the ADC. Figure 36 shows the connecting diagram when operating the ADC in single-ended mode.

Figure 36. Single-Ended Mode Connection Diagram

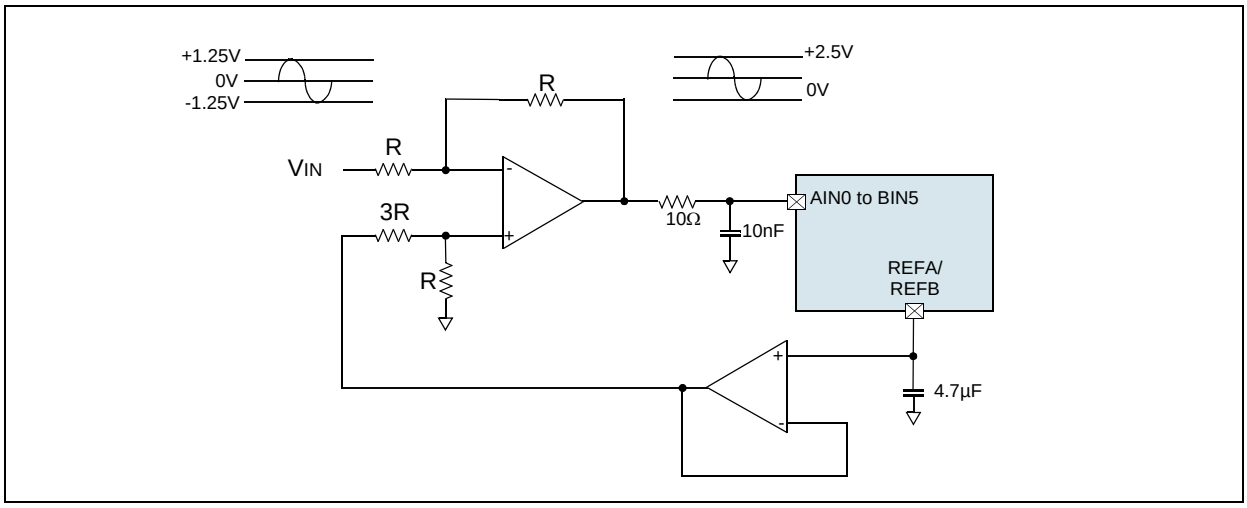
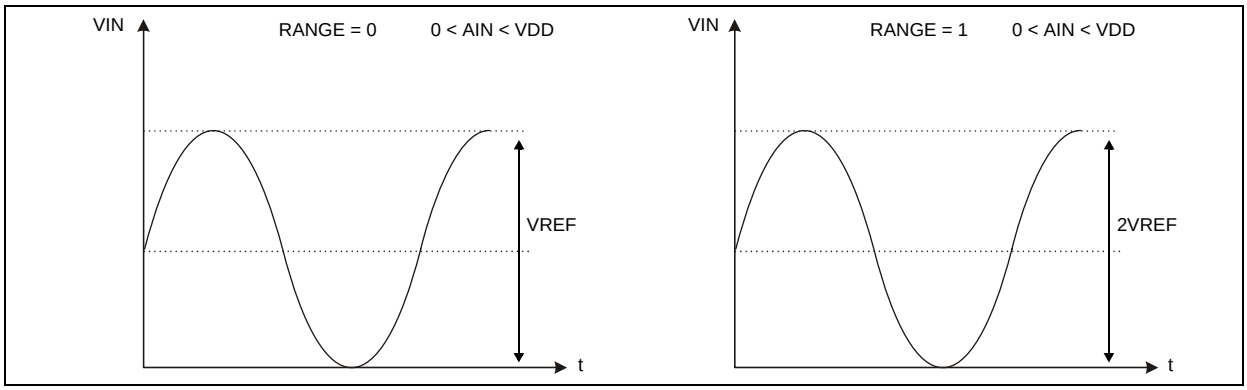


Figure 37. Definition of Single-Ended Input



Fully Differential Mode

The AS1545 consists of six differential analog input pairs. Figure 38 defines the fully differential analog input of the AS1545. The amplitude of the differential signal is the difference between the signals applied to the AIN+ and AIN- pins in each differential pair (AIN+ - AIN-). These pins should be simultaneously driven by two signals each of amplitude $V_{REF}/2$ (or V_{REF}, depending on the range required) that are 180º out of phase. If RANGE = 1 is selected the amplitude of the differential signal is $\pm V_{REF}$ regardless of the common mode (CM).

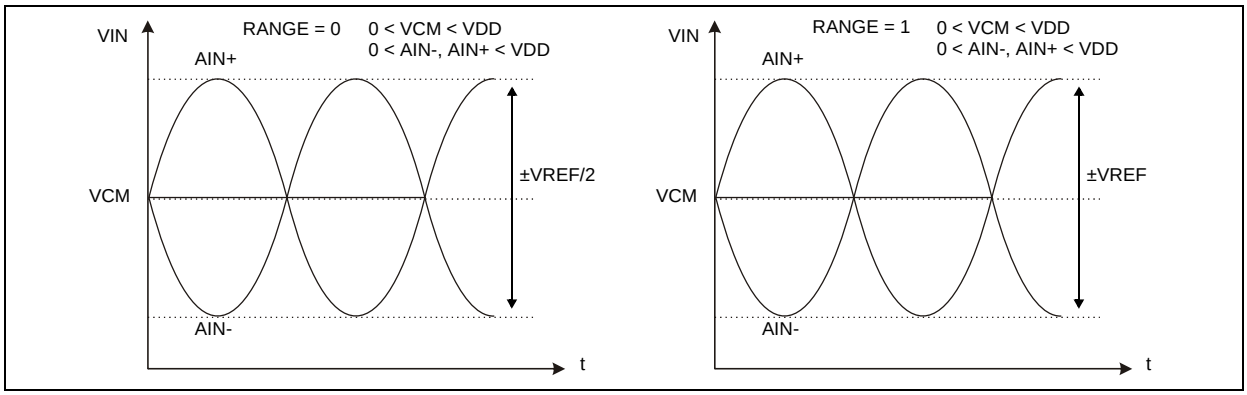
The common mode is the average of the two signals and is therefore the voltage on which the two inputs are centered.

$$(V_{IN}+ + V_{IN}-)/2 \qquad \text{(EQ 1)}$$

Althought fully differential operation with phase between inputs of 180° is recommanded, non true differential signals can also be applied.

Note: It is important to note that the absolute voltage of the analog inputs goes from AGND to V_{DD}.

Figure 38. Definition of Fully Differential Input



Pseudo Differential Mode

The AS1545 consists of six pseudo differential pairs. In pseudo differential mode, AIN+ is connected to the signal source with an amplitude of V_{REF} or 2 × V_{REF} (depending on the range selected) to make use of the full dynamic range of the part. A dc input is applied to the AIN- pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the AIN+ input. The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground allowing dc common-mode voltages to be cancelled. Figure 39 shows a connection diagram for pseudo differential mode.

Figure 39. Pseudo Differential Mode Connection Diagram

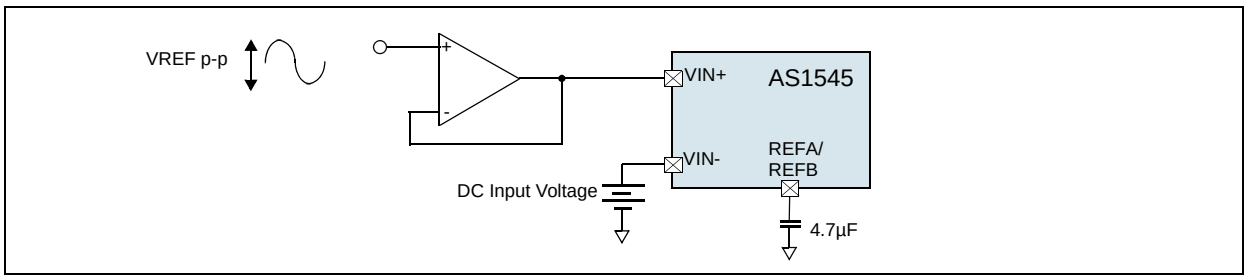
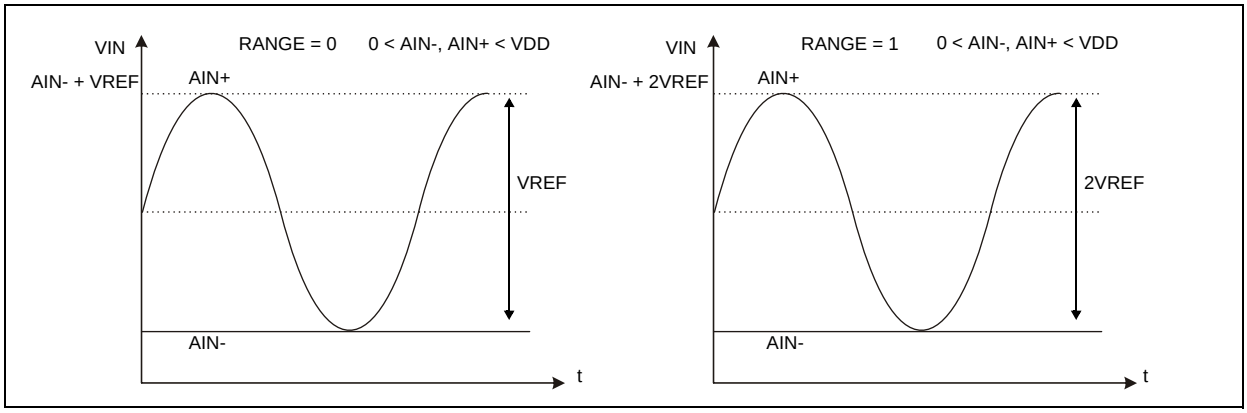


Figure 40. Definition of Pseudo Differential Input



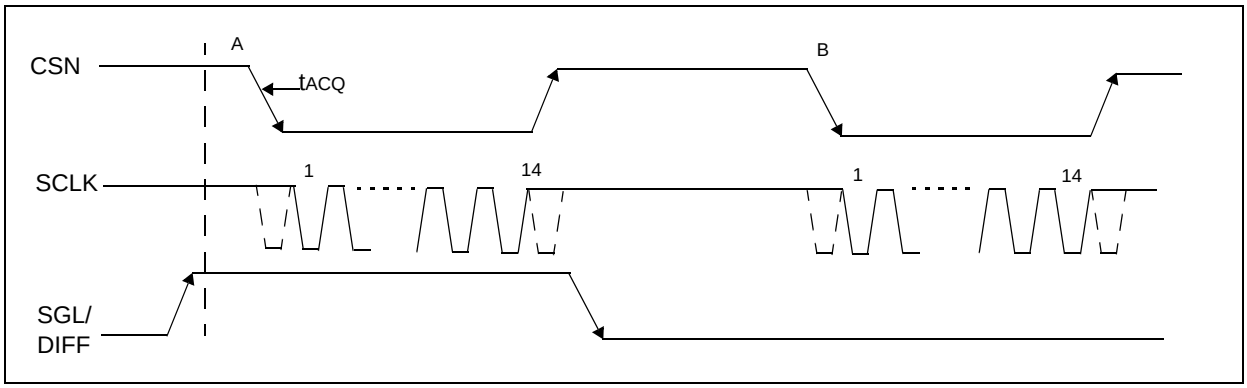
Analog-to-Digital Conversion

The analog inputs of the AS1545 can be configured as single-ended pseudo-differential or fully differential via the SGL/DIFF logic pin, as shown in Figure 41. If this pin is coupled to a logic low, the analog input channels to each on-chip ADC are set up as three fully differential pairs or 3 pseudo-differential inputs. If this pin is at logic high, the analog input channels to each on-chip ADC are set up as six single-ended analog inputs. The required logic level on this pin needs to be established prior to the acquisition time and remain unchanged during the conversion time until the track-and-hold has returned to track. The track-and-hold returns to track on the 13th rising edge of SCLK after the CSN falling edge (see Figure 51). If the level on this pin is changed, it is recognized by the AS1545; therefore, keep the same logic level during acquisition and conversion to avoid corrupting the conversion in progress.

The channels used for simultaneous conversions are selected via the multiplexer address input pins, A0 to A2. The logic states of these pins also need to be established prior to the acquisition time; however, they may change during the conversion time, provided that the mode is not changed. If the mode is changed from fully differential to pseudo-differential, for example, then the acquisition time would start again from this point. The selected input channels are decoded as shown in Table 5 on page 20.

The analog input range of the AS1545 can be selected as [0V to V_{REF} or -V_{REF}/2 to +V_{REF}/2] or [0V to 2×V_{REF} or -V_{REF} to +V_{REF}] via the RANGE and MODE pin (see Table 5 on page 20). This selection is made in a similar fashion to that of the SGL/DIFF pin by setting the logic state of the RANGE pin a time t_{ACQ} prior to the falling edge of CSN. The logic level on this pin can be altered after the third falling edge of SCLK. If this pin is tied to a logic low, the analog input range selected is [0V to V_{REF} or -V_{REF}/2 to +V_{REF}/2]. If this pin is tied to a logic high, the analog input range selected is [0V to 2×V_{REF} or -V_{REF} to +V_{REF}].

Figure 41. Selecting Differential or Singe-Ended Configuration



Output Coding

The AS1545 output coding is set to either twos complement or straight binary, depending on which analog input configuration is selected for a conversion. Output coding scheme for each possible analog input configuration is show in the Table 7.

Table 7. AS1545 Output Coding

MODE	Output Coding
Differential	Twos complement
Single-Ended	Straight binary
Pseudo-Differential	Straight binary

Transfer Functions

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is V_{REF}/4096 when the 0V to V_{REF} range is used, and the LSB size is 2 × V_{REF}/4096 when the 0V to 2 × V_{REF} range is used. In differential mode, the LSB size is 2 × V_{REF}/4096 when the 0V to V_{REF}. The ideal transfer characteristic for the AS1545 when straight binary coding is output is shown (with the 2 × V_{REF} range) in Figure 42 & Figure 43 on page 24, and Figure 44 & Figure 45 on page 24 shows the twos complement.

Figure 42. Straight Binary Transfer Function for Single-Ended, RANGE = 0

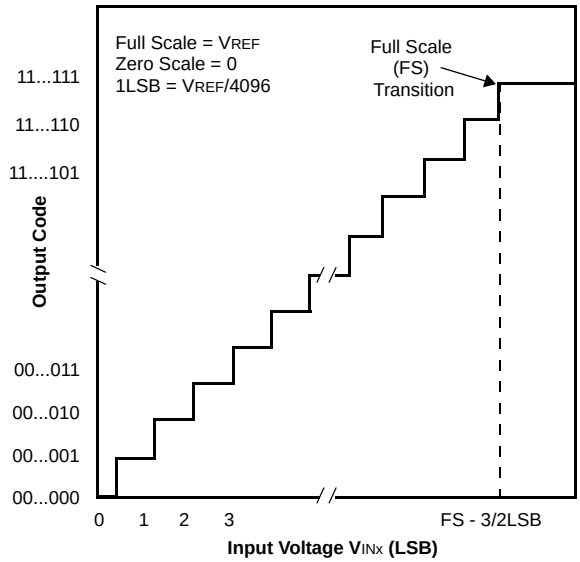


Figure 43. Straight Binary Transfer Function for Single-Ended, RANGE = 1

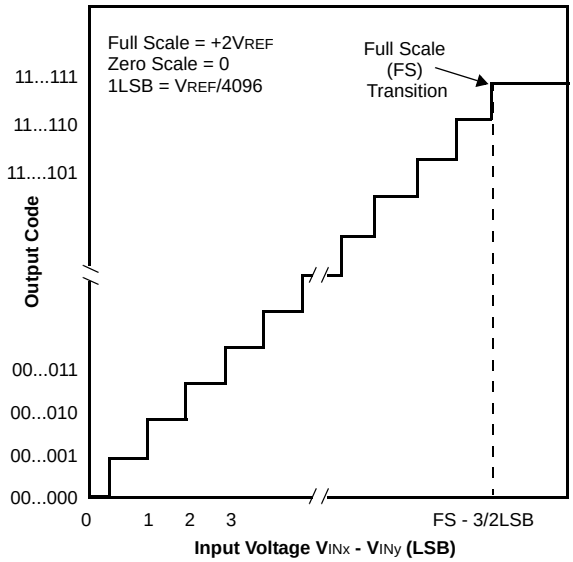


Figure 44. Two's Complement Transfer Function for Differential, RANGE = 0

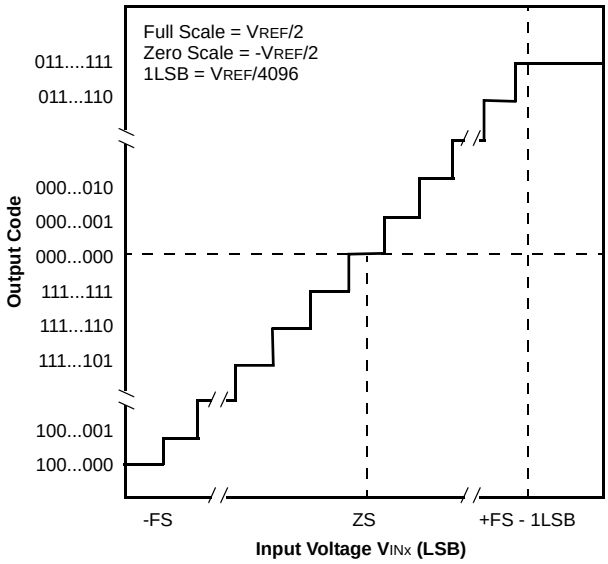
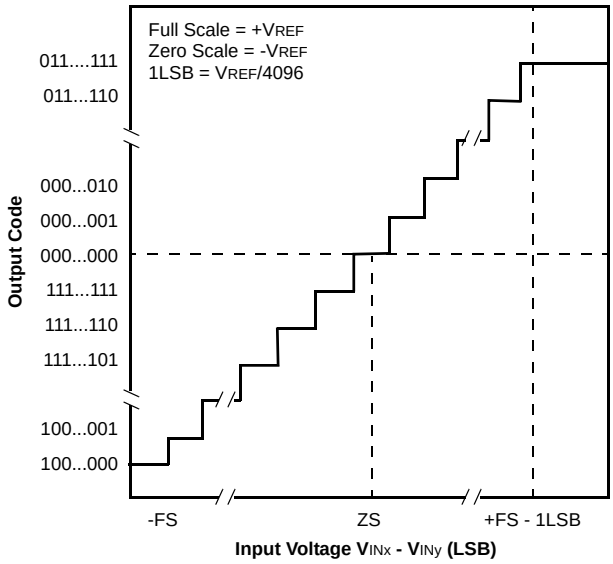


Figure 45. Two's Complement Transfer Function for Differential, RANGE = 1



Digital Inputs

V_{DRIVE} Functionality

The AS1545 also has a VDRIVE feature to control the voltage at which the serial interface operates and allows the ADC to easily interface to both 3V and 5V processors. For example, if the AS1545 was operated with a VDD of 5V, the VDRIVE pin could be powered from a 3V supply, allowing a large dynamic range with low voltage digital processors. Therefore, the AS1545 could be used with the 2 × VREF input range, with a VDD of 5V while still being able to interface to 3V digital parts.

10 Application Information

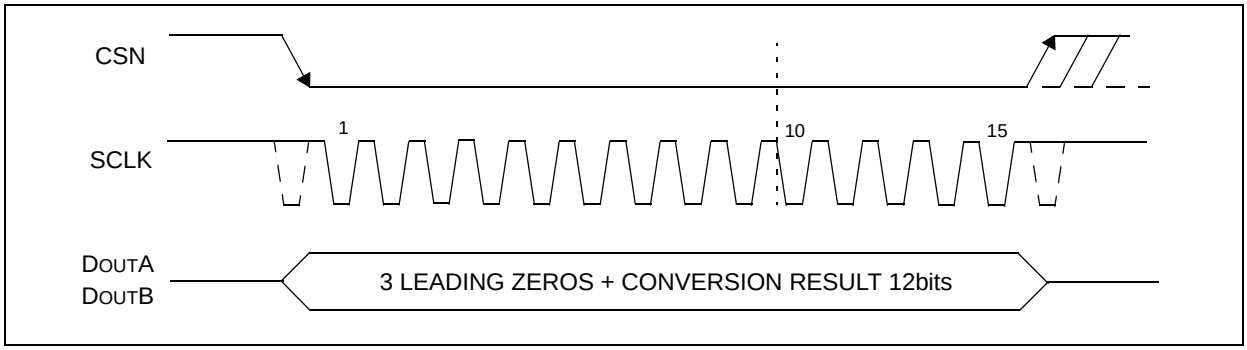
Operation Modes

The operation mode of the AS1545 is selected by controlling the (logic) state of the CSN signal during a conversion process. There are three possible modes of operation: Full Power-UP mode, Full Power-Down mode, and Partial Power-Down mode. After a conversion is initiated, the point at which CSN is pulled high determines which power-down mode, if any, the device enters. Similarly, in power-down mode, CSN can control whether the device returns to Full Power-Up mode or remains in power-down. These modes of operation provides flexible power management and can be selected to optimize the power dissipation/throughput rate ratio for differing application requirements.

Full Power-Up Mode

In this mode the AS1545 is fully powered all the time without any power-up time. This mode is suitable for applications that need the fastest throughput rates. Figure 46 shows the general diagram of the operation of the AS1545 in this mode. On the falling edge of CSN conversion is initiated. To ensure that the part remains fully powered up at all times, CSN must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of CSN. The conversion is terminated and DOUTA and DOUTB go back into three-state, if CSN is brought high any time after the 10th SCLK falling edge but before the 15th SCLK falling edge. During this process the part remains powered up.

Figure 46. Full Power-Up Mode Operation



Fiveteen serial clock cycles are required to complete the conversion and access the conversion result. The DOUT line does not return to three-state after 15 SCLK cycles have elapsed, but instead does so when CSN is brought high again. If CSN is left low for another SCLK cycle (for example, if only a 16 SCLK burst is available), one trailing zeros are clocked out after the data. If CSN is left low for a further 16 SCLK cycles, the result from the other ADC on board is also accessed on the same DOUT line, as shown in Figure 52 (see Serial Interface on page 28)

Once 32 SCLK cycles have elapsed, the DOUT line returns to three-state on the 32nd SCLK falling edge. If CSN is brought high prior to this, the DOUT line returns to three-state at that point. Once a data transfer is complete and DOUTA and DOUTB have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing CSN low again (assuming the required acquisition time is allowed).

Full Power-Down Mode

This mode is intended for applications where throughput rates are slower. In this mode the AS1545 will stay power down until the falling edge of CSN. The device continues to power-up when the CSN is held low till the falling edge of the 10th SCLK.

When the AS1545 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 50 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing CSN high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 48. Once CSN is brought high in this window of SCLKs, the part completely powers down.

Note: It is important to note, that the full power-down mode can only be established if both digital outputs, DOUTA and DOUTB are not left floating. Therefore a pulldown or pullup of >1GΩ is required.

Figure 47. Exiting Partial Power-Down Mode

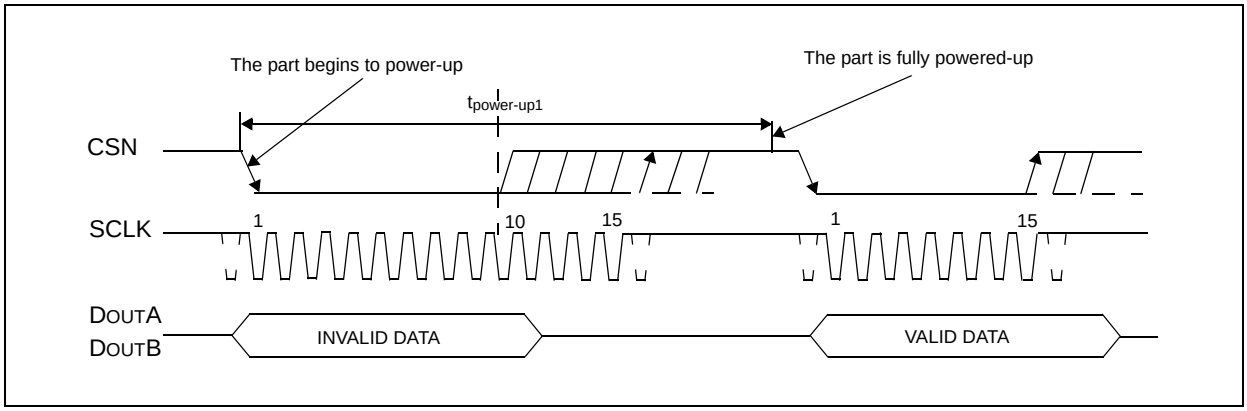


Figure 48. Entering Full Power-Down Mode

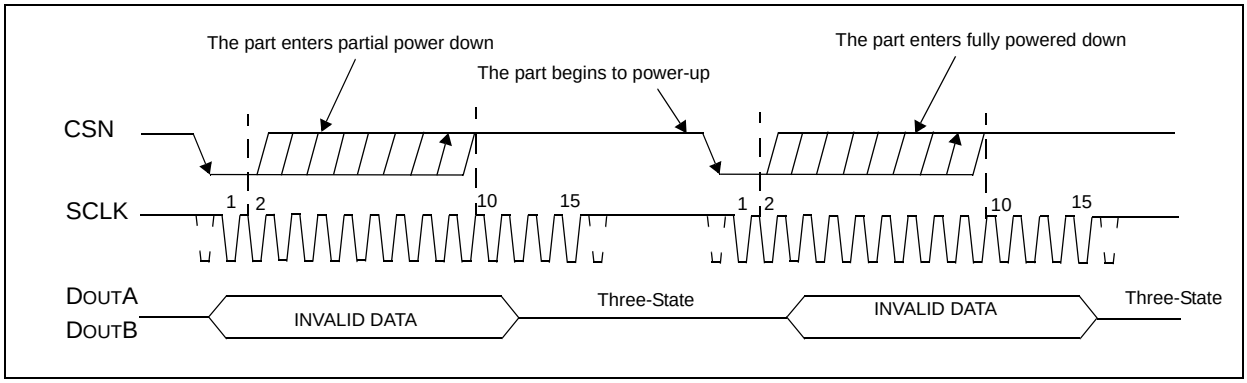
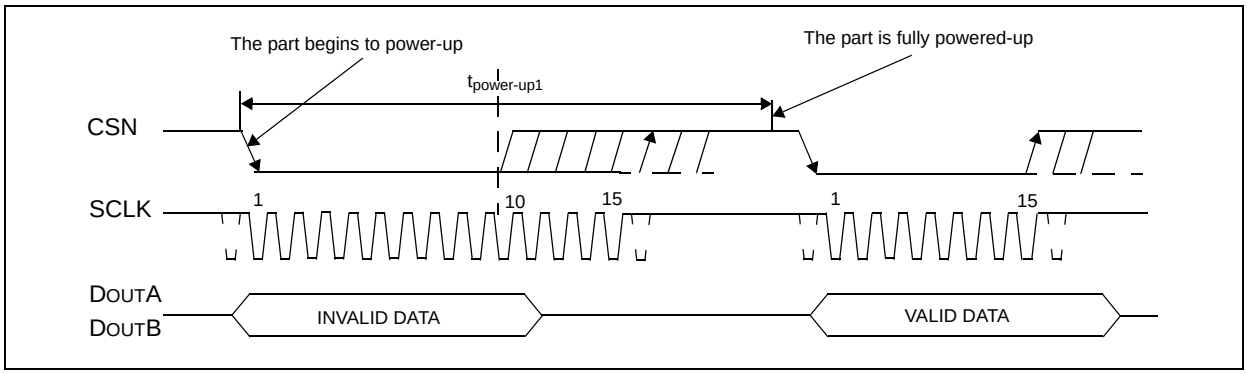


Figure 49. Exiting Full Power-Down Mode



Note: It is not necessary to complete the 15 SCLKs once CSN is brought high to enter a power-down mode.

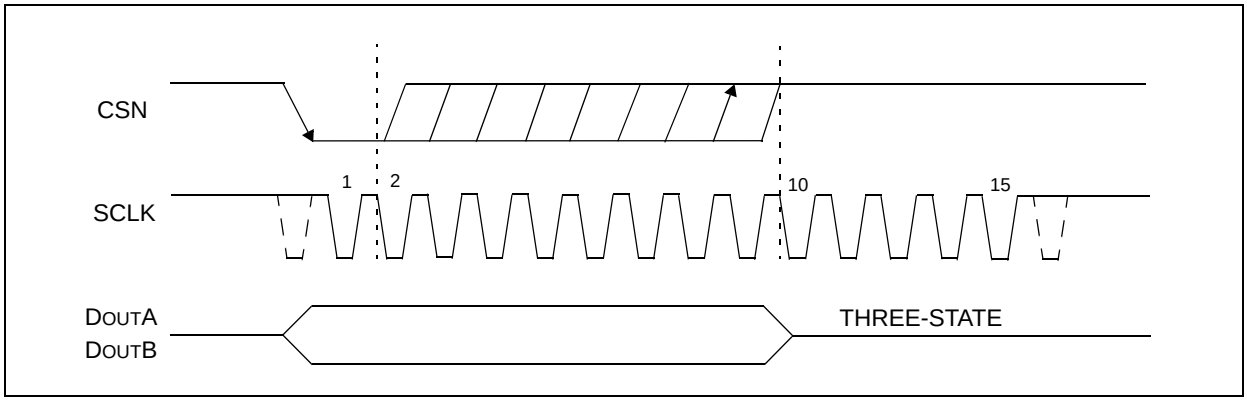
The required power-up time must elapse before a conversion can be initiated, as shown in Figure 49.

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate, and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AS1545 is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down mode, the conversion process must be interrupted by bringing CSN high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 50. Once CSN is brought high in this window of SCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of CSN is terminated, and DOUTA and DOUTB go back into three-state. If CSN is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the CSN line.

Figure 50. Partial Power-Down Mode



To exit this mode of operation and power up the AS1545 again, a dummy conversion is performed. On the falling edge of CSN, the device begins to power up and continues to power up as long as CSN is held low until after the falling edge of the 10th SCLK. The device is fully powered up after approximately 1 µs has elapsed, and valid data results from the next conversion, as shown in Figure 47. If CSN is brought high before the second falling edge of SCLK, the AS1545 again goes into partial power-down. This avoids accidental power-up due to glitches on the CSN line. Although the device may begin to power up on the falling edge of CSN, it powers down again on the rising edge of CSN. If the AS1545 is already in partial power-down mode and CSN is brought high between the second and 10th falling edges of SCLK, the device enters full power-down mode.

Power-Up Times

As described in detail, the AS1545 has two power-down modes, partial power-down and full power-down. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times, as explained in this section, apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins.

The power-up time is always 1µs, independent of the mode currently in.

Note: It is important to note that, when using the internal reference, charging the external reference capacitance typically needs around 250µs but can take up to 1ms.

When power supplies are first applied to the AS1545, the ADC may power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold CSN low until after the 10th SCLK falling edge (see Figure 46); in the second cycle, CSN must be brought high before the 10th SCLK edge but after the second SCLK falling edge (see Figure 50). Alternatively, if it is intended to place the part in full power-down mode when the supplies are applied, then three dummy cycles must be initiated. The first dummy cycle must hold CSN low until after the 10th SCLK falling edge (see Figure 46); the second and third dummy cycles place the part in full power-down (see Figure 48).

Once supplies are applied to the AS1545, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

Power vs. Throughput Rate

The power consumption of the AS1545 varies with throughput rate. When using very slow throughput rates and as fast an SCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the AS1545 quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed SCLK value is used or if it is scaled with the sampling rate. Figure 10 on page 11 shows plots of power vs. the throughput rate when operating in normal mode for a fixed maximum SCLK frequency, and an SCLK frequency that scales with the sampling rate with V_{DD} = 3V and V_{DD} = 5V, respectively. In all cases, the internal reference was used.

Serial Interface

The timing diagram for serial interfacing to the AS1545 is shown in Figure 51. The serial clock provides the conversion clock and controls the transfer of information from the AS1545 during conversion.

The CSN signal initiates the data transfer and conversion process. The falling edge of CSN puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires a minimum of 15 SCLKs to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 51 at Point B. If a 16-SCLK transfer is used, then two trailing zeros will appear after the final LSB. On the rising edge of CSN, the conversion is terminated and D_{OUT}A and D_{OUT}B go back into three-state. If CSN is not brought high but is instead held low for a further 15 SCLK cycles on D_{OUT}A, the data from Conversion B is output on D_{OUT}A (followed by 1 trailing zero).

Likewise, if CSN is held low for a further 15 SCLK cycles on D_{OUT}B, the data from Conversion A is output on D_{OUT}B. This is illustrated in Figure 52 where the case for D_{OUT}A is shown. In this case, the D_{OUT} line in use goes back into three-state on the 32nd SCLK falling edge or the rising edge of CSN, whichever occurs first.

A minimum of 15 serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AS1545. CSN going low provides the 3 leading zeros to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges. Therefore, the first falling clock edge on the serial clock has the leading zero provided and also clocks out the second leading zero. The 12-bit result then follows after a third leading zero with the final bit in the data transfer valid on the 15th falling edge, having being clocked out on the previous (14th) falling edge. It may also be possible to read in data on each SCLK rising edge depending on the SCLK frequency or the supply voltage. The secondrising edge of SCLK after the CSN falling edge would have the third leading zero provided, and the 14th rising SCLK edge would have DB0 provided.

If a falling edge of SCLK is coincident with the falling edge of CSN, then this falling edge of SCLK is not acknowledged by the AS1545, and the next falling edge of SCLK will be the first registered after the falling edge of CSN.

Figure 51. Timing Diagram

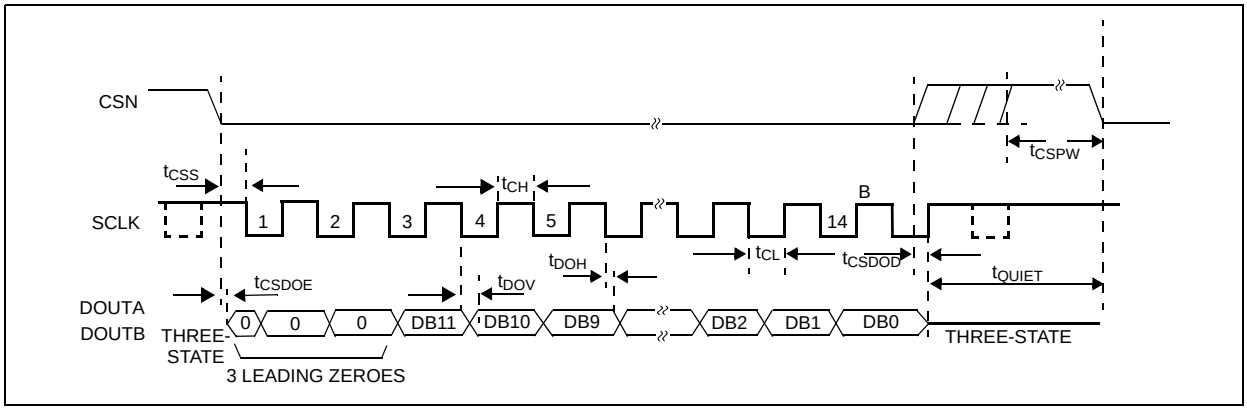


Figure 52. Reading Data from Both ADCs on One DOUT Line with 32 SCLKs

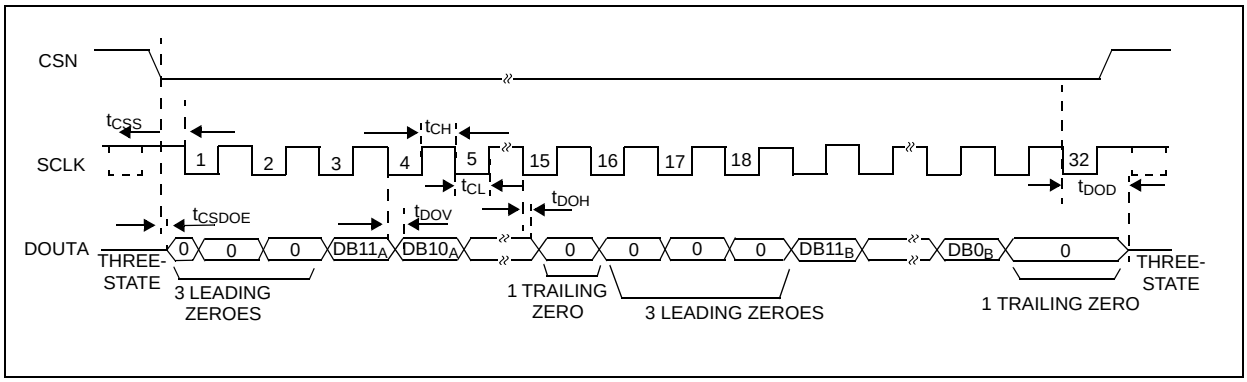
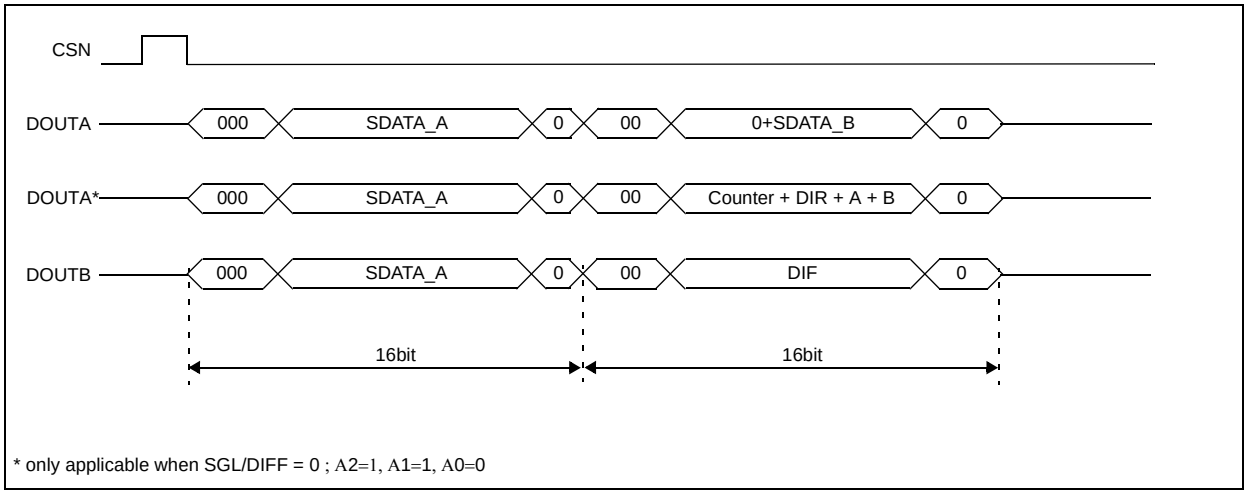


Figure 53. 32 SCLKs Data transfer for all modes in DOUTA, DOUTB



Difference calculator and quadrature signals calculator

The AS1545 internally calculates the difference between the output codes of ADC A and ADC B. There are several requirements that need to be taken into account in order to work with the difference calculator. First off, the output data of both ADCs needs to be in straight binary coding. This means that the difference calculator will only give the correct results in single ended and pseudo differential modes. Also, it is important to note that in order to read the data from the difference calculator we must read all 32 bits of data of the ADC, therefore reducing the overall sampling rate of the ADC by half.

The difference calculator will always give you a 13 bit two's complement result. The first bit is the sign of the operation and the next 12 bits are the data. For simplicity in the design, an systematic error of 1 LSB can be expected from the difference calculator.

Below we have an detailed example describing the operation of the difference calculator.

Let's assume that V_{INA} = 1.667V V_{INB} = 2V V_{REF} = 2.5V and we are working in single ended mode.

DOUT_A = 1010 1010 1010 or 2730 in decimal
DOUT_B = 1100 1100 1100 or 3276 in decimal

The difference should be 2730-3276=-546 in decimal

In 2's complement -546 is 1 1101 1101 1110 in binary. This is a 1 for the minus sign plus 4096-546=3550 in decimal which corresponds to 1101 1101 1110 in binary

As stated before, there is a -1LSB error in the operation so the actual output should be -547 in decimal which corresponds to 1 1101 1101 1101 in binary which is the result that the difference calculator clocks out.

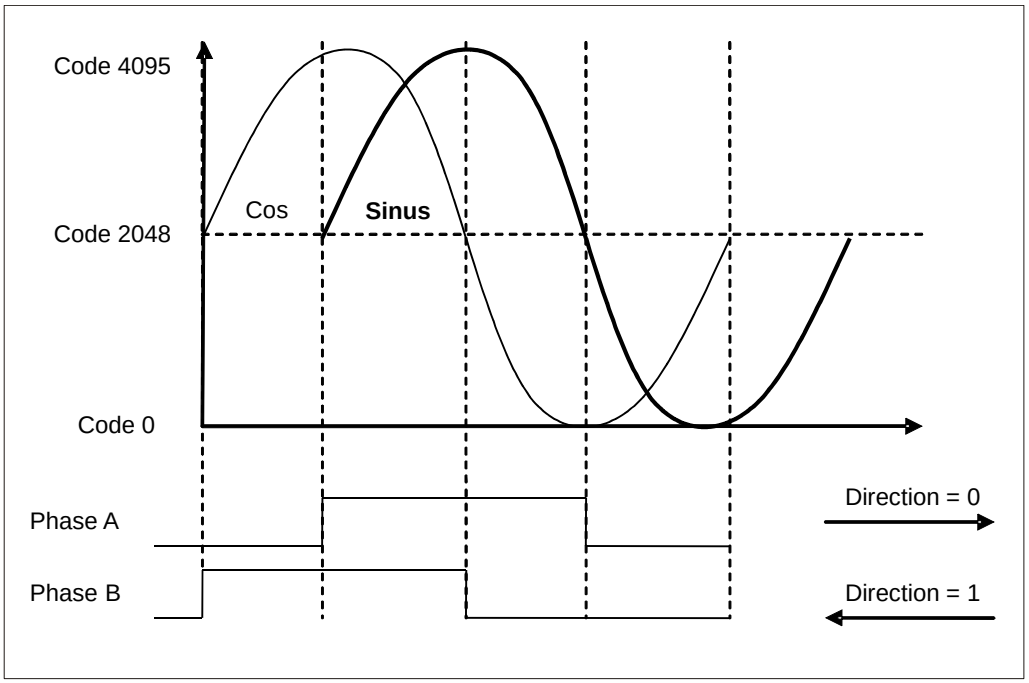
On top of the difference calculator, the ADC also provide us with information regarding input signals in quadrature (90 degrees phase difference) like the ones we would get from a position calculation system of a motor control.

In order for this mode to work, we must have SGL/DIFF=0, A2=1. A1=1. A0=0, according to what is specified in the channel addresses table. Also, it is important to note that in order to read the data from the quadrature inputs calculator we must read all 32 bits of data of the ADC, therefore reducing the overall sampling rate of the ADC by half.

The ADC provides us with the following information:

- Phase A and Phase B bits, dividing the period into four quadrants
- DIR bit, which indicates the direction of the rotation of the rotor
- Counter, this is a 10 bit word that, in the case of using a step down in the rotor indicates the number of times the step down has spun. The counter increases twice per period if DIR is equal zero and decreases twice per period if DIR equals one.

Figure 54. A to B phase



Direction of the rotor based on the DIR bit

If the rotor is rotating as the above picture, the direction bit is low.

If the rotor is rotating in the opposite direction to the above picture, the direction bit is high.

Note: This mode works only for SGL/DIFF=0, A2=1. A1=1. A0=0.

11 Application Hints

Grounding and Layout

The analog and digital supplies to the AS1545 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AS1545 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All three AGND pins of the AS1545 should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the AS1545 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the AS1545.

Avoid running digital lines under the device as this couples noise onto the die. However, the analog ground plane should be allowed to run under the AS1545 to avoid noise coupling. The power supply lines to the AS1545 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF ceramic capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

PCB Design Guidelines for TQFN

The lands on the TQFNpackage are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width, thereby having a portion of the pad exposed. To ensure that the solder joint size is maximized, the land should be centered on the pad.

The bottom of the chip scale package has a thermal pad. The thermal pad on the PCB should be at least as large as the exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

To improve thermal performance of the package, use thermal via on the PCB incorporating them in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the PCB thermal pad to AGND.

12 Package Drawings and Markings

Figure 55. 32-lead TQFN Package

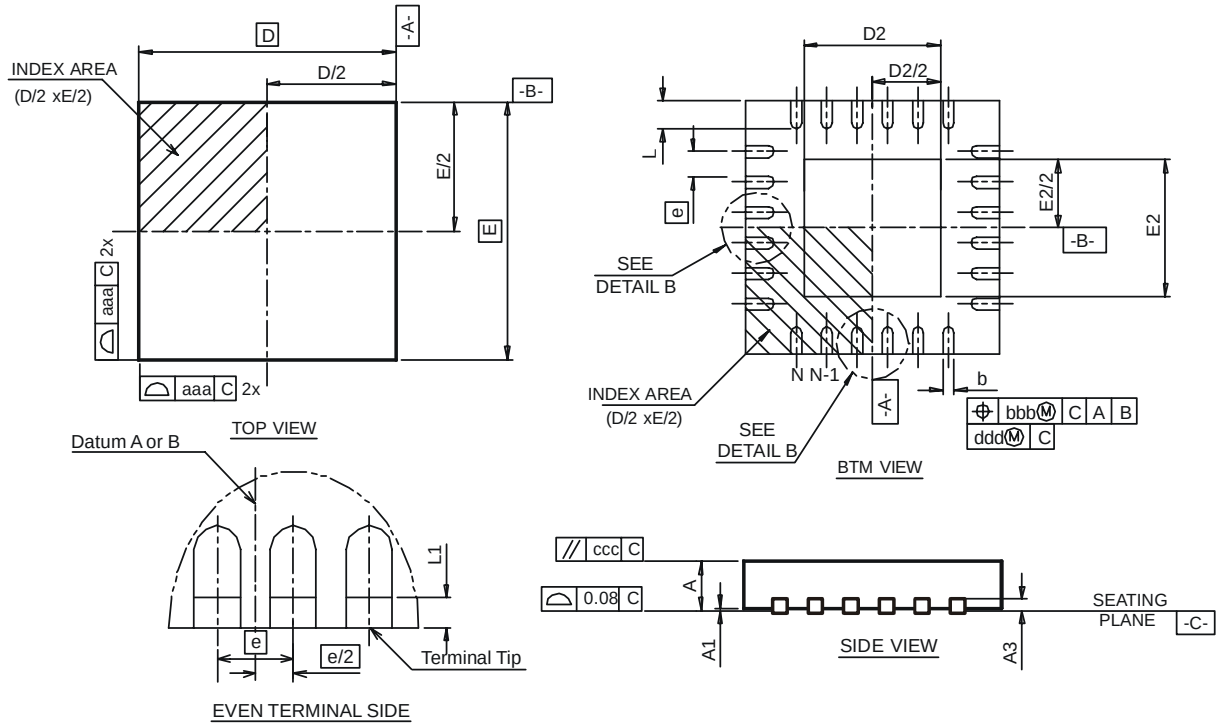


Table 8. 32-lead TQFN Package Dimensions

Symbol	Min	Nom	Max	Note		Symbol	Min	Nom	Max	Note
A	0.70	0.75	0.80	1,2		b	0.18	0.25	0.30	1,2,5
A1	0.00	0.02	0.05	1,2		L	0.30	0.40	0.50	1,2,5
L1	0.03		0.15	1,2		N		32		1,2,5
K	0.20			1,2		ND		8		1,2,5
e		0.5				NE		8		1,2,5
D2	3.30	3.45	3.55	1,2,5		aaa		0.10		1,2
E2	3.30	3.45	3.55	1,2,5		bbb		0.10		1,2
D BSC		5.00		1,2,5		ccc		0.10		1,2
E BSC		5.00		1,2,5		ddd		0.05		1,2

Notes:

1. Figure 55 is shown for illustration only.
2. All dimensions are in millimeters; angles in degrees.
3. Dimensioning and tolerancing conform to *ASME Y14.5 M-1994*.
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95-1, SPP-012*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
7. ND refers to the maximum number of terminals on side D.
8. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

13 Ordering Information

The device is available as the standard products shown in Table 9.

Table 9. Ordering Information

Ordering Code	Description	Marking	Delivery Form	Package
AS1545-BQFT	Dual, 12-Bit, 1MSPS, SAR ADC	AS1545	T&R	32-lead TQFN

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
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