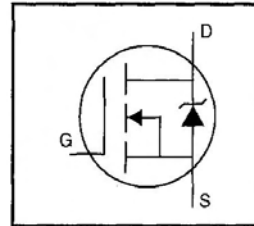


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- Dynamic dv/dt Rating
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}=4V$ & $5V$
- 175°C Operating Temperature
- Fast Switching
- Lead-Free

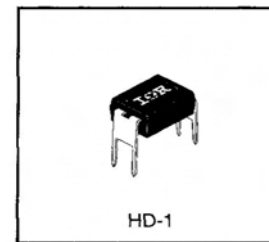


$V_{DSS} = 60V$
 $R_{DS(on)} = 0.20\Omega$
 $I_D = 1.7A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	1.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 5.0 V$	1.2	
I_{DM}	Pulsed Drain Current ①	14	
$P_D @ T_C = 25^\circ C$	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	490	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

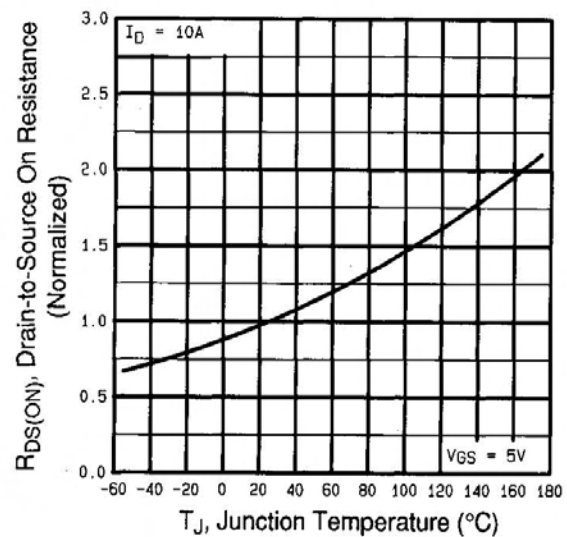
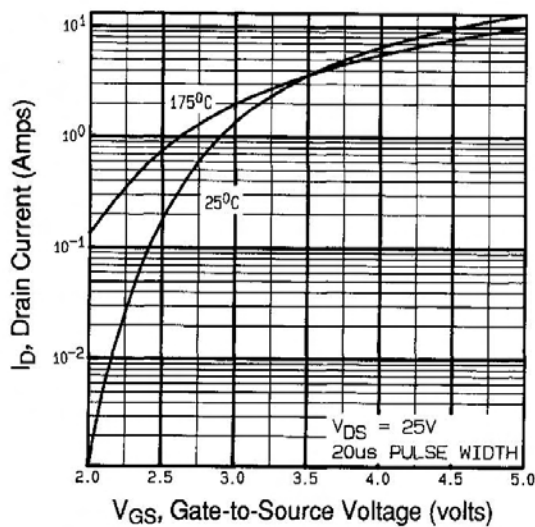
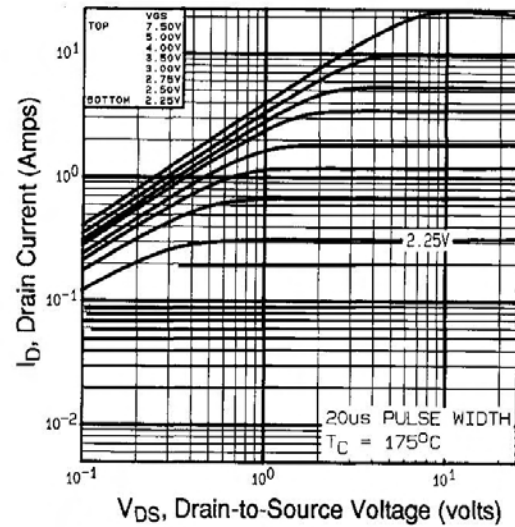
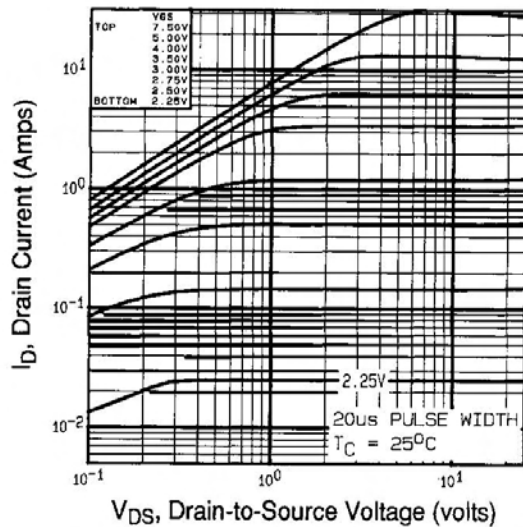
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.070	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	$V_{GS}=5.0V$, $I_D=1.0A$ ④
		—	—	0.28		$V_{GS}=4.0V$, $I_D=0.85A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
g_{fs}	Forward Transconductance	1.9	—	—	S	$V_{DS}=25V$, $I_D=1.0A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=60V$, $V_{GS}=0V$
		—	—	250		$V_{DS}=48V$, $V_{GS}=0V$, $T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
Q_g	Total Gate Charge	—	—	8.4	nC	$I_D=10A$
Q_{gs}	Gate-to-Source Charge	—	—	2.6		$V_{DS}=48V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	6.4		$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	$V_{DD}=30V$
t_r	Rise Time	—	110	—		$I_D=10A$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G=12\Omega$
t_f	Fall Time	—	26	—		$R_D=2.8\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	400	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	170	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	42	—		$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	14		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}$, $I_S=1.7A$, $V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	93	130	ns	$T_J=25^\circ\text{C}$, $I_F=10A$
Q_{rr}	Reverse Recovery Charge	—	0.34	0.65	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=25V$, starting $T_J=25^\circ\text{C}$, $L=197mH$
 $R_G=25\Omega$, $I_{AS}=1.7A$ (See Figure 12)
- ③ $I_{SD}\leq 10A$, $di/dt\leq 90A/\mu s$, $V_{DD}\leq V_{(BR)DSS}$,
 $T_J\leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



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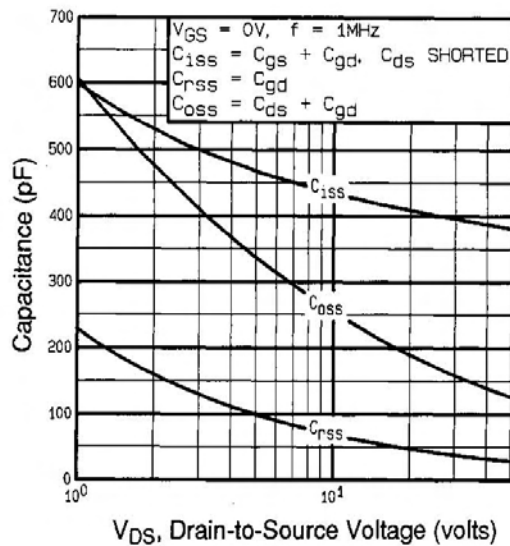


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

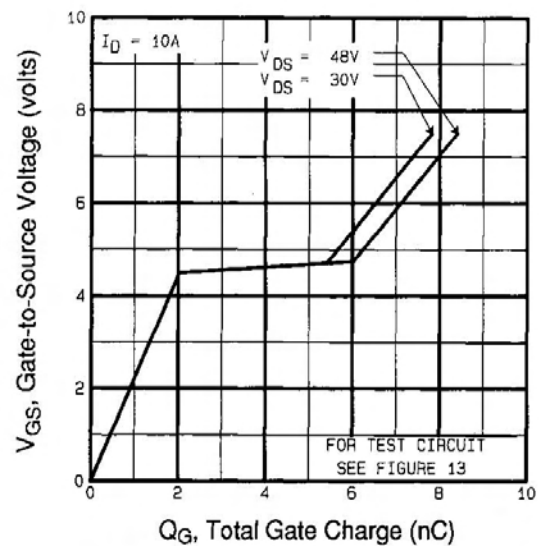


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

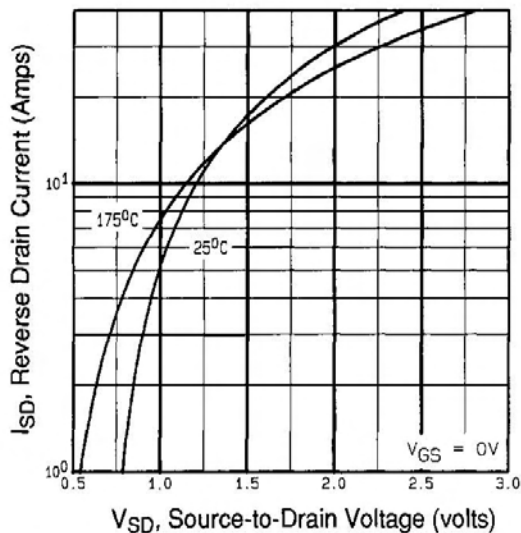


Fig 7. Typical Source-Drain Diode Forward Voltage

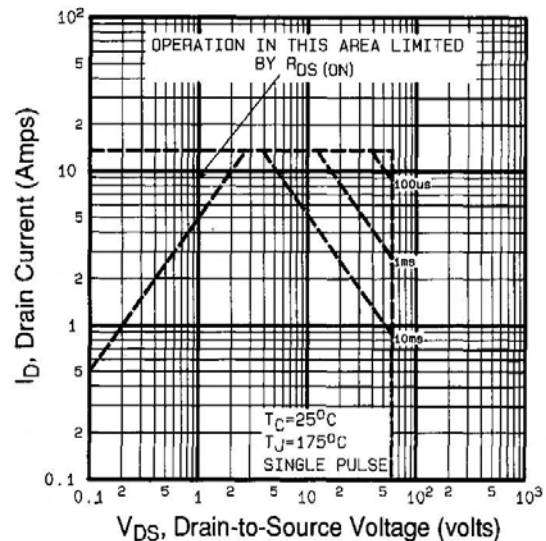


Fig 8. Maximum Safe Operating Area

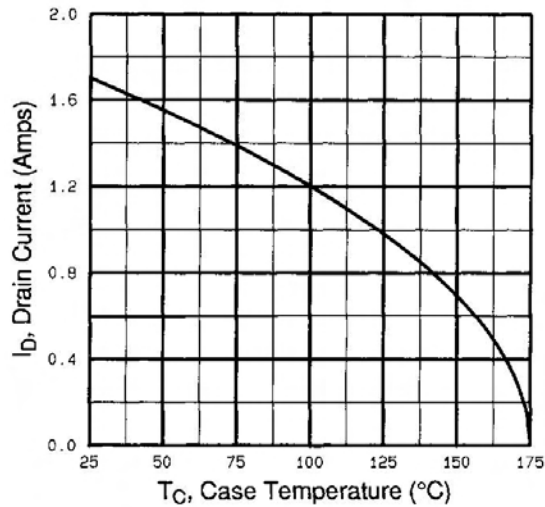


Fig 9. Maximum Drain Current Vs. Case Temperature

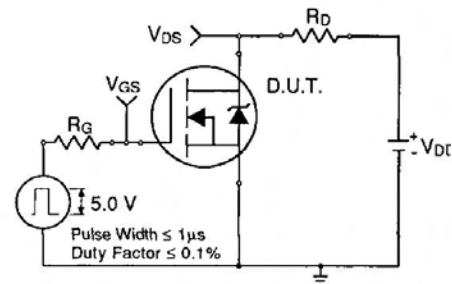


Fig 10a. Switching Time Test Circuit

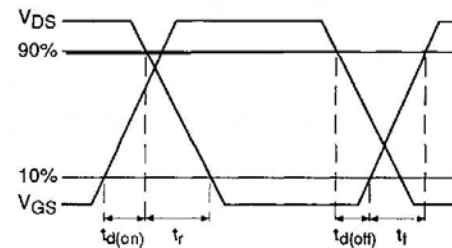


Fig 10b. Switching Time Waveforms

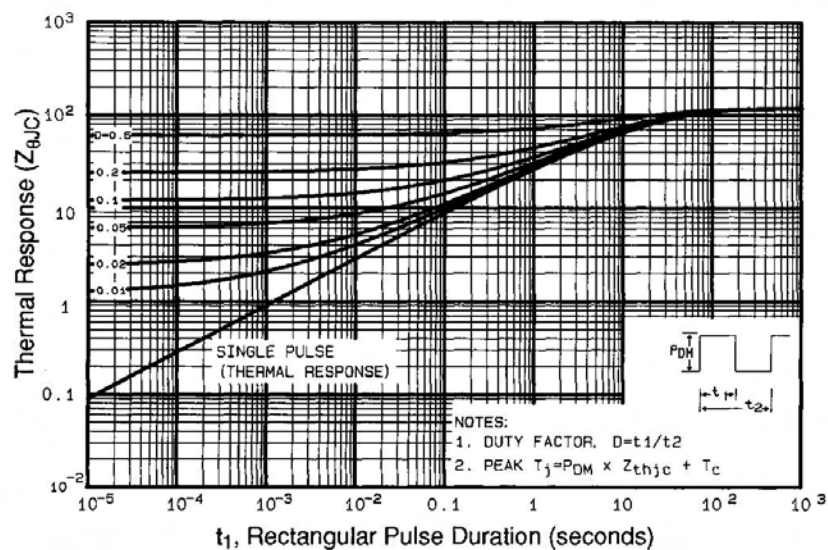


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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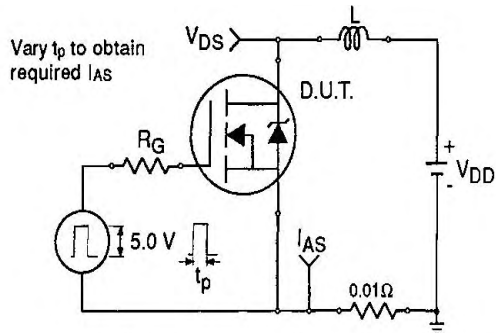


Fig 12a. Unclamped Inductive Test Circuit

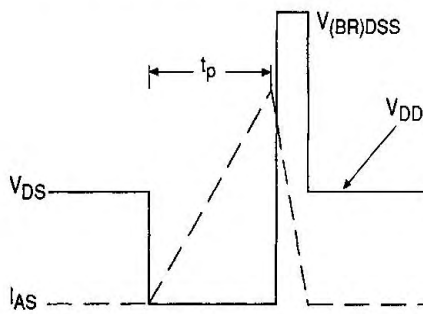


Fig 12b. Unclamped Inductive Waveforms

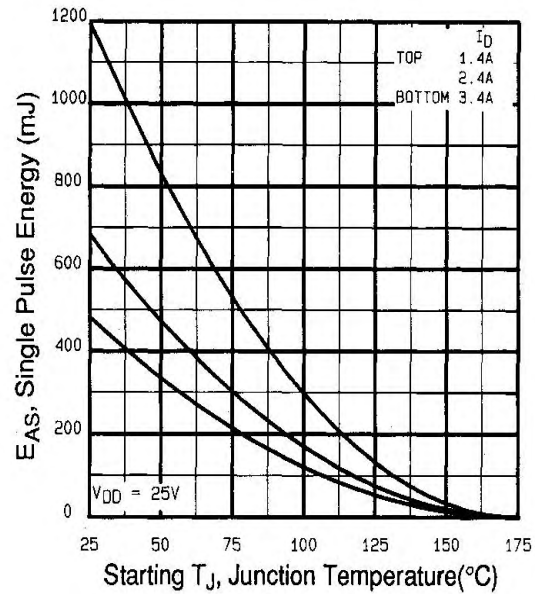


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

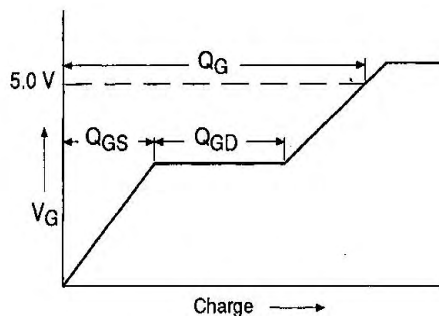


Fig 13a. Basic Gate Charge Waveform

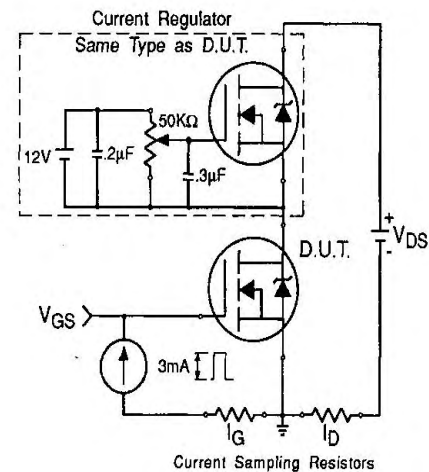
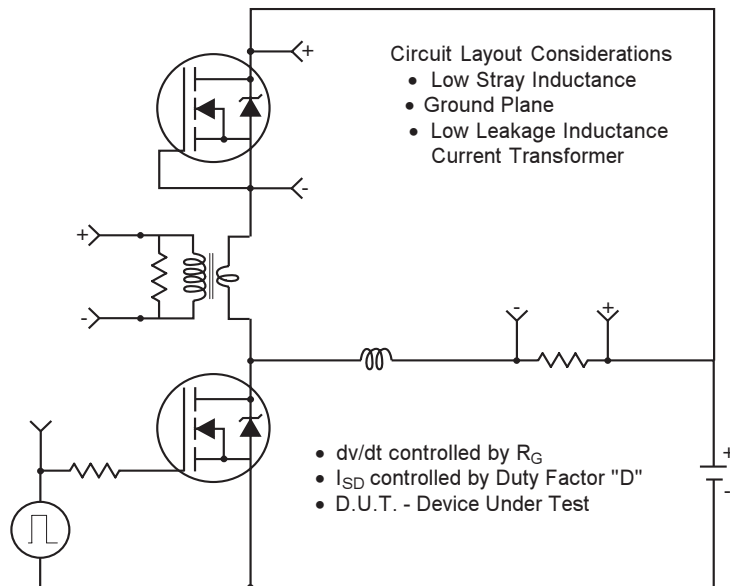


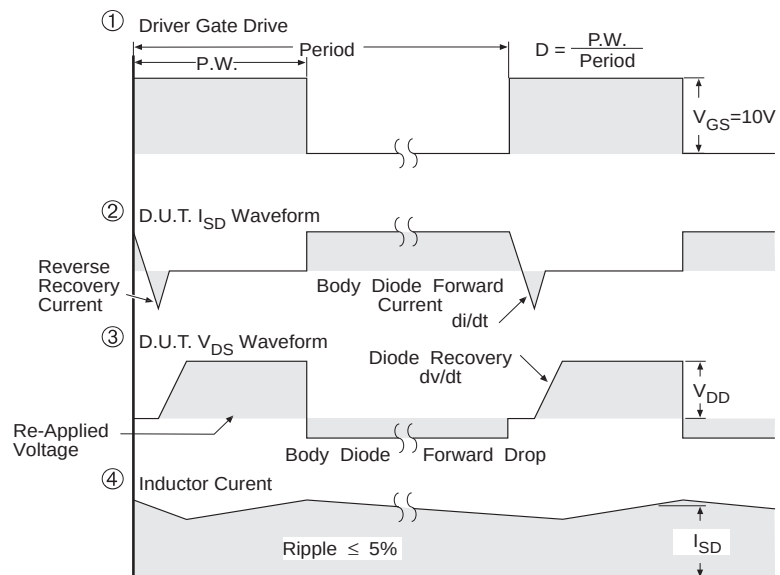
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



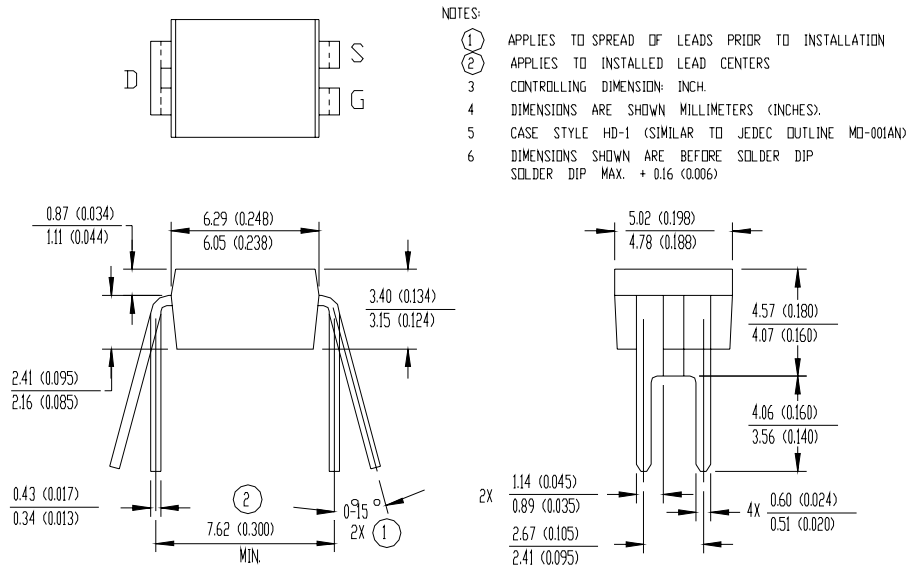
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

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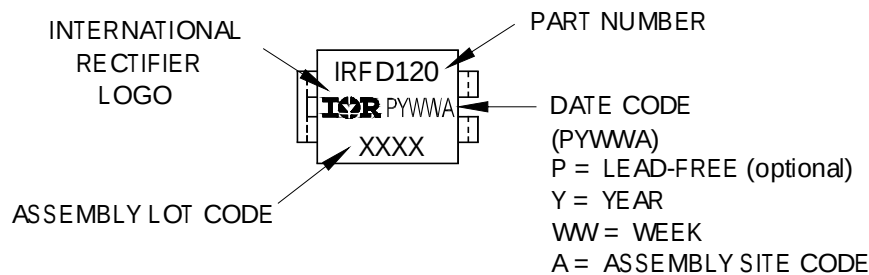
Hexdip Package Outline

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Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



Data and specifications subject to change without notice.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
12/04



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