User Manual for

TL7218X Development Board

UM-TL7218X-E2

Ver 1.0.1

2025/12/02

Keyword

TL7218X, Bluetooth® LE, Zigbee, Thread, Matter, 2.4 GHz

Brief

This document is the development board user manual of Telink multi-standard wireless SoC TL7218X. It mainly introduces the development board block diagram, development board features, various peripheral interfaces and detailed function descriptions.

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Revision History

Version	Change Description
1.0.0	Initial release.
1.0.1	Updated TL_Key1 connection in Table 1-4, added footnote for PD4 in Table 2-5, updated links in Table 3-1.

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1 Overview

The TL7218X development board is designed based on the TL7218X chip and is used to verify the TL721x series chips. It can be used to verify the following chips:

- TL7218A
- TL7218D
- TL7218H
- TL7218J
- TL7215A
- TL7215D

The TL7218X is a wireless SoC for Bluetooth LE 6.0, 802.15.4 and 2.4 GHz proprietary. This chip supports industrial alliance standards including Bluetooth LE, Zigbee, Thread, Matter and 2.4GHz proprietary standard.

This development board supports testing of various functions, such as RF conduction test, current test, audio input and output test, combination of lights and buttons, and so on.

This document provides a detailed description of the TL7218X development board's interfaces, power supply, debugging methods, audio sockets, buttons, lights, jumpers, and others to make it easy for users to familiarize with this board and use it for subsequent development and debugging.

1.1 Block Diagram

The top and bottom view of the TL7218X development board are shown as below.

Figure 1-1 Top view of TL7218X development board

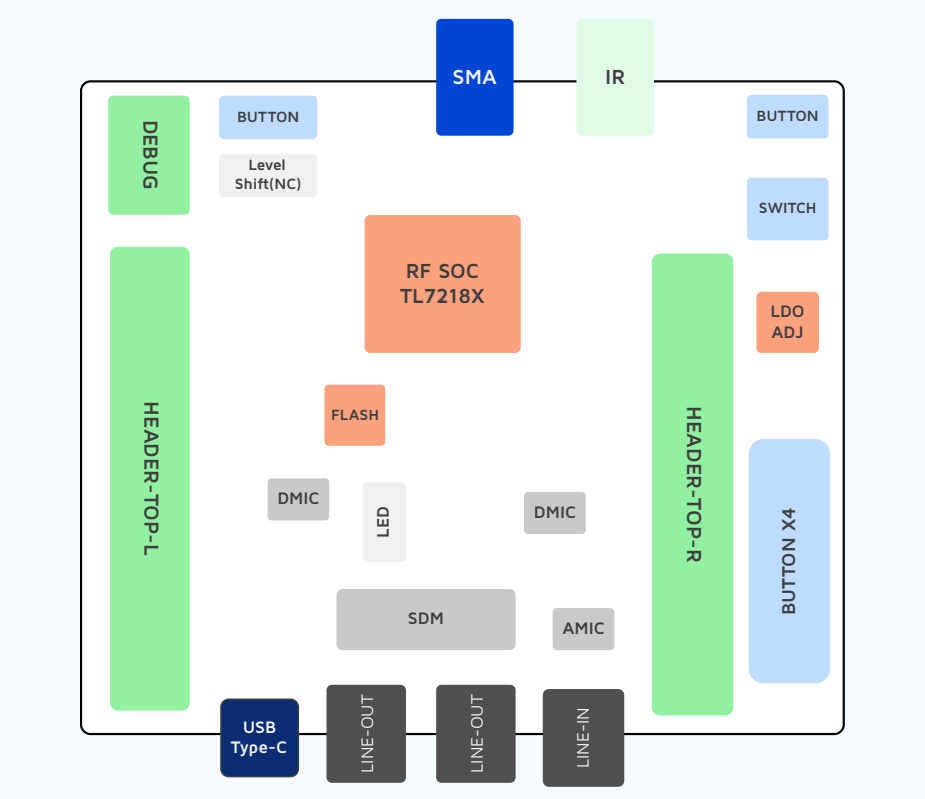
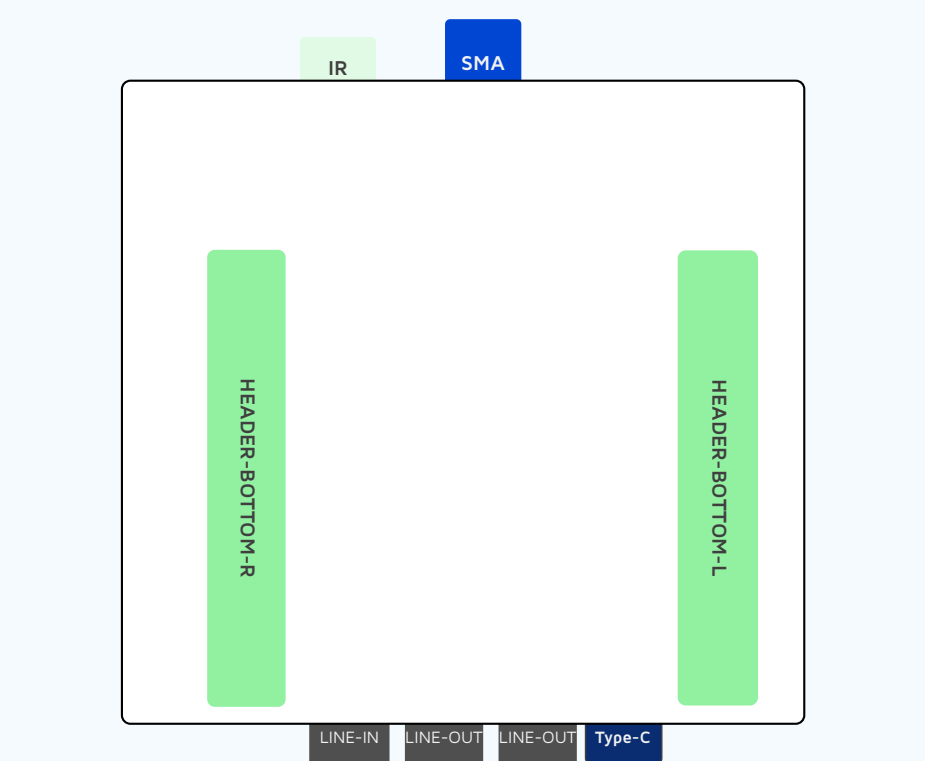


Figure 1-2 Bottom view of TL7218X development board



1.2 Board Features

The following table lists the features of the TL7218X development board.

Table 1-1 Board Features

No.	Name	Description	Reference section
1	Current test interface	Total current test and each branch current test via jumper combinations	2.3 Current Measurement
2	RF interface	RF conduction test via SMA connector	2.4 RF Test
3	Debug interface	Supports 2-wire and 4-wire JTAG interface Supports Full-speed USB interface	2.2 Debug Interface
4	GPIO interface	Supports flexible connection of all GPIOs	2.5 GPIO Interface
5	Peripheral interface	Supports peripherals such as buttons, LEDs, external flash, DMIC, AMIC, etc.	2.6 Peripheral Interface - USB Type-C 2.7 Peripheral Interface - 32.768KHz Crystal 2.8 Peripheral Interface - DMIC 2.9 Peripheral Interface - Flash 2.10 Peripheral Interface - IR
6	Uplink interface	Supports single-ended uplink testing	2.11 Uplink Interface
7	Downlink interface	Supports SDM differential downlink testing	2.12 Downlink Interface

1.3 Kit List

The following table lists the main materials in this development kit.

Table 1-2 Kit List

No.	Name	Quantity
1	TL7218X development board	1
2	Whip antenna	1
3	USB 2.0 Type-A to Type-C cable	1

1.4 Board Pictures

The following picture shows the default state of the board for user verification.

Figure 1-3 Top view of the real board

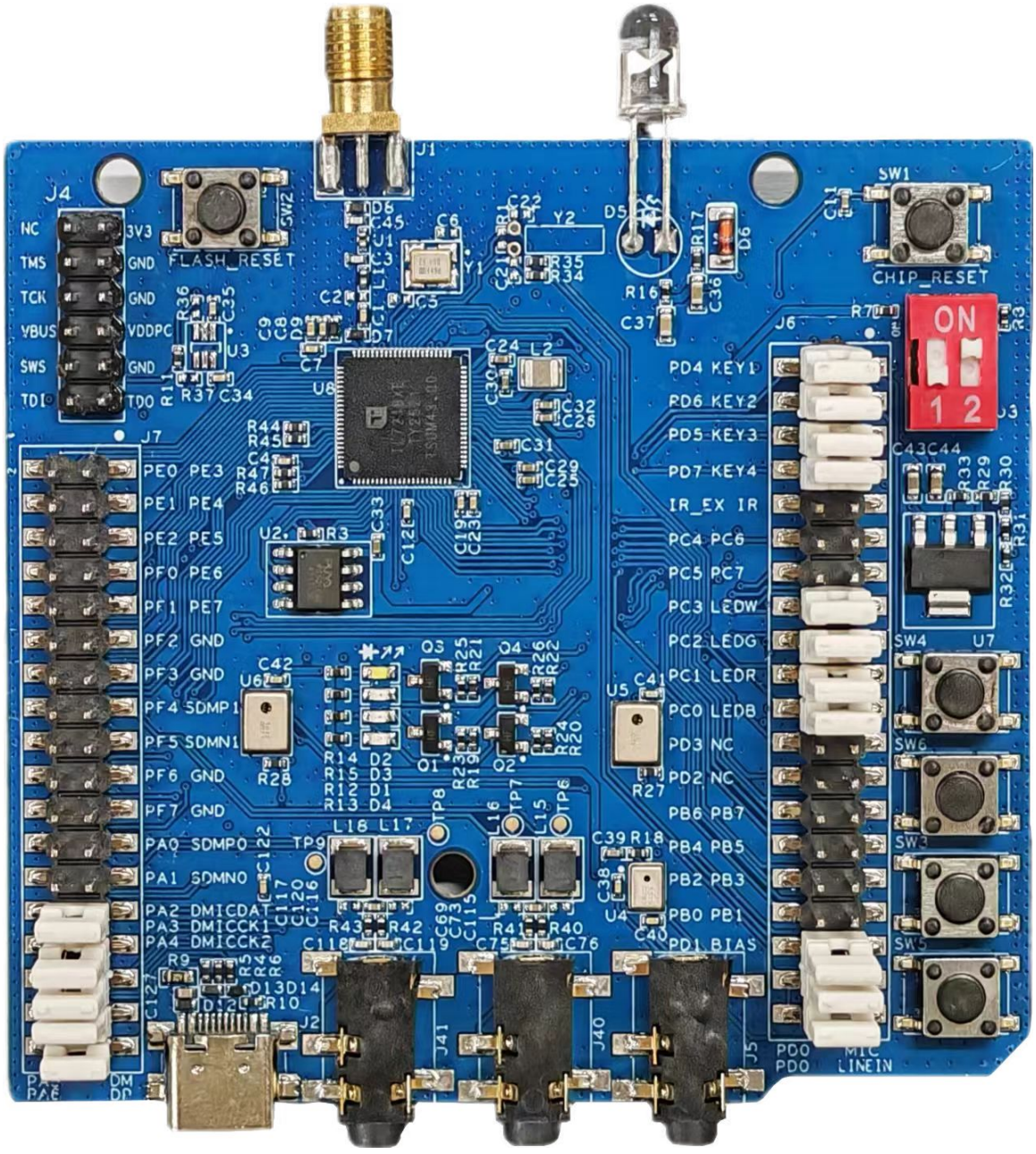
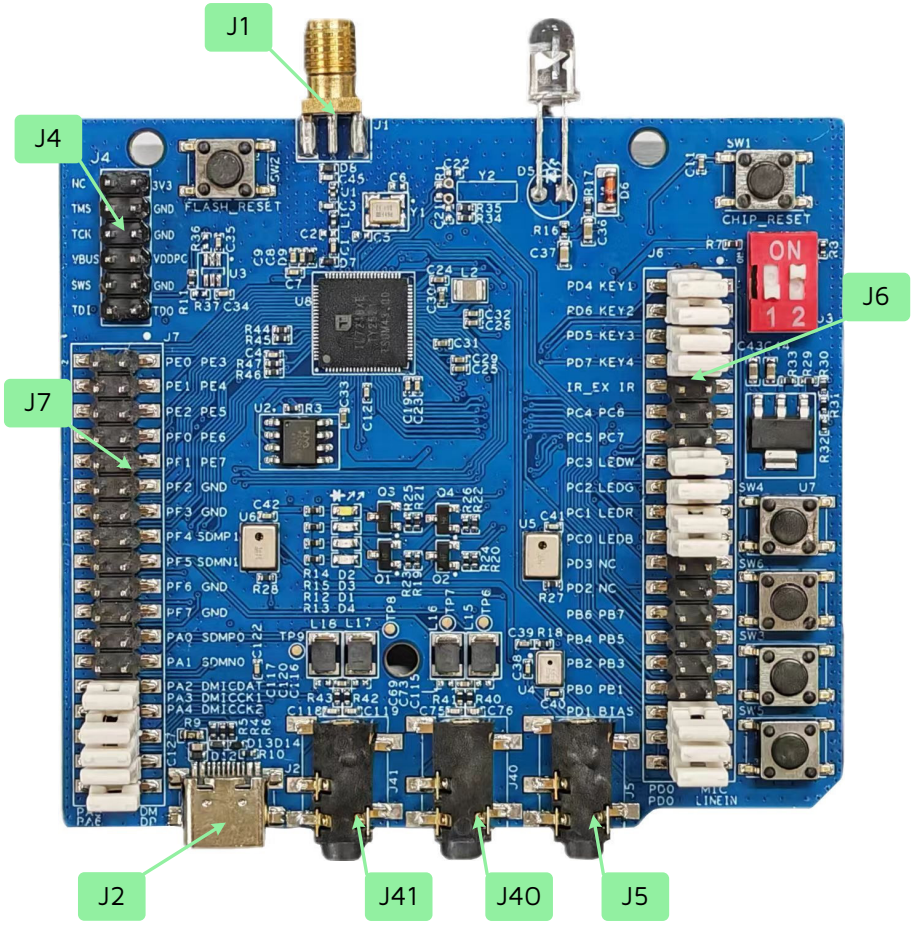


Figure 1-4 Bottom view of the real board

1.5 Connectors

The following figure identifies the connectors such as jumpers and sockets on the top of the development board.

Figure 1-5 Connectors on top of the board



The following table lists the connectors on the top of the development board.

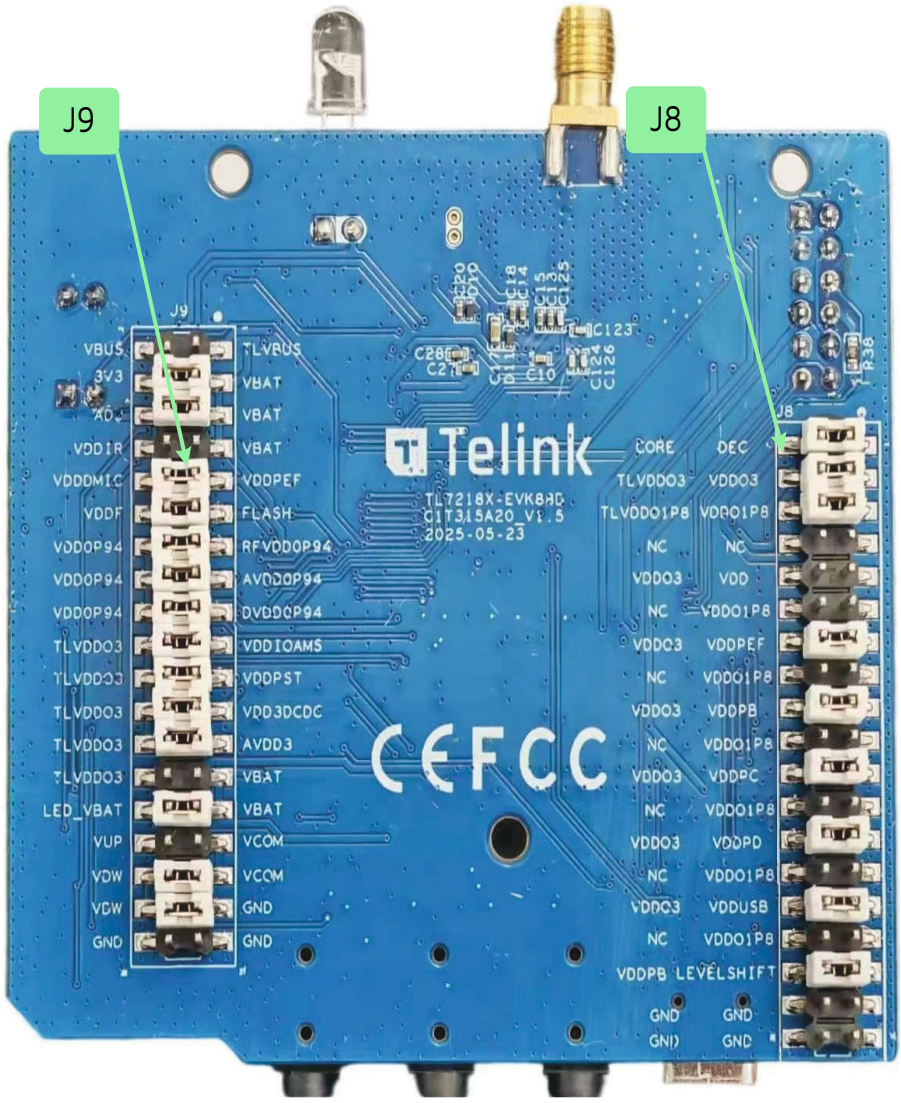
Table 1-3 List of Connectors on board top

No.	Ref. Des.	Connector type	Description	Reference section
1	J4	2x6-pin header	JTAG and single wire connector	2.2 Debug Interface
2	J6	2x20-pin header	GPIO connector	2.5 GPIO Interface
3	J7	2x18-pin header	GPIO connector	2.5 GPIO Interface
4	J2	USB Type-C	Full-speed USB connector	2.6 Peripheral Interface - USB Type-C
5	J1	SMA female connector	RF connector	2.4 RF Test
6	J5	3.5mm jack	Uplink connector	2.11 Uplink Interface

No.	Ref. Des.	Connector type	Description	Reference section
7	J40/J41	3.5mm jack	Downlink connector	2.12 Downlink Interface

The following figure identifies the connectors such as jumpers and sockets on the bottom of the development board.

Figure 1-6 Connectors on bottom of the board



The following table lists the connectors on the bottom of the development board.

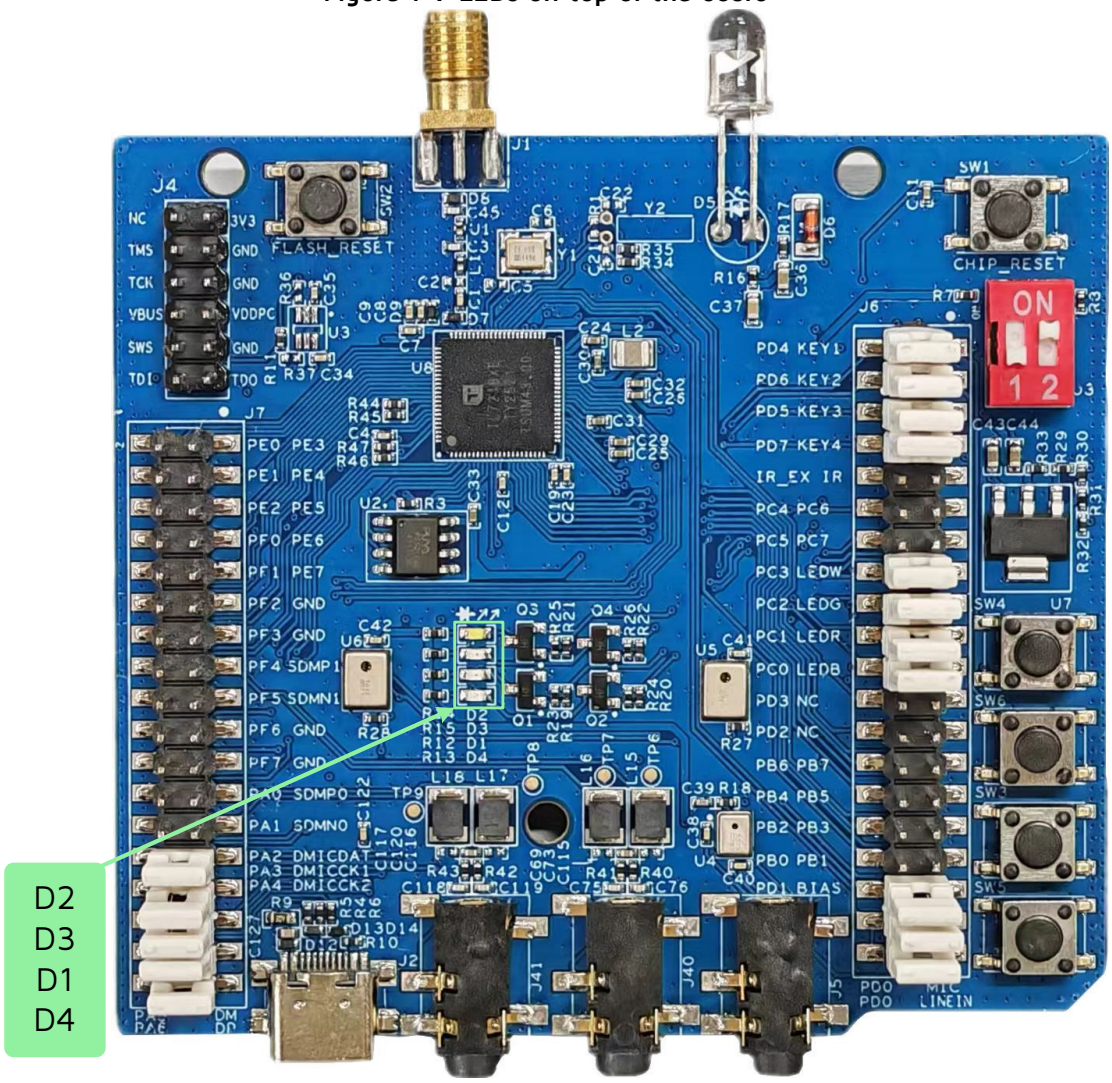
Table 1-4 List of connectors on board bottom

No.	Ref. Des.	Connector type	Description	Reference section
1	J8	2x19-pin header	Connector for current test	2.3 Current Measurement
2	J9	2x19-pin header	Connector for current test	2.3 Current Measurement

1.6 LED

The following figure identifies the LEDs on the top of the development board.

Figure 1-7 LEDs on top of the board



The following table lists the LEDs on the top of the board.

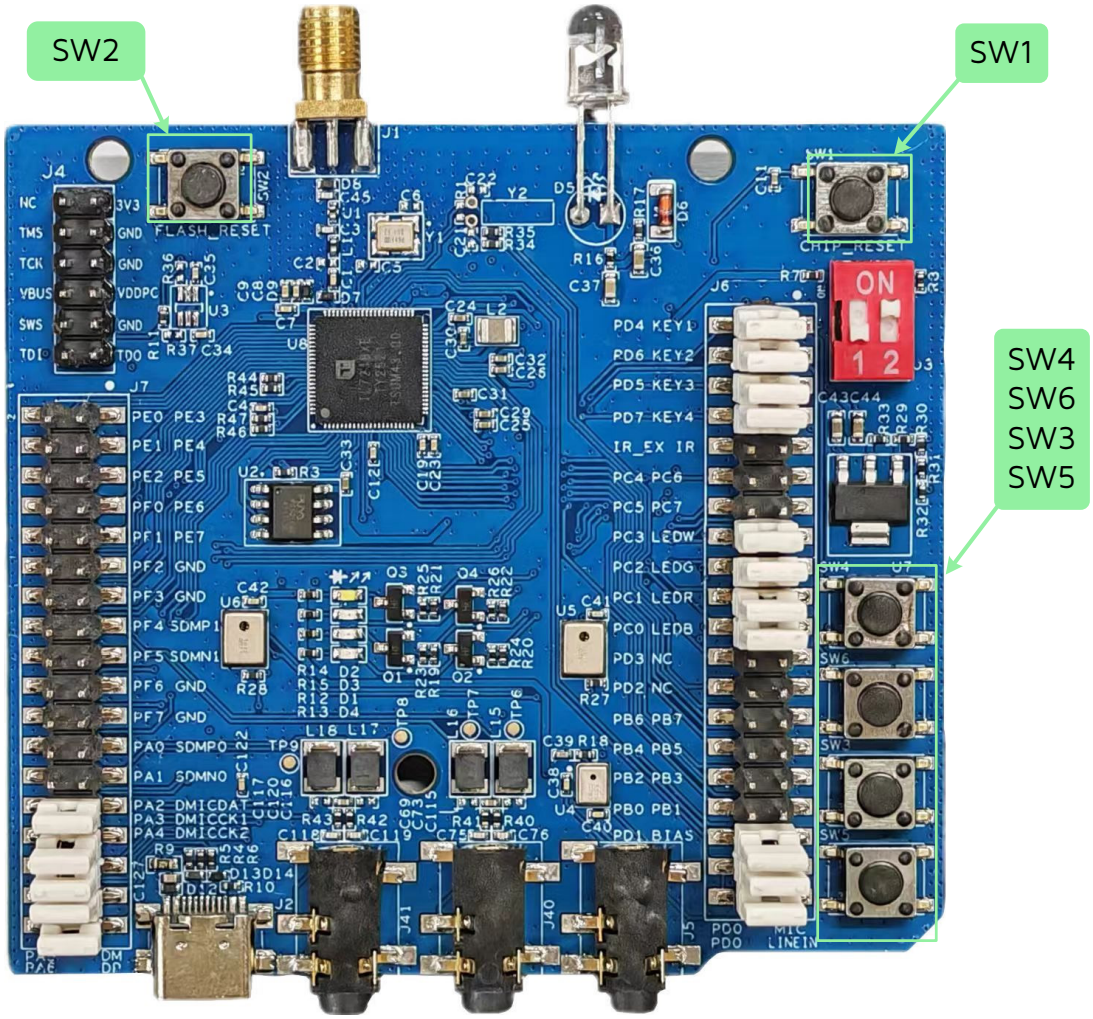
Table 1-5 LEDs on board top

No.	Ref. Des.	LED color	Description
1	D1	Red	(1) PC1 of TL7218X connects to PIN20 of J6. (2) PIN20 of J6 connects to PIN19 via jumper by default (3) PIN19 of J6 controls the switching and brightness of D1 by controlling transistor Q1. (4) If you want to use another GPIO of the TL7218X to control D1, remove this jumper and connect PIN19 of J6 to the other GPIO you want to use. (5) Power of D1 is supplied by connecting J9's Pin29 and Pin30 via a jumper.
2	D2	White	(1) PC3 of TL7218X connects to PIN16 of J6. (2) PIN16 of J6 connects to PIN15 via jumper by default. (3) PIN15 of J6 controls the switching and brightness of D2 by controlling transistor Q3. (4) If you want to use another GPIO of the TL7218X to control D2, remove this jumper and connect PIN15 of J6 to the other GPIO you want to use. (5) Power of D2 is supplied by connecting J9's Pin29 and Pin30 via a jumper.
3	D3	Green	(1) PC2 of TL7218X connects to PIN18 of J6. (2) PIN18 of J6 connects to PIN17 via jumper by default. (3) PIN17 of J6 controls the switching and brightness of D3 by controlling transistor Q4. (4) If you want to use another GPIO of the TL7218X to control D3, remove this jumper and connect PIN17 of J6 to the other GPIO you want to use. (5) Power of D3 is supplied by connecting J9's Pin29 and Pin30 via a jumper.
4	D4	Blue	(1) PC0 of TL7218X connects to PIN22 of J6. (2) PIN22 of J6 connects to PIN21 via jumper by default. (3) PIN21 of J6 controls the switching and brightness of D4 by controlling transistor Q2. (4) If you want to use another GPIO of the TL7218X to control D4, remove this jumper and connect PIN21 of J6 to the other GPIO you want to use. (5) Power of D4 is supplied by connecting J9's Pin29 and Pin30 via a jumper.

1.7 Button

The following figure identifies the Buttons on the top of the development board.

Figure 1-8 Buttons on top of the board



The following table lists the buttons on the top of the board.

Table 1-6 List of buttons on the board top

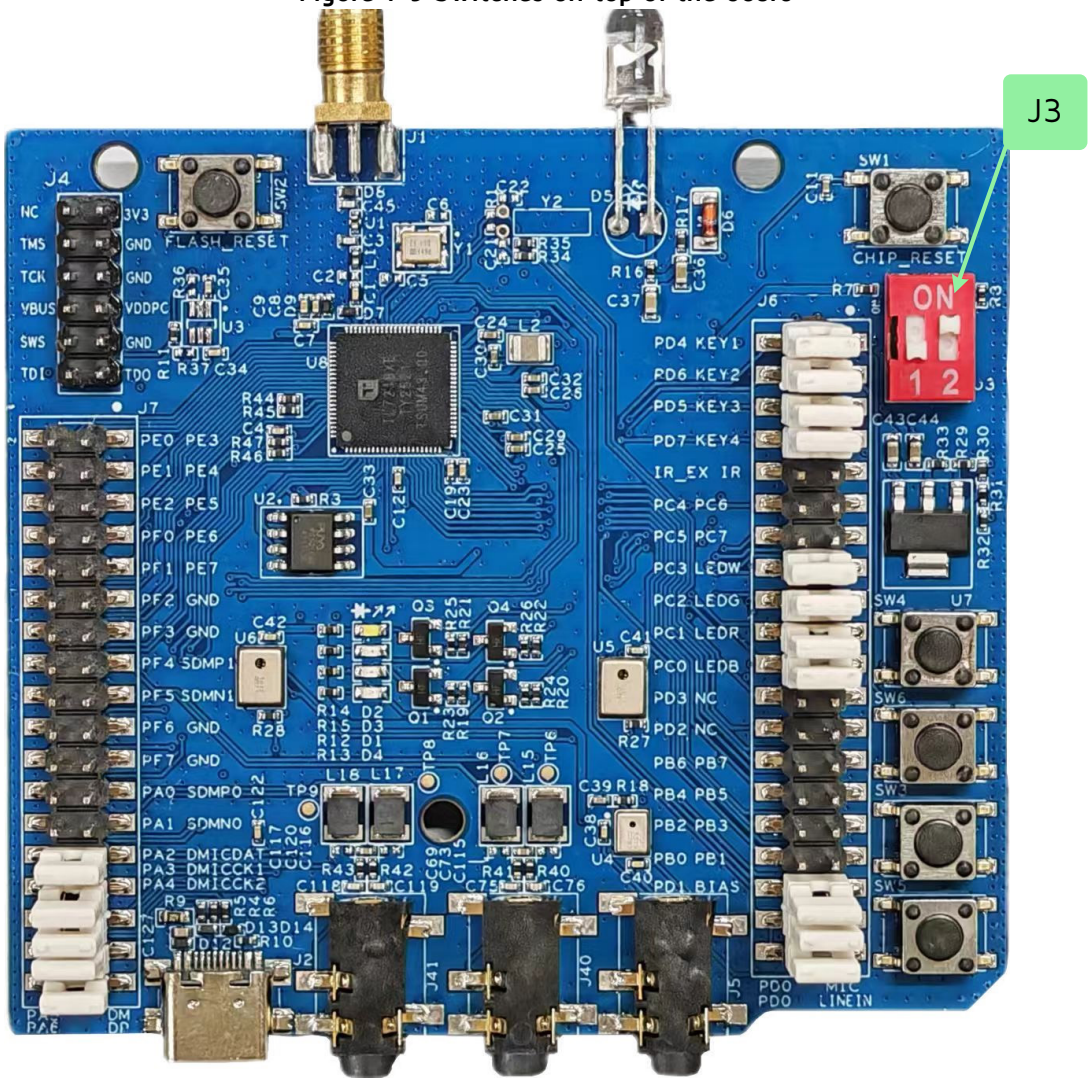
No.	Ref. Des.	Function	Description
1	SW1	Chip reset	Press SW1 to reset the main chip
2	SW2	Flash reset	Press SW2 to reset the flash

No.	Ref. Des.	Function	Description
3	SW3, SW4, SW5, SW6	–	(1) SW3, SW4, SW5 and SW6 form a 2x2 key matrix. (2) SW3's two end networks are TL_Key1 and TL_Key3 respectively. (3) SW4's two end networks are TL_Key1 and TL_Key4 respectively. (4) SW5's two end networks are TL_Key2 and TL_Key3 respectively. (5) SW6's two end networks are TL_Key2 and TL_Key4 respectively. (6) TL_Key1 is sourced as follows: a) PB7 of TL7218X connects to PIN27 of J6. b) PIN1 of J6 is shorted to PIN2 via a jumper by default, remove this jumper, use a wire to connect PIN1 of J6 and PB7 of TL7218X. c) PIN1 of J6 is connected to one end of SW3 and SW4 with the network name TL_Key1. (7) TL_Key2 is sourced as follows: a) PD6 of TL7218X connects to PIN4 of J6. b) PIN4 of J6 is shorted to PIN3 via a jumper by default. c) PIN3 of J6 is connected to one end of SW5 and SW6 with the network name TL_Key2. (8) TL_Key3 is sourced as follows: a) PD5 of TL7218X connects to PIN6 of J6. b) PIN6 of J6 is shorted to PIN5 via a jumper by default. c) PIN5 of J6 is connected to one end of SW3 and SW5 with the network name TL_Key3. (9) TL_Key4 is sourced as follows: a) PD7 of TL7218X connects to PIN8 of J6. b) PIN8 of J6 is shorted to PIN7 via a jumper by default. c) PIN7 of J6 is connected to one end of SW4 and SW6 with the network name TL_Key4. (10) If you want to use another GPIO of the TL7218X to control the keys, remove the corresponding jumper and connect PIN 1/3/5/7 of J6 to the other GPIO you want to use.

1.8 Switch

The following figure identifies the switches on the top of the development board.

Figure 1-9 Switches on top of the board



The following table lists the switch functions on the top of the board.

Table 1-7 List of switches on board top

No.	Ref. Des.	Function	Description
1	J3	JTAG mode selection	(1) PB0 of the TL7218X determines the JTAG work mode. a) When PB0 is high, JTAG supports 2-wire mode. b) When PB0 is low, JTAG supports 4-wire mode. (2) J3 shorts PIN1 and PIN2 by default, when PB0 is low, JTAG supports 4-wire mode by default.

2 Function Description

2.1 Power Supply

The TL7218X development board can be powered by the following ways:

- 5V via the USB Type-C port and converted to 3.3V through LDO U7 for regulated power supply;
- 5V via the USB Type-C port or J4 PIN8 to directly power the chip (J9 PIN27 and PIN28 need to be shorted through a jumper)
- Access 1.8V ~ 4.3V through J4 PIN1 interface, J4 PIN1 is connected to J9 PIN4 in hardware, by default J9 PIN3 and PIN4 are shorted through a jumper, J9 PIN3 provides voltage to U8 PIN47 VBAT pin.

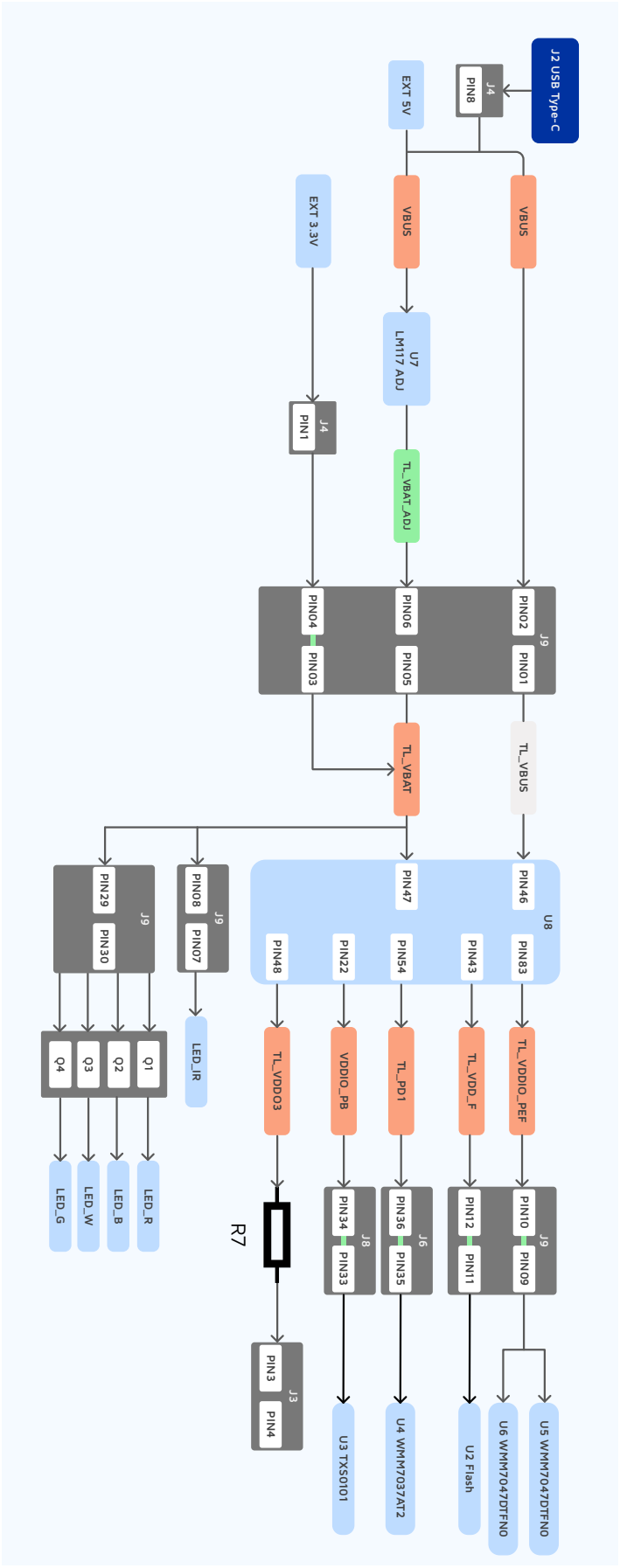
The following table lists the power path of the chip.

Table 2-1 Power supply of the chip

No.	Power source	Power supply	Description
1	External power via USB Type-C J2	VBUS to VBAT	The external power provides 5V to U7, and at the same time select the 4-step voltage (default is 3.8V) through J9 PIN29 ~ PIN34, and then provide TL_VBAT through J9 PIN6 to PIN47 of U8. This pin is the voltage input pin of the chip.
2	External power via USB Type-C J2	VBUS	(1) Directly supply 5V to the chip, short J9 PIN1 - PIN2 to select this mode. (2) Short J9 PIN27 - PIN28 when selecting this mode, other modes do not need to short this jumper
3	External power via connector J4	TL_VBAT	(1) Unplug the jumper between J9 PIN5 and PIN6, and short J9 PIN3 and PIN4 through a jumper. (2) Apply 1.8V ~ 4.3V to J4 PIN1, this directly provides TL_VBAT to U8 PIN47. This pin is the only power supply input for the chip.

The following figure shows the power supply path of the main power sources.

Figure 2-1 Power supply path



2.2 Debug Interface

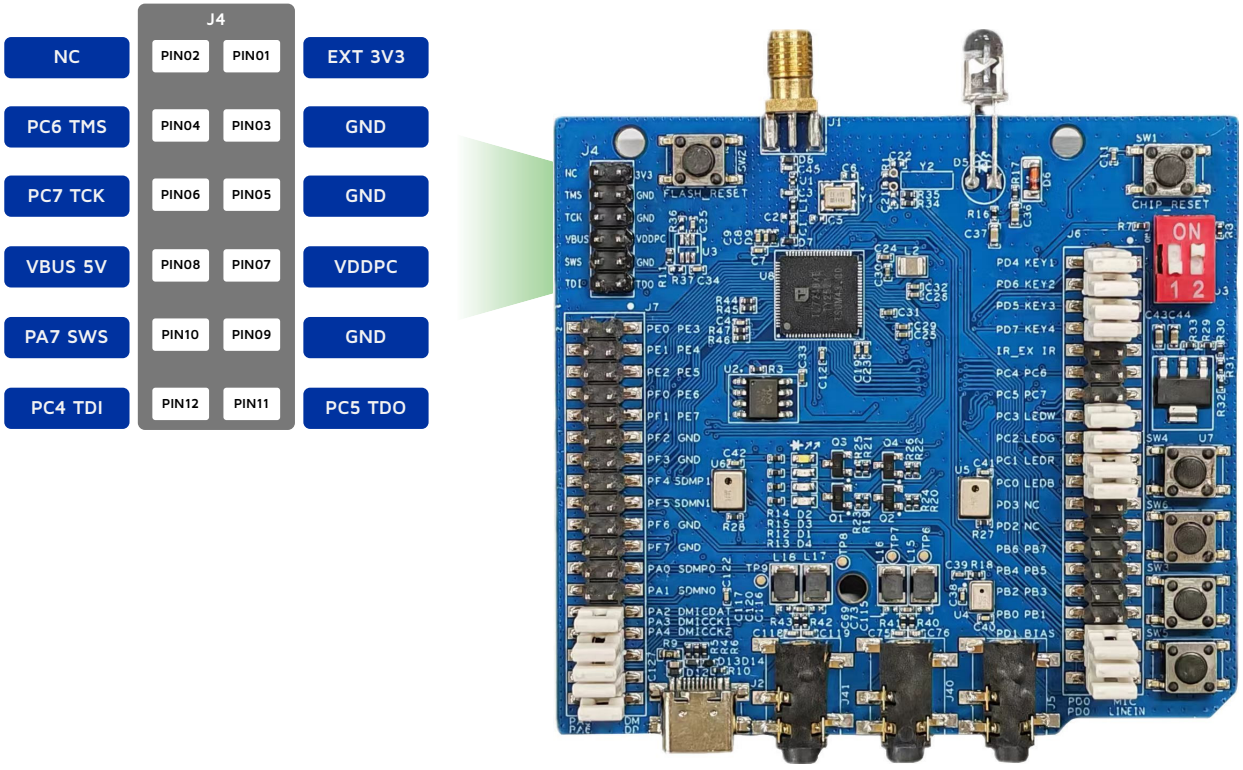
The TL7218X development board supports the following two debug methods.

Table 2-2 Debug methods

No.	Debug method	Connector	Description
1	JTAG	J4	(1) Power up the TL7218X development board. (2) J4 supports 4-wire JTAG function • U8.PIN32.PC4 to J4.PIN12 - TDI • U8.PIN33.PC5 to J4.PIN11 - TDO • U8.PIN35.PC7 to J4.PIN06 - TCK • U8.PIN34.PC6 to J4.PIN04 - TMS
2	Single Wire		(1) Power up the TL7218X development board. (2) J4 supports Telink proprietary debug protocol, single wire. • U8.PIN13.PA7 to J4.PIN10 - SWS (3) Connect the SWM of the burner with this SWS. (4) The SWS connects U8.PIN13 of the chip via R11(or U3 the level shifter).

The following figure shows the details of each J4 pins.

Figure 2-2 Debug interfaces on the board



2.3 Current Measurement

The methods to measure the current of each pin of TL7218X development board are provided as follows.

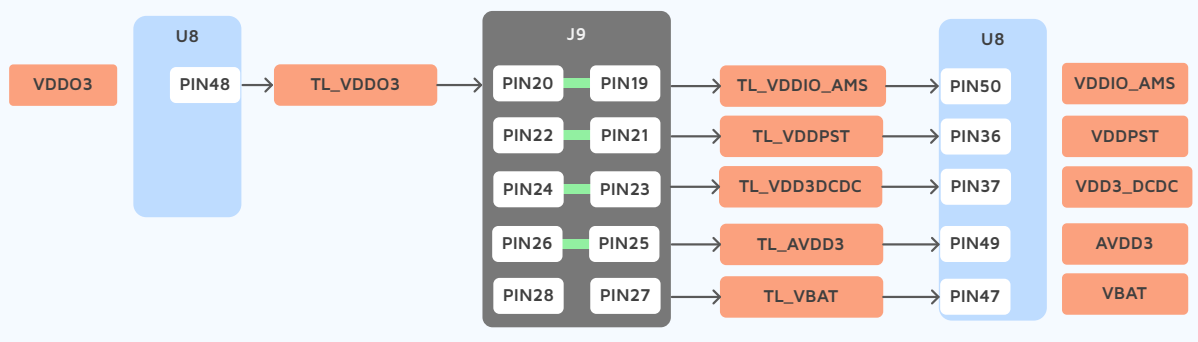
Table 2-3 Current measurement method of the board

No.	Test item	Power supply	Description
1	Total current of the chip	TL_VBAT	(1) The main power supply of the chip is U8 PIN47. (2) When using the above method 1 power supply, pull out the jumper between J9 PIN5 and PIN6, and connect in series the ammeter, at this time the total chip current can be measured. (3) When using the above method 2 power supply, connect in series an ammeter between J9 PIN3 and PIN4, and the total chip current can be measured. (4) Make sure that there is no external power consumption and no GPIO external current (including JTAG and SWS), so as to avoid high chip current. (5) Details refer to Figure 2-1.
2	3V3 branch current of the chip	TL_VDDO3 TL_VDDIO_AMS TL_VDDPST TL_VDD3DCDC TL_AVDD3	(1) The U8 PIN47 generates 3V3 branch voltage when the chip is connected to 1.8V~4.3V. (2) The U8 PIN48 is the 3V3 branch voltage output source. (3) The U8 PIN48 and U8 PIN36/PIN37/PIN49/PIN50 are shorted together through J9's PIN21-PIN22, PIN23-PIN24, PIN25-PIN26, and PIN19-PIN20 to supply power to the chip. (4) The J8 PIN3-PIN4 is used as a source of power supply to the chip IO ports, pull out the jumper between J8 PIN3-PIN4, connect in series the ammeter, then test the total current of the chip IO port in the 3.3V voltage domain. (5) The U8 PIN48 shorted through J8's PIN13-PIN14, PIN17-PIN18, PIN21-PIN22, PIN25-PIN26, can provide 3.3V IO port voltage to U8 PIN 83 (VDDIO_PEF), PIN22 (VDDIO_PB), PIN23 (VDDIO_PC), PIN59 (VDDIO_PD), and can test the power supply current of different IO groups by connecting in series an ammeter between the jumpers, respectively.

No.	Test item	Power supply	Description
3	0V94 branch current of the chip	TL_VDD0P94 TL_RFVDD_0P94 TL_AVDD0P94 TL_DVDD0P94	(1) The U8 PIN47 generates 0V94 branch voltage when the chip is connected to 1.8V~4.3V voltage. (2) The U8 PIN40 is the 0V94 branch voltage output source. (3) The U8 PIN40 and U8 PIN41/PIN42/PIN65 are shorted together through J9 PIN15-PIN16, PIN17-PIN18, and PIN13-PIN14, respectively, and supply power to the digital module (PIN41), analog module (PIN42), and RF module (PIN65), respectively. (4) The 0V94 power branch supplies power to the RF part, considering the high efficiency of the DCDC, the application of this path power supply is usually configured as 0.94V DCDC mode. (5) Unplug the jumper between J9 PIN13 and PIN14, connect in series an ammeter, and the RF operating current can be tested.
4	1V8 branch current of the chip	TL_VDDO1P8 TL_VDDF	(1) The U8 PIN47 generates a 1V8 branch voltage when the chip is connected to a 1.8V~4.3V voltage. (2) The U8 PIN28 is the 1V8 branch voltage output source from a separate internal LDO. (3) The J8 PIN5-PIN6 is used as a source of power supply to the chip IO, unplug the jumper between J8 PIN5 and PIN6, connect in series an ammeter, the total current of the chip IO port in the 1.8V voltage domain can be tested. (4) U8 PIN28 shorted through J8 PIN13-PIN15, PIN17-PIN19, PIN21-PIN25, PIN25-PIN27, provide 1.8V IO port voltage to U8 PIN 83 (VDDIO_PEF), PIN22 (VDDIO_PB), PIN23 (VDDIO_PC), PIN59 (VDDIO_PD), and the power supply current of different IO groups can be tested by connecting in series an ammeter between the jumpers, respectively.
5	1V8 branch current inside the chip	TL_VDDF	(1) The U8 PIN47 generates internal 1V8 branch voltage when it is connected to 1.8V~4.3V. (2) The U8 PIN43 is the internal 1V8 branch voltage output to external flash power supply source. (3) The internal 1V8 branch of the chip is used to supply power to the codec and Flash inside the chip. (4) The 1V8 branch of the chip can be configured in DCDC mode and LDO mode, and in DCDC mode, it shares the same inductor with 0v94. (5) Unplug the jumper between J9 PIN11 and PIN12, and connect in series an ammeter, the Flash working current can be tested.

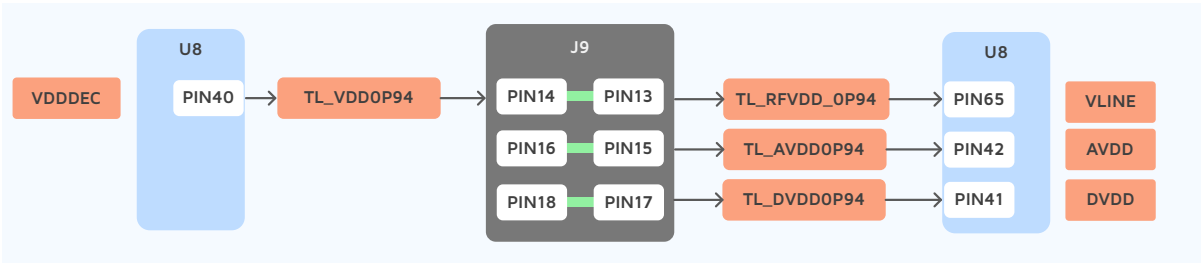
The following figures shows the connection of 3V3 branch of the chip.

Figure 2-3 The 3V3 branch of the chip



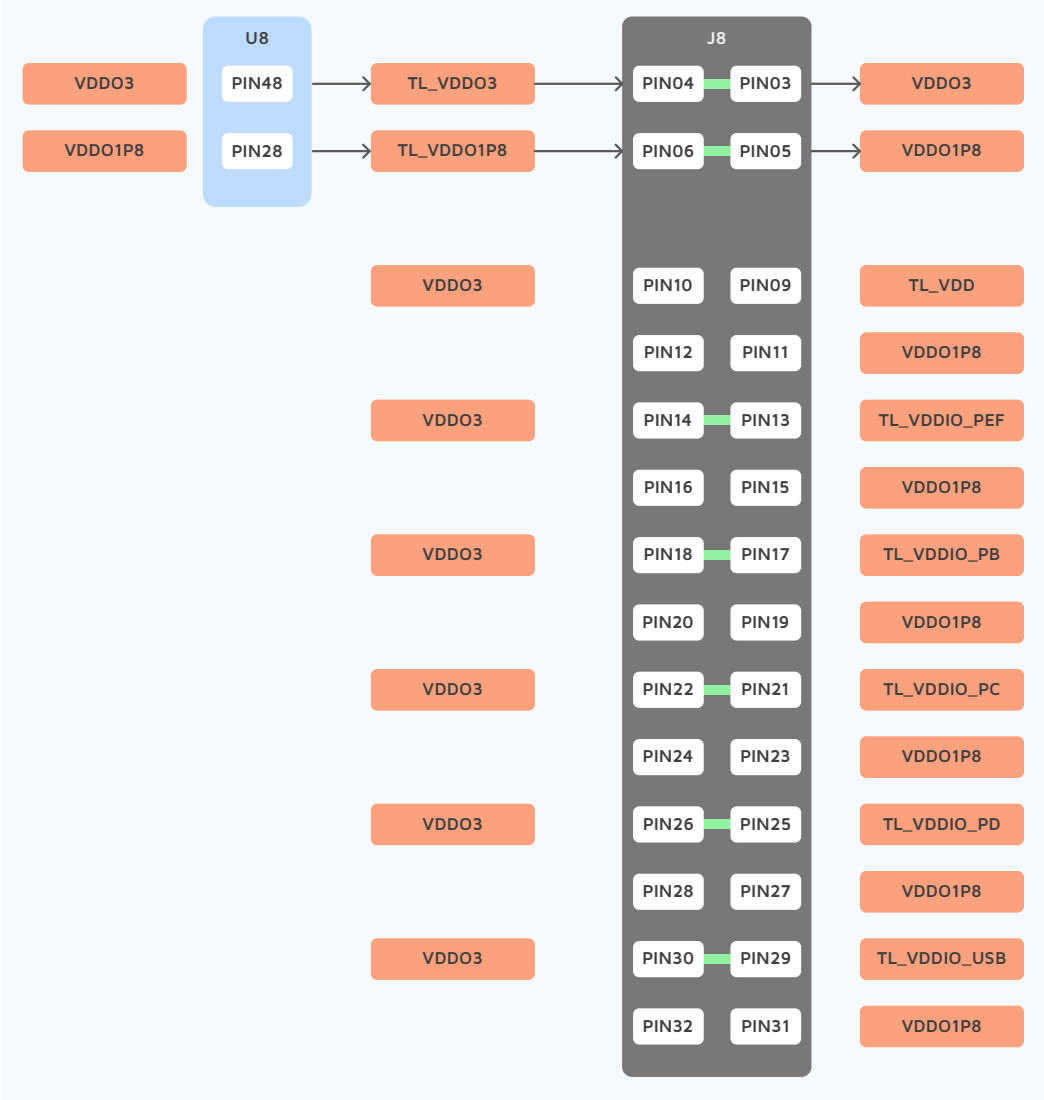
The following figures shows the connection of 0V94 branch of the chip

Figure 2-4 The 0V94 branch of the chip



The following figure shows the IO voltage domain configuration of the chip.

Figure 2-5 The IO voltage domain configuration of the chip



2.4 RF Test

The methods for conducting and radiating tests on RF of TL7218X development board are provided.

The following table lists the methods of RF test.

Table 2-4 RF test method

No.	Test item	Connector	Description
1	RF test	J1	(1) Power up the TL7218X development board normally. (2) RF conduction test: connect the J1 SMA connector to the test instrument to perform RF conduction test. (3) RF radiation test: connect the whip antenna in the kit to the J1 SMA connector to perform RF radiation test.

2.5 GPIO Interface

On the TL7218X development board, all GPIOs are connected to the connectors for easy access.

The following table lists the connections of all GPIO.

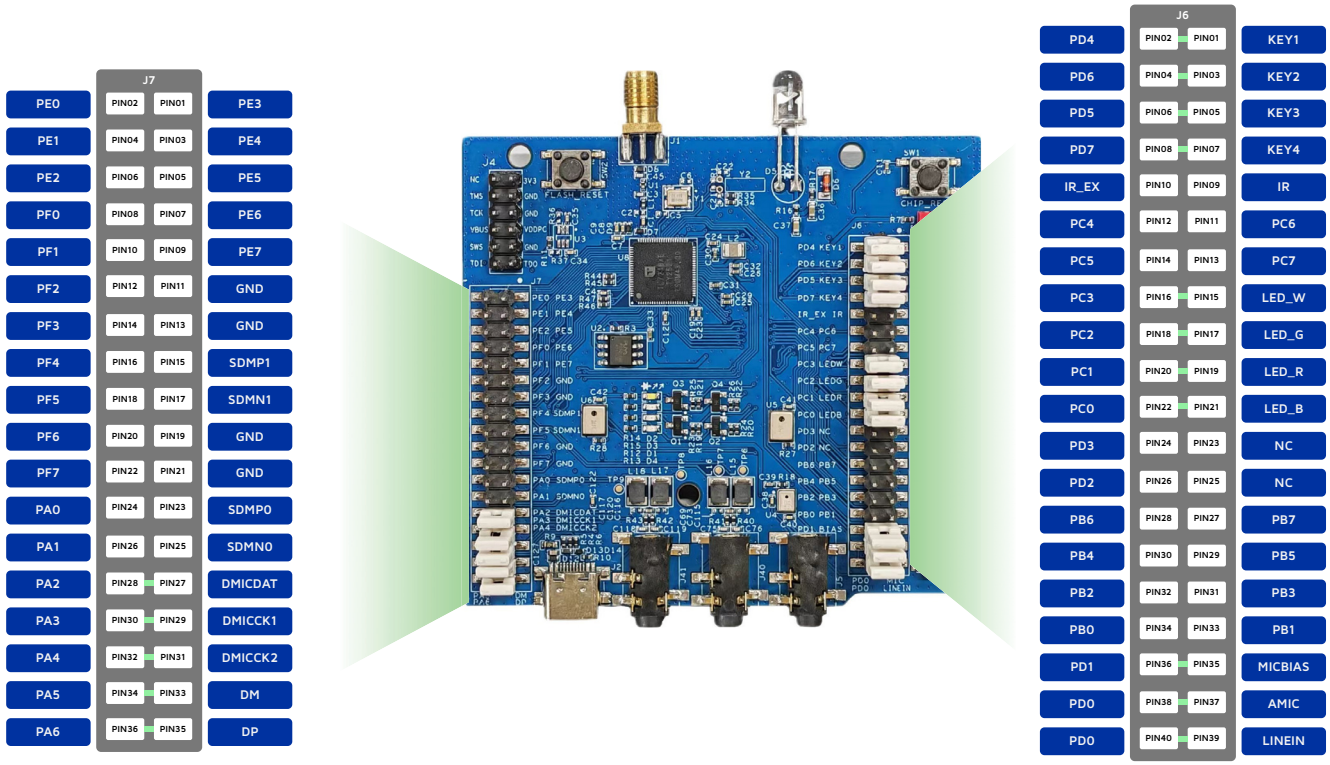
Table 2-5 GPIO connections

No.	Chip pins	IO name	Connector pins
1	U8.PIN01	PA2	J7.PIN28
2	U8.PIN02	PA3	J7.PIN30
3	U8.PIN03	PA4	J7.PIN32
4	U8.PIN14	PB0	J6.PIN34
5	U8.PIN15	PB1	J6.PIN33
6	U8.PIN16	PB2	J6.PIN32
7	U8.PIN17	PB3	J6.PIN31
8	U8.PIN18	PB4	J6.PIN30
9	U8.PIN19	PB5	J6.PIN29
10	U8.PIN20	PB6	J6.PIN28
11	U8.PIN21	PB7	J6.PIN27
12	U8.PIN24	PC0	J6.PIN22
13	U8.PIN25	PC1	J6.PIN20
14	U8.PIN26	PC2	J6.PIN18
15	U8.PIN27	PC3	J6.PIN16
16	U8.PIN53	PD0	J6.PIN38&PIN40
17	U8.PIN54	PD1	J6.PIN36
18	U8.PIN55	PD2	J6.PIN26
19	U8.PIN56	PD3	J6.PIN24
20	U8.PIN60	PD4	J6.PIN2
21	U8.PIN61	PD5	J6.PIN6
22	U8.PIN62	PD6	J6.PIN4
23	U8.PIN63	PD7	J6.PIN8
24	U8.PIN67	PE0	J7.PIN2

No.	Chip pins	IO name	Connector pins
25	U8.PIN68	PE1	J7.PIN4
26	U8.PIN69	PE2	J7.PIN6
27	U8.PIN70	PE3	J7.PIN1
28	U8.PIN71	PE4	J7.PIN3
29	U8.PIN72	PE5	J7.PIN5
30	U8.PIN73	PE6	J7.PIN7
31	U8.PIN74	PE7	J7.PIN9
32	U8.PIN75	PF0	J7.PIN8
33	U8.PIN76	PF1	J7.PIN10
34	U8.PIN77	PF2	J7.PIN12
35	U8.PIN78	PF3	J7.PIN14
36	U8.PIN79	PF4	J7.PIN16
37	U8.PIN80	PF5	J7.PIN18
38	U8.PIN81	PF6	J7.PIN20
39	U8.PIN82	PF7	J7.PIN22
40	U8.PIN84	PA0	J7.PIN24
41	U8.PIN85	PA1	J7.PIN26

The following figure shows the net names of all the pins of J7 and J6 for reference.

Figure 2-6 All pins of J7 and J6



2.6 Peripheral Interface - USB Type-C

The TL7218X development board is designed with a USB Type-C connector for power supply and full-speed communication support.

The following table lists the connections of DM and DP.

Table 2-6 DM and DP of USB

No.	Chip pins	IO name	Connector pins	Description
1	U8.PIN10	PA5	J7.PIN34	(1) Connect to J7 PIN34 and then to J7 PIN33 via the jumper. (2) Connect to the DM pin of USB. (3) The pin location refers Figure 2-6.
2	U8.PIN11	PA6	J7.PIN36	(1) Connect to J7 PIN36 and then to J7 PIN35 via the jumper. (2) Connect to the DP pin of USB. (3) The pin location refers Figure 2-6.

2.7 Peripheral Interface - 32.768KHz Crystal

The TL7218X development board embeds a 32KHz RC circuit and also supports an external 32.768KHz crystal.

The following table lists the pin connections of the 32.768KHz crystal.

Table 2-7 Connection of 32.768KHz crystal

No.	Chip pins	IO name	Connector pins	Description
1	U8.PIN55	PD2	J6.PIN26	(1) Supports configuration as GPIO and external 32.768KHz crystal function. The default function is GPIO, which is connected to external 32.768KHz crystal through R34, so as to test the GPIO and enable the external 32.768KHz crystal function. (2) The pin location refers Figure 2-6.
2	U8.PIN56	PD3	J6.PIN24	(1) Supports configuration as GPIO and external 32.768KHz crystal function. The default function is GPIO, which is connected to external 32.768KHz crystal through R35, so as to test the GPIO and enable the external 32.768KHz crystal function. (2) The pin location refers Figure 2-6.

2.8 Peripheral Interface - DMIC

The TL7218X development board is designed with two DMICs, the part number of microphone is WMM7047DTFN0 for demonstration.

The following table lists the connections of DMIC pin.

Table 2-8 Connection of DMIC pin

No.	Chip pins	IO name	Connector pins	Description
1	U8.PIN01	PA2	J7.PIN28	(1) Connect to J7 PIN28 and then to J7 PIN27 via the jumper. (2) Connect to the data pin of DMIC. (3) The pin location refers Figure 2-6.
2	U8.PIN02	PA3	J7.PIN30	(1) Connect to J7 PIN30 and then to J7 PIN29 via the jumper. (2) Connect to the clock pin of DMIC. (3) The pin location refers Figure 2-6.
3	U8.PIN03	PA4	J7.PIN32	(1) Connect to J7 PIN32 and then to J7 PIN31 via the jumper. (2) Connect to the clock pin of DMIC2. (3) The pin location refers Figure 2-6.

2.9 Peripheral Interface - Flash

The TL7218X development board is equipped with an external flash, the part number P25Q16SU, which is convenient for customers to extend the use or verify the new flash.

The following table lists the connections of the flash pins.

Table 2-9 Connections of Flash pins

No.	Chip pins	IO name	Flash
1	U8.PIN07	PG0	U2.PIN05
2	U8.PIN08	PG1	U2.PIN06
3	U8.PIN09	PG2	U2.PIN07
4	U8.PIN06	PG3	U2.PIN01
5	U8.PIN05	PG4	U2.PIN02
6	U8.PIN04	PG5	U2.PIN03

2.10 Peripheral Interface - IR

The TL7218X development board is designed with IR debugging circuit for demonstration.

The following table lists the connections of IR pin.

Table 2-10 Connection of IR pin

No.	Chip pins	IO name	Connector pins	Description
1	U8.PIN44	IR_EX_DIOD	J6.PIN10	(1) Connect to J6.PIN10 and then to the IR section of the circuit. (2) Work as internal debugging interface. (3) The pin location refers Figure 2-6.
2	U8.PIN45	IR	J6.PIN9	(1) Connect to J6.PIN9 and then to the IR section of the circuit. (2) The pin location refers Figure 2-6.

2.11 Uplink Interface

The uplink of the TL7218X development board supports one AMIC, one single-ended LINE-IN path configuration. Both can be configured via wires.

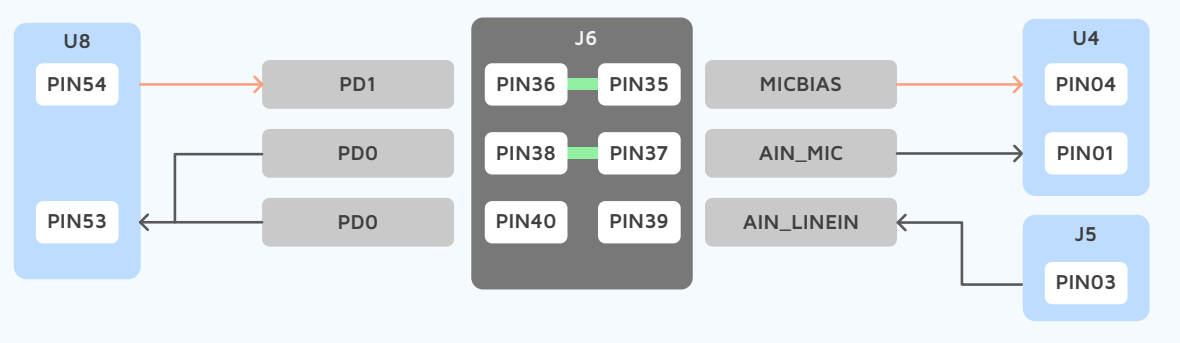
The following table lists the configuration methods for the uplink path.

Table 2-11 Configuration of uplink path

No.	Chip pins	Description
1	One single-ended AMIC configuration	(1) The default connection of the development board is one single-ended AMIC configuration. (2) The jumper on PIN37-PIN38 of J6 and the jumper on PIN35-PIN36 of J6 are plugged by default. (3) The pin location refers Figure 2-7.
2	One single-end LINE-IN configuration	(1) Unplug the connector on PIN37-PIN38 of J6 and the jumper on PIN35-PIN36 of J6. (2) Plug the jumper on PIN39-PIN40 of J6. (3) At this point, connect to the audio test instrument through the 3.5mm socket of the J5 for uplink performance testing using the single-ended connection method. (4) The pin location refers Figure 2-7.

The following figure shows the relationship of single-ended AMIC and LINE-IN uplink path.

Figure 2-7 Relationship of single-ended AMIC and LINE-IN uplink



2.12 Downlink Interface

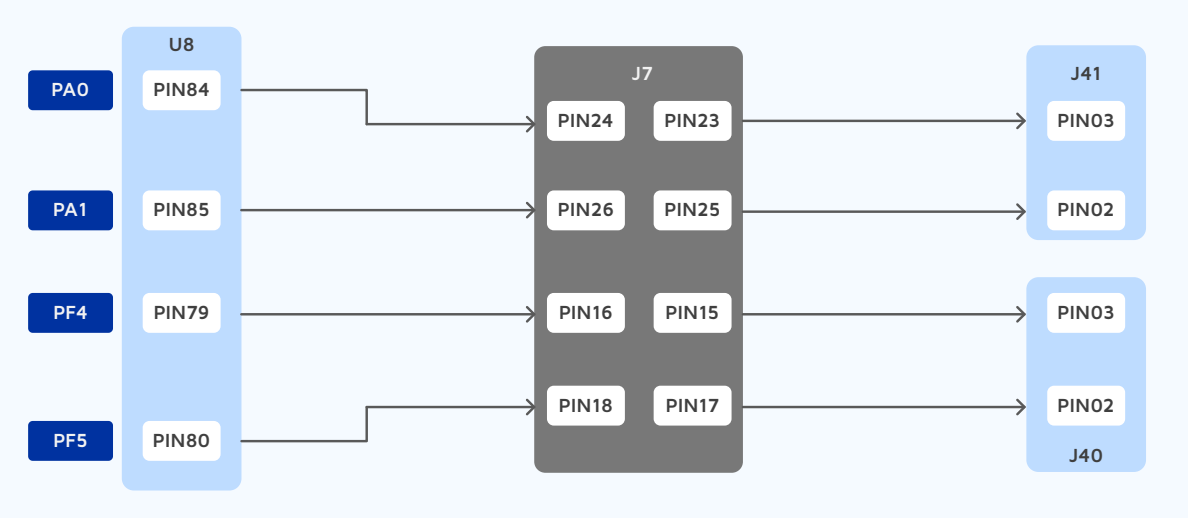
The downlink of the TL7218X development board supports two SDM differential outputs. Note that single-ended configuration is not supported.

The following table lists the downlink configuration methods.

Table 2-12 Configuration of downlink path

No.	Chip pins	IO name	Connector pins	Description
1	U8.PIN084	PA0	J7.PIN24	(1) Connect to J7.PIN24 and then to J7.PIN23 via the jumper. (2) Connect to J41.PIN03 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8.
2	U8.PIN85	PA1	J7.PIN26	(1) Connect to J7.PIN26 and then to J7.PIN25 via the jumper. (2) Connect to J41.PIN02 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8.
3	U8.PIN79	PF4	J7.PIN16	(1) Connect to J7.PIN16 and then to J7.PIN15 via the jumper. (2) Connect to J40.PIN03 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8.
4	U8.PIN80	PF5	J7.PIN18	(1) Connect to J7.PIN18 and then to J7.PIN17 via the jumper. (2) Connect to J40.PIN02 after passing through the relevant circuit of SDM. (3) The pin location refers Figure 2-8.

Figure 2-8 Connections of downlink path



3 Related Documents

The following table lists other documents and resources that you can refer to for more information. Some of these documents are only available under a Non-Disclosure Agreement (NDA). To access such documents, please contact your local Telink Field Application Engineer (FAE) or sales representative.

Table 3-1 Related Documents

No.	Name	Description	Link / Obtain method
1	TL721x datasheet	Provides information on the electrical characteristics, hardware description, and ordering options for the TL721x series chip.	TL721x datasheet
2	TL721x Hardware Guideline	Provides hardware design guide for the TL721x series chip.	TL721x Hardware Guideline
3	TL7218X board files	Provides design files of schematic, PCB layout and gerber file for the TL7218X development board.	TL7218X board files