PS9332L, PS9332L2

R08AN0002EJ0100
Rev.1.00
Jul 12, 2013

Photocouplers Used to Drive IGBTs and Featuring Built-in Protection Functions

Contents

1. Introduction 2
2. Product overview 2
3. Description of operations and functions 4
4. Sample design 7
5. PS9332 peripheral circuits 13
6. Specifying dead time 14
7. Summary 15

1. Introduction

The recent rise in awareness of environmental issues and the corresponding demand for energy savings has seen an increase in the use of inverter technology in a wide range of fields, including industrial machinery, power equipment, and home appliances. The demand for industrial inverters such as general-purpose inverters and AC servos is growing strongly in the traditional European and North American markets and is also taking off in emerging markets. Demand for inverter technology is also expected to grow in the expanding "clean energy" fields of solar and wind power generation. One of the most common semiconductor devices used in these inverters is an IGBT (Insulated Gate Bipolar Transistor).

The PS9332L and PS9332L2 (hereafter referred to as PS9332) are gate-driving photocouplers with built-in IGBT protection functions.

The PS9332 integrates an active Miller clamp that was previously attached externally to prevent the IGBT from malfunctioning, which facilitates the design of peripheral IGBT driving circuits. The PS9332 is available in an 8-pin SDIP (shrink dual inline package), shown in Figure 1 below, contributing even further to system compactness.

This application note describes the features and applications of the PS9332.

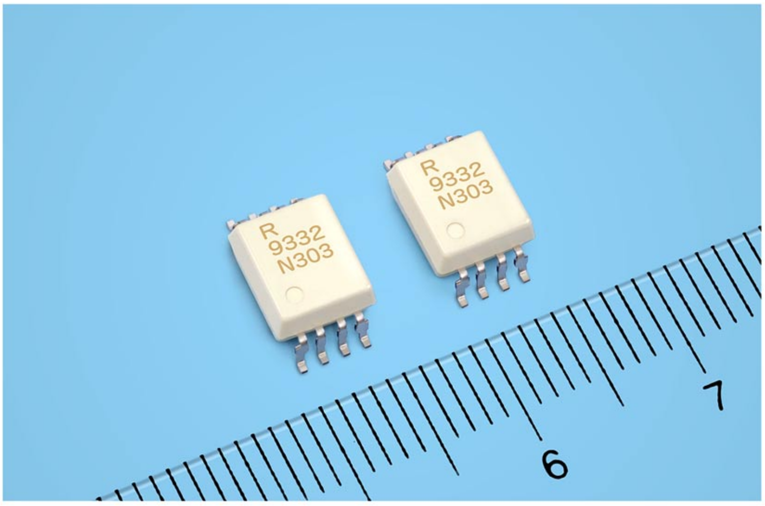


Figure 1 Photograph of PS9332 (SDIP-8)

2. Product overview

The equivalent circuit of the PS9332 is shown in Figure 2.1. The PS9332 features a GaAlAs LED on the signal receiving side, and on the signal output side, a photo detector IC that combines a photo diode (PD), signal processing circuit, and a large-current output circuit along with IGBT protection circuits (active Miller clamp and UVLO). The photo detector IC is fabricated with the Bi-CMOS process proven in other Renesas Electronics IGBT-driving photocouplers, enabling both a high output current (I_O = 2 A MAX.) and low circuit current (I_{CC} = 2.5 mA MAX.), which enables high-temperature operation (T_A = 125ºC MAX.).

The features of the PS9332 are described on the following pages. Table 2.1 is a truth table for the PS9332's logic circuits. For details of the PS9332's electrical specifications, see the data sheet.

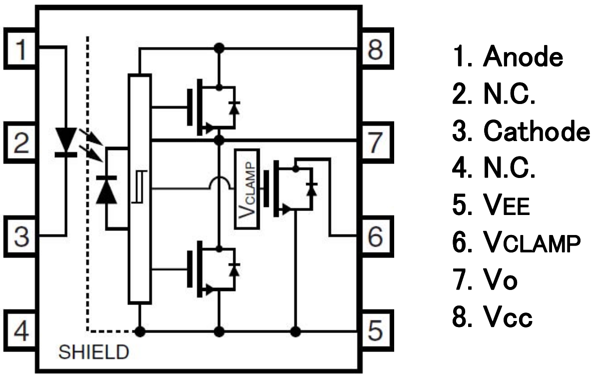


Figure 2.1 PS9332 Equivalent Circuit

Features

- IGBT protection functions (active Miller clamp, UVLO)
- High output peak current: 2.0 A MAX.
- High-speed switching: t_{PLH}, t_{PHL} = 200 ns MAX.
- Propagation delay difference between two parts: PDD = 90 ns MAX.
- Low power consumption: I_{CCH}, I_{CCL} = 2.5 mA MAX.
- Low driving current: I_{FLH} = 4 mA MAX.
- Low dissipation: $V_{OH} = V_{CC} - 1.3$ V TYP.
- High temperatures supported: Up to 125ºC
- 8 mm creepage: 8-pin SDIP (PS9332L2)
- Complies with international safety standards: UL, VDE, CSA, SEMKO
- High common mode transient immunity: CM_H, CM_L = 50 kV/μs MIN.

Table 2.1 Truth Table

I_F	UVLO ($V_{CC2} - V_{EE}$)	Miller Clamp (V_{CLAMP})	V_O
OFF	Not active (>V_{UVLO+})	Active	Low
ON	Not active (>V_{UVLO+})	Not active	High
OFF	Active (<V_{UVLO-})	Not active	Low
ON	Active (<V_{UVLO-})	Not active	Low

3. Description of operations and functions

3.1 Operational overview

Figure 3.1 shows an example of the IGBT driving circuit we recommend with the PS9332.

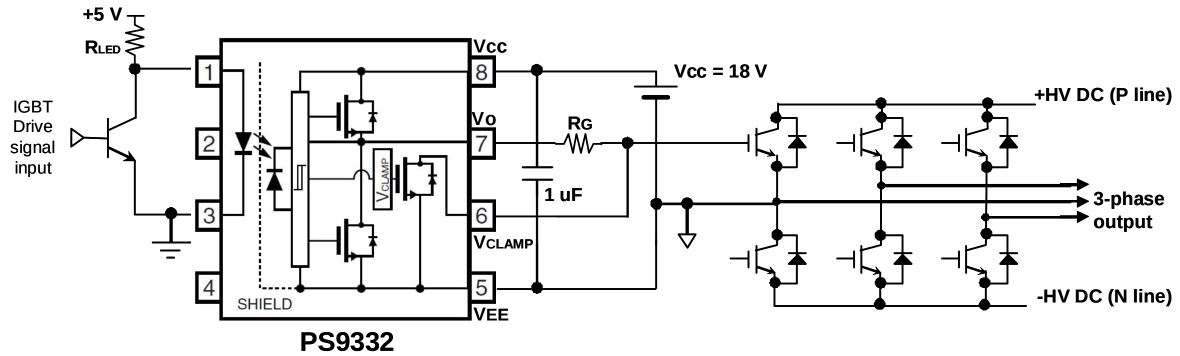


Figure 3.1 Example of Operational Circuit Recommended for PS9332

When the IGBT driving signal (I_F) is input to the PS9332's LED (pin 1), the output voltage V_O (pin 7) goes high (active-high operation (Figure 3.2)).

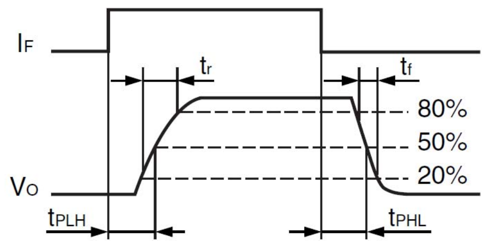


Figure 3.2 Waveform of PS9332 LED (I_F) Forward Current vs. Output Voltage

The gate voltage of the IGBT drops when the LED is turned off. When the gate voltage at the V_{CLAMP} pin (pin 6) drops below approximately 3 V, the active Miller clamp in the PS9332 starts operating to allow the Miller current to flow from the V_{CLAMP} pin (pin 6). When the LED is turned on, clamping is stopped.

3.2 IGBT protection functions

3.2.1 Active Miller clamp

The active Miller clamp is used to prevent the current that occurs due to parasitic capacitance (Miller current) from causing the IGBT to malfunction.

When the IGBT connected to the photocoupler is off, the current (Miller current (I_{CG})) flowing to the Miller capacitor between the IGBT's collector and gate (the CG Miller capacitor) may generate voltage at the gate, causing the IGBT to malfunction.

When IGBT <2> in the half-bridge circuit in Figure 3.3 is turned on, a steep voltage (dV_{CE}/dt) is applied between the collector and emitter (CE) of IGBT <1>. At this time, Miller current (I_{CG}) briefly flows to the gate resistor (R_G) of the IGBT and the Q1 MOSFET in the PS9332, via the CG Miller capacitor of IGBT <1>. This causes the gate voltage of IGBT <1> to rise, and if the gate voltage then exceeds the threshold voltage, parasitic turn-on will occur, causing through-current to flow.

The active Miller clamp incorporated in the PS9332 allows this Miller current to escape via a different route, preventing a rise in the IGBT's gate voltage and thereby preventing parasitic turn-on of the IGBT and any resulting unexpected through-current.

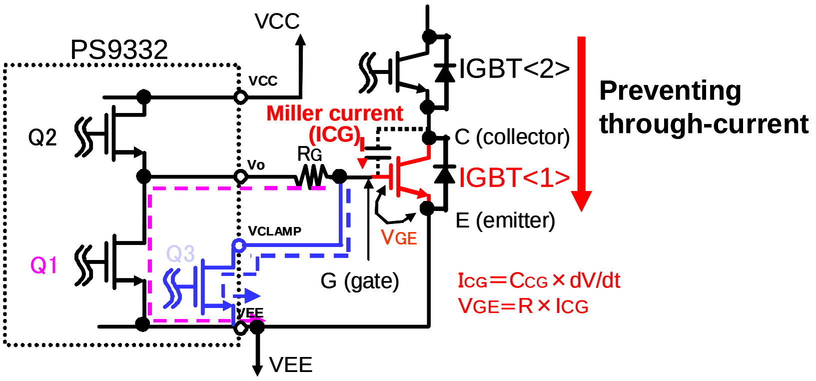


Figure 3.3 Active Miller Clamp

In terms of actual operation, the PS9332 monitors the gate voltage of the IGBT at the V_{CLAMP} pin (pin 6) while the LED is off, and once the $V_{CLAMP} – V_{EE}$ voltage reaches approximately 3 V, the clamp circuit starts operating, sending the Miller current to V_{EE} via the Q3 MOSFET of the clamp circuit (clamp current (I_{CL}) = 1.6 A TYP. when $V_{CLAMP} = V_{EE}$ + 2.5 V). IGBT <1> therefore remains off.

Figure 3.4 shows an example of the waveform when the active Miller clamp is operating and not operating. If clamping is not performed, the gate voltage of the IGBT <2> temporarily rises due to the Miller current that flows when IGBT gate <2> is turned on, which might cause IGBT <1> to malfunction. If clamping is performed, the gate voltage of IGBT <1> is prevented from rising and therefore IGBT <1> remains off.

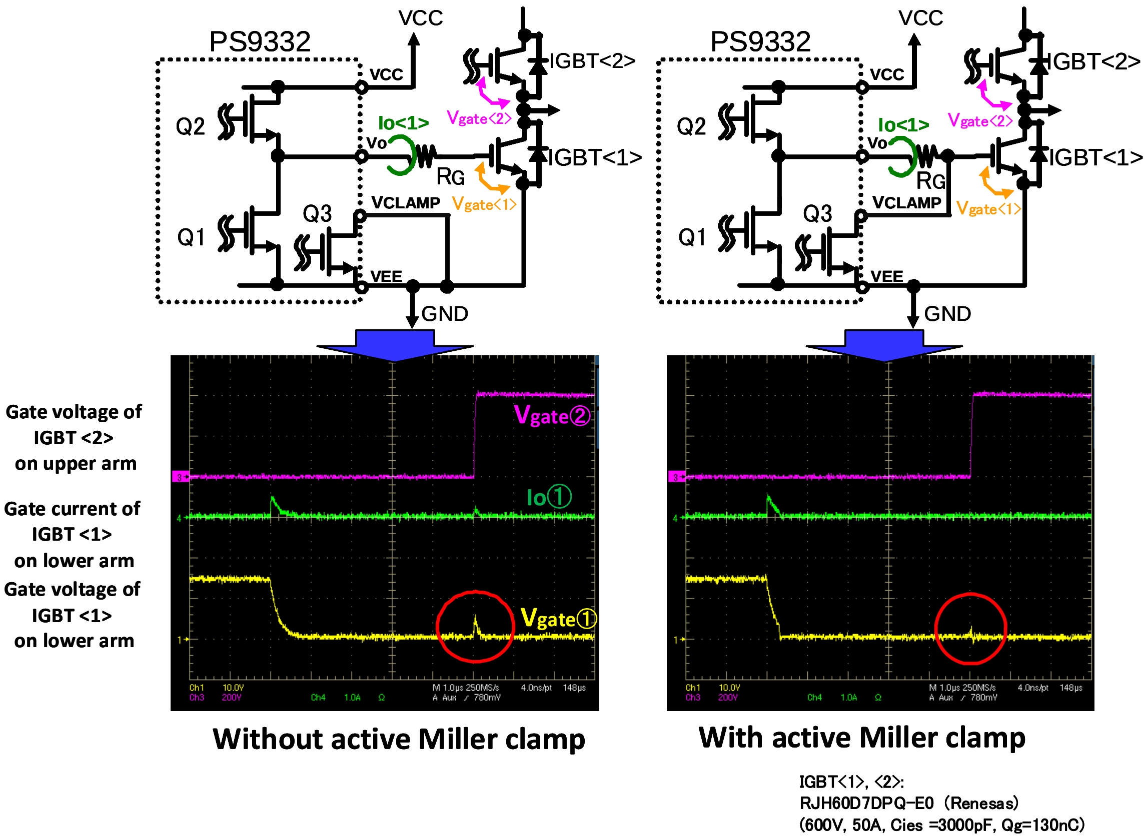


Figure 3.4 Example of Waveform When Active Miller Clamp Is Operating and Not Operating

The active Miller clamp starts operating approximately 200 ns after the gate is turned off. For your reference, Figure 3.5 shows an example of the waveforms of the PS9332 output current (I_O) and clamp current (I_{CLAMP}) when the gate is turned off.

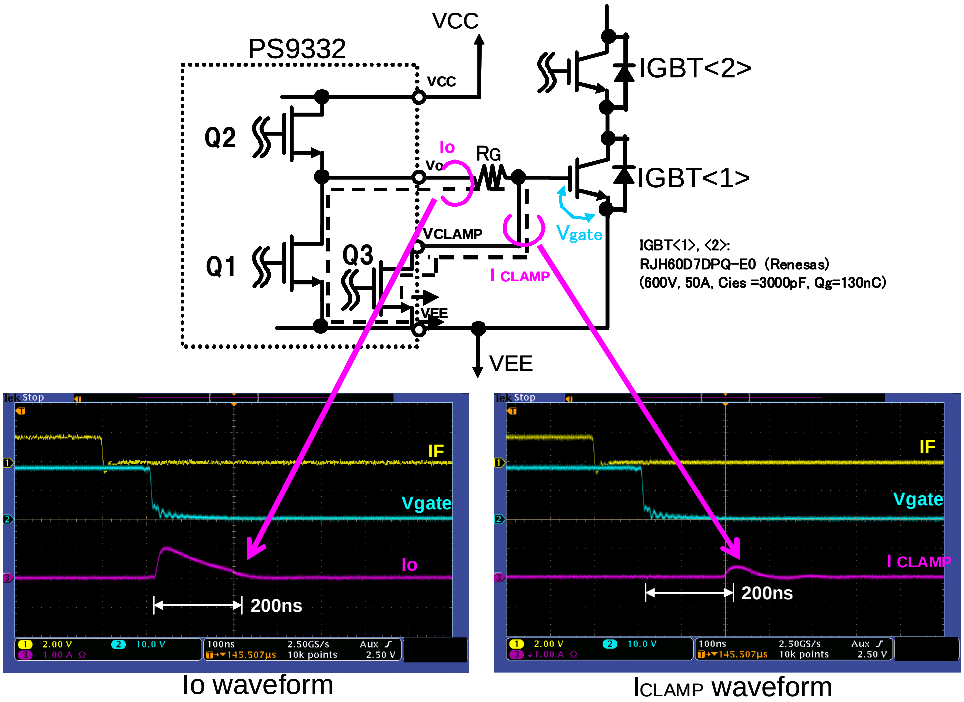


Figure 3.5 Example of Waveform When Active Miller Clamp Starts Operating

3.2.2 UVLO (undervoltage lockout)

The UVLO circuit holds V_O at low level when the PS9332's power supply voltage V_{CC} is insufficient.

If the IGBT's gate voltage (V_O in the PS9332) drops during on state, the $V_{CE\ (sat)}$ of the IGBT becomes larger and it might cause a large amount of power to dissipate, leading to overheating and failure of the IGBT. To prevent this, if the PS9332 detects that its power supply voltage ($V_{CC} – V_{EE}$) is insufficient, it holds V_O at low level to protect the IGBT.

As shown in Figure 3.6, when the PS9332's power supply voltage ($V_{CC} – V_{EE}$) is low (when the power supply voltage is rising from 0 V), the PS9332 holds the V_O output at low level until the voltage rises to V_{UVLO+}, even if the LED is on. Conversely, when the PS9332's power supply voltage ($V_{CC} – V_{EE}$) is falling (changing to a negative voltage) the V_O output is high level until the voltage reaches $V_{UVLO–}$, but if the voltage falls below $V_{UVLO–}$, the PS9332 pulls the V_O output down to low level even if the LED is on.

Therefore, if the PS9332's power supply voltage ($V_{CC} – V_{EE}$) falls below $V_{UVLO–}$ (9.5 to 12.5 V) due to some error, the V_O output of the PS9332 will go low even if the LED is on. When the power supply voltage ($V_{CC} – V_{EE}$) subsequently rises to above V_{UVLO+} (10.8 to 13.4 V), the V_O output goes high again (with the LED on).

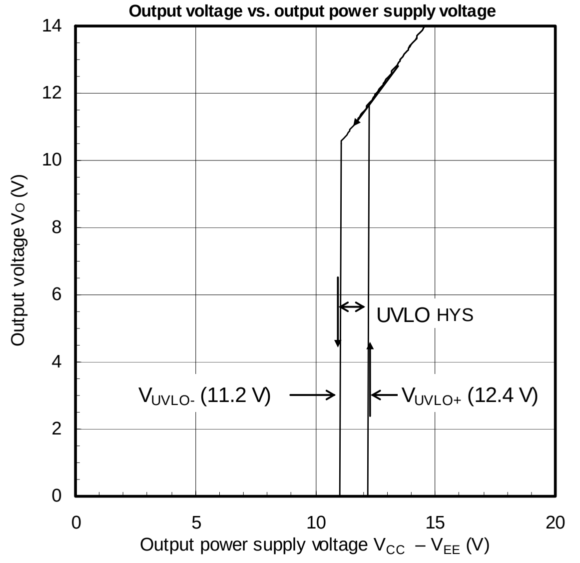


Figure 3.6 UVLO

4. Sample design

4.1 Design of active Miller clamp

The active Miller clamp must be connected to the PS9332's active Miller clamp pin (V_{Clamp}: pin 6) as close as possible to the IGBT's gate in order to prevent parasitic turn-on of the IGBT due to a rise in the gate voltage caused by Miller current flowing through the gate resistor.

Figure 4.1 shows an example of how the active Miller clamp is connected when using a single power supply (negative power supply not used).

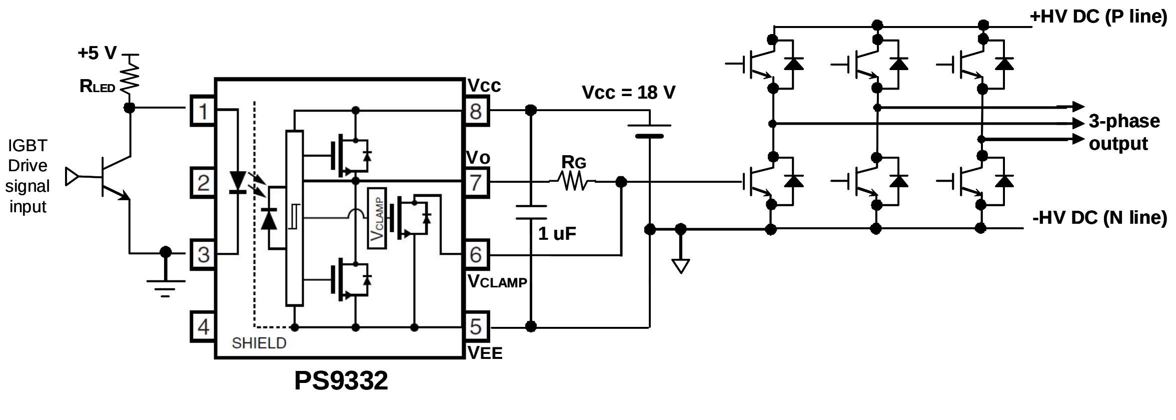


Figure 4.1 Example of Connecting Active Miller Clamp
When Using Single Power Supply (Negative Power Supply Not Used)

Figure 4.2 shows an example of how the active Miller clamp is connected when using a negative power supply.

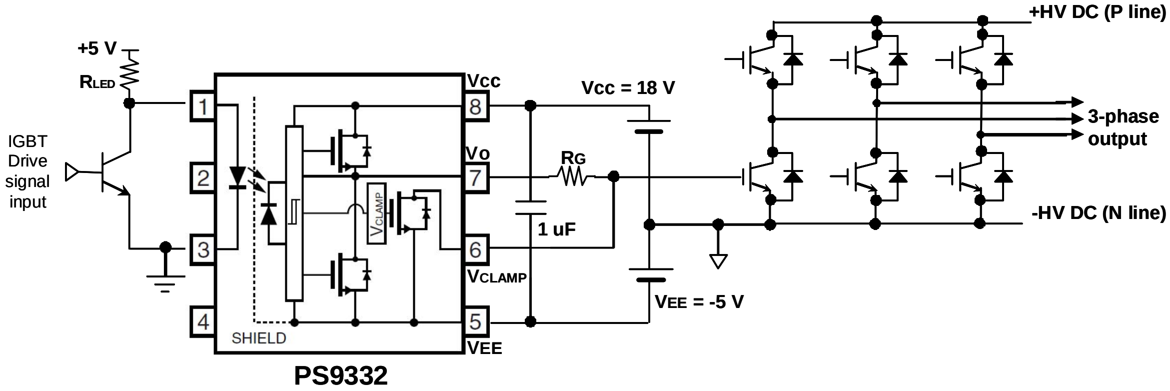


Figure 4.2 Example of Connecting Active Miller Clamp When Using Negative Power Supply

Note, however, that the PS9332 clamp current is about 1.6 A, making it difficult to connect V_{CLAMP} directly to the gate of a high-power IGBT. Check the estimated Miller current capacity and if the clamp current at V_{CLAMP} is insufficient, externally connect a PNP transistor as shown in Figure 4.3. Connecting an external buffer is effective because the Miller current from the IGBT does not flow through the gate resistor.

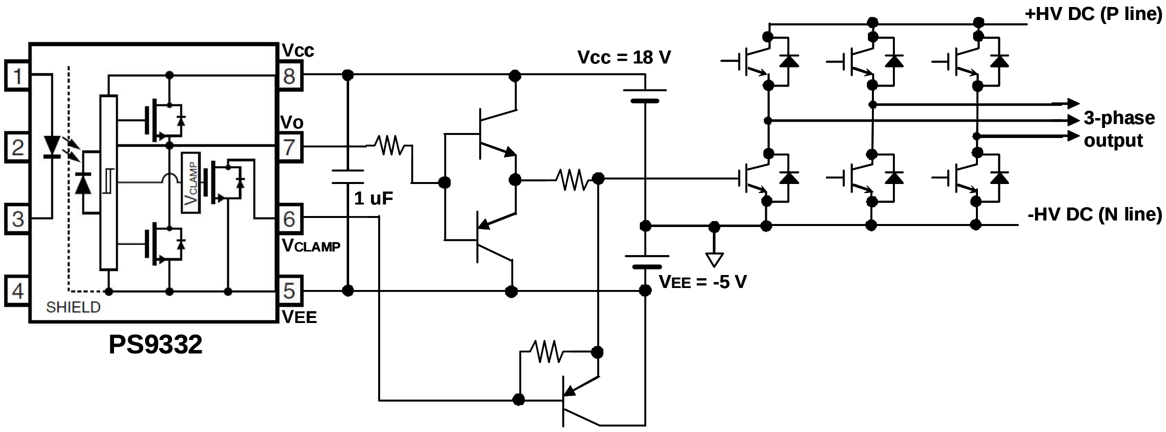


Figure 4.3 Example of Connecting Active Miller Clamp to V_{CLAMP} Pin When Buffer Is Connected Externally

If the active Miller clamp is not used, such as when using a negative power supply, connect the V_{CLAMP} pin to V_{EE}, as shown in Figure 4.4.

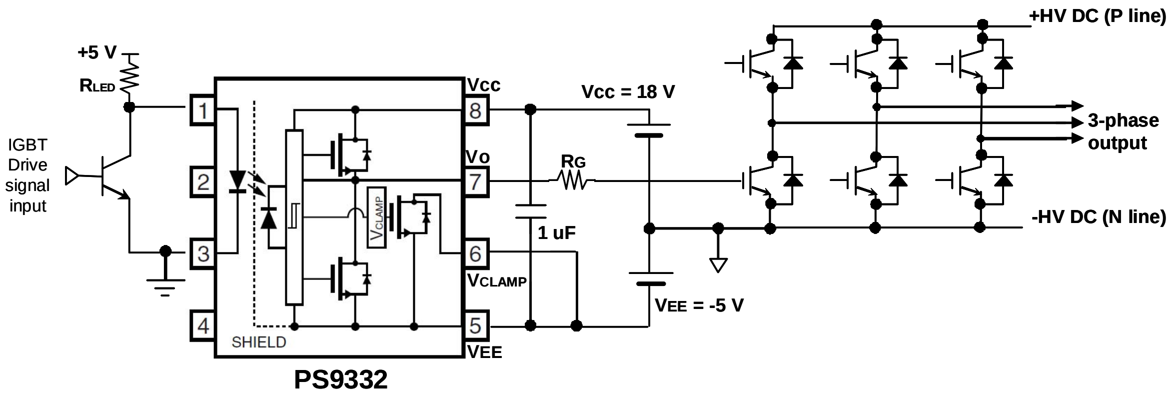


Figure 4.4 Connection When Active Miller Clamp Is Not Used

4.2 Design of IGBT gate driver

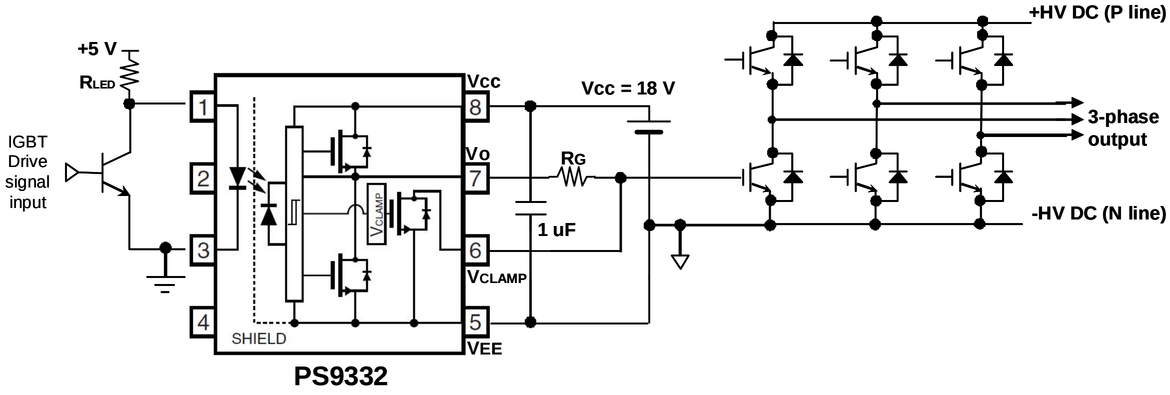


Figure 4.5 Example Application Circuit Using PS9332

Figure 4.5 shows an example IGBT gate driver that uses the PS9332. The gate resistor settings are described in 4.2.1 and 4.2.2 below.

4.2.1 Calculating the minimum resistance of the IGBT's external gate resistor (R_G)

(1) Calculation from the photocoupler side

The external gate resistor (R_G) must be selected so that the peak output current of the PS9332 ($I_{OL(PEAK)}$) does not exceed its maximum rating. The minimum value of the gate resistor (R_G) can be approximated by using the following expression:

$R_G \geq \{(V_{CC} - V_{EE}) - V_{OL}\}/I_{OL(PEAK)}$ ········ [4.2.1]
$V_{CC} - V_{EE}$: PS9332 power supply difference ($V_{EE} = 0$ when not using a negative power supply)
V_{OL}: PS9332's low-level output voltage

Calculate the minimum value of the external gate resistor (R_G) under the following conditions:

$I_{OL(PEAK)} = 2.0$ A
$V_{CC} - V_{EE} = 18$ V
Voltage drops to $V_{OL} = 2.5$ V while $I_{OL} = 2.0$ A.

Characteristics curves showing the relationship between the low-level output voltage (V_{OL}) and low-level output current (I_{OL}) are provided in Figure 4.6 for reference. These settings make allowances for operation under low temperatures (–40ºC). Note that because the low-side MOSFET voltage drops less than the high-side MOSFET voltage in the PS9332, the minimum value of the external gate resistor (R_G) is calculated based on the low-side MOSFET.

From equation [4.2.1]:

$$R_G \geq \{(V_{CC} - V_{EE}) - V_{OL}\}/I_{OL(PEAK)}$$
$$= (18 - 2.5)/2.0$$
$$= 7.8\ \Omega$$

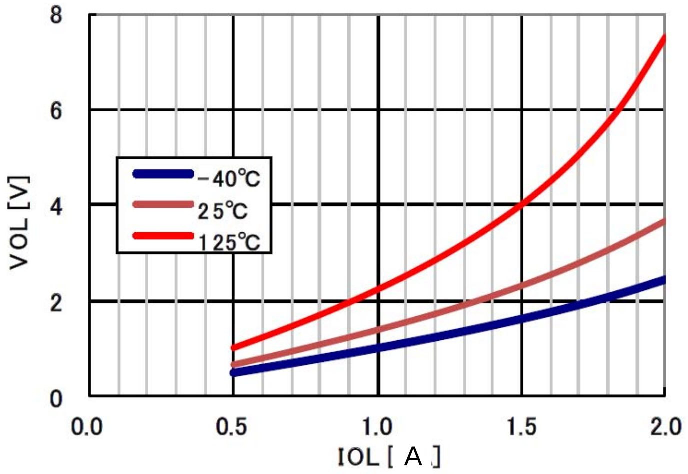


Figure 4.6 V_{OL} vs. I_{OL} Characteristics

(2) Calculation from the IGBT side

The charge characteristics of the IGBT's gate are described in the IGBT's data sheet, but in general, the characteristics curve is as shown in Figure 4.7.

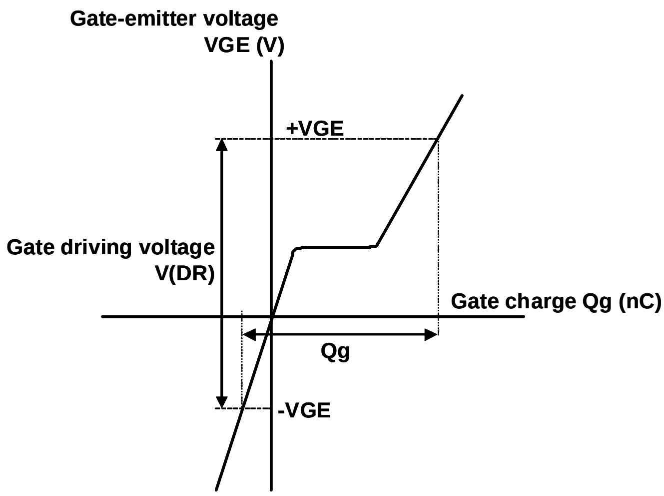


Figure 4.7 VGE vs. Q_g Characteristics

The gate charge is expressed as follows:

$Q_g = C \times V_{(DR)}$,

with Q_g indicating the total charge, and $V_{(DR)}$ indicating the gate driving voltage ($V_{(DR)} = +V_{GE} - (-V_{GE})$).

The relationship between the gate capacitance, the switching time, and the gate driving current is as follows:

$dQ_g/dt = C \times dV_{(DR)}/dt = I_G$

In this case, if tsw represents the switching time required by the system, the current that must be supplied to the gate (I_G) is indicated by:

$I_G = Q_G/tsw$

Because a constant driving voltage $V_{(DR)}$ is used, the relationship between the gate peak current and the total gate resistance (R_G') is as follows:

$$R_G' = V_{(DR)}/I_G,$$

with R_G' indicating the sum of the external gate resistance R_G and the IGBT gate's own series resistance (internal resistance).

Therefore, in order to satisfy the switching time required by the system, the external gate resistance calculated from the photocoupler side (R_G) must be smaller than the total gate resistance calculated from the IGBT side (R_G'). If tsw is unable to be satisfied, you will have to consider selecting a photocoupler that can drive a larger current, or attaching an external current amplifier (buffer).

4.2.2 Checking the allowable dissipation of the PS9332 and adjusting R_G

The power consumption of the PS9332 (P_T) is a total of the power consumption of the LED on the input side (primary side) (P_D) and the power consumption of the photo detector IC on the output side (secondary side) connected to the IGBT (P_O).

$$P_T = P_D + P_O \cdots\cdots\; [4.2.2]$$

(1) LED power consumption

The power consumption of the LED on the input side (primary side) (P_D) is calculated as follows:

$$P_D = I_F \times V_F \times \text{Duty ratio} \cdots\cdots\; [4.2.3]$$

(2) Photo detector IC power consumption

The power consumption of the photo detector IC on the output side (secondary side) (P_O) is calculated as follows:

$$P_O = P_{o(Circuit)} + P_{o(Switching)} \cdots\cdots\; [4.2.4]$$

$P_{o(Circuit)}$ is the circuit power consumption of the photo detector IC (the power consumed by I_{CC}).

$P_{o(Switching)}$ is the power consumption of the photo detector IC required to charge and discharge the gate capacitor (the power consumed by I_O).

1. Circuit power consumption of photo detector IC: $P_{o(Circuit)}$

$$P_{o(Circuit)} = I_{CC} \times (V_{CC} - V_{EE}) \cdots\cdots\; [4.2.5]$$

I_{CC} is the circuit current supplied to the photo detector IC.

$V_{CC} - V_{EE}$ is the power supply difference of the photo detector IC.

2. Power consumption of photo detector IC required to charge and discharge the IGBT gate capacitor

$$P_{o(Switching)} = Esw(R_G, Q_G) \times f_{SW} \cdots\cdots\; [4.2.6]$$

$E_{SW}(R_G, Q_G)$ is the per-cycle power consumed when charging the IGBT gate capacitor (see Figure 4.8 and Figure 4.9).

f_{SW} is the switching frequency.

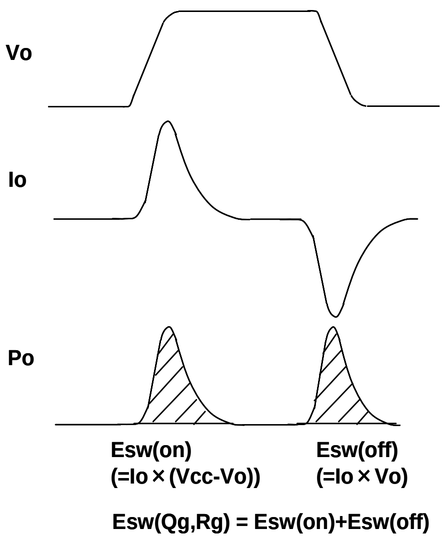


Figure 4.8 PS9332 Power Consumption Waveform During Switching

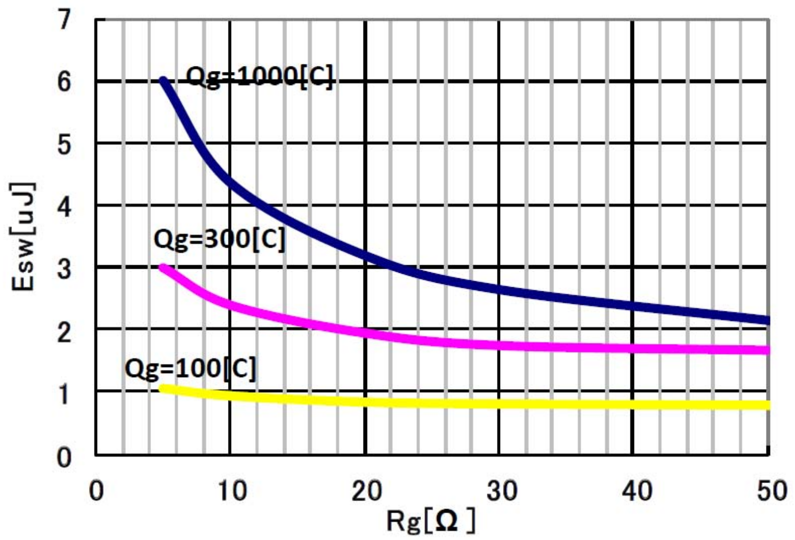


Figure 4.9 PS9332 Switching Dissipation per Cycle

3. Power consumption of photo detector IC
   From the calculations in [4.2.4], [4.2.5], and [4.2.6], the power consumption of the photo detector IC is as follows:

$$P_O = P_{o(Circuit)} + P_{o(Switching)}$$
$$= I_{CC} \times (V_{CC} - V_{EE}) + Esw(R_G, Q_G) \times f_{SW} \cdots\cdots [4.2.7]$$

(3) Checking the allowable dissipation of the PS9332 and adjusting R_G

When used in the circuit shown in Figure 4.5, the power consumption of the PS9332 is as follows, calculated under the conditions of R_G = 7.8 Ω, Duty (MAX.) = 80%, Q_G = 300 nC, f = 20 kHz, I_F = 12 mA, and T_A = 100°C:

1. Power consumption of input side (primary side, LED) (P_D)
   From the calculation in [4.2.3]:

$$P_D = I_F \times V_F \times \text{Duty ratio}$$
$$= 12\ \text{mA} \times 1.75\ \text{V} \times 0.8 = 16.8\ \text{mW}$$

2. Power consumption of output side (secondary side, photo detector IC) (P_O)
   From the calculation in [4.2.7]:

$$P_O = I_{CC} \times (V_{CC} - V_{EE}) + Esw(R_G, Q_G) \times f_{SW}$$
$$= 2.5\ \text{mA} \times 18\ \text{V} + 2.7\ \mu\text{J} \times 20\ \text{kHz}$$
$$= 45\ \text{mW} + 54\ \text{mW}$$
$$= 99\ \text{mW} < 250\ \text{mW}$$

(absolute maximum allowable dissipation for photo detector IC when T_A = 100ºC)

The gate resistance R_G has a significant effect on the performance of the IGBT, so be sure to select the right gate resistor for your gate driver design. A smaller gate resistance means faster switching to charge and discharge the IGBT's input capacitor, which leads to lower switching dissipation. However, a smaller gate resistance also leads to a larger voltage variation (dV/dt) and current variation (di/dt) during switching. It is therefore important to evaluate the actual operation of the IGBT by referring to the relevant technical documents before selecting the gate resistor.

5. PS9332 peripheral circuits

5.1 Layout

1. To minimize floating capacitance between the primary side and the secondary side (the input and the output), be sure to place the circuits so that they are not too close to the primary-side and secondary-side wiring patterns on the board, and that there is no cross-wiring if multi-layer wiring is being used.
2. To prevent transient noise from the IGBT from affecting the PS9332, keep the IGBT collector/emitter circuit pattern and DC lines (P and N lines) of the inverter circuit through which a large current flows as far away as possible from the PS9332's LED driver and V_{CC} and V_O lines.
3. Place the bypass capacitors (with a capacitance of 1 µF or higher) between V_{CC} and V_{EE} on the secondary side (output side) of the PS9332 as close to the PS9332's V_{CC} (pin 8) and V_{EE} (pin 5) pins as possible (in other words, keep the distance between the PS9332's pins and the capacitor pins as short as possible).

5.2 LED driver

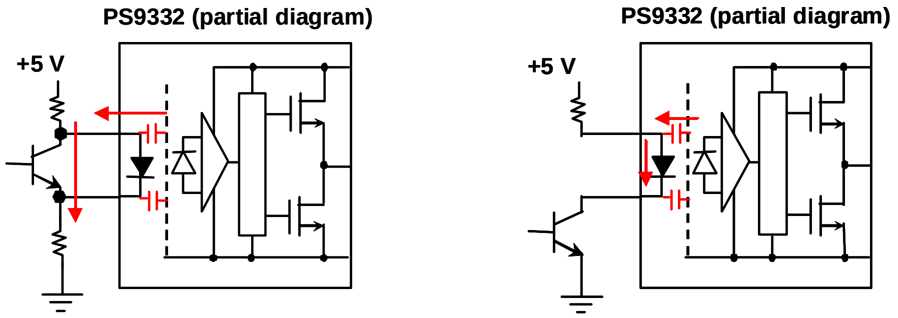
Design the LED driver so that the recommended current (I_F) and voltage (V_F) are applied to the LED. Table 5.1 shows the recommended operating conditions for the LED.

Table 5.1 Recommended Operating Conditions for PS9332 LED

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input voltage (OFF)	$V_{F\ (OFF)}$	–2	–	0.8	V
Input current (ON)	$I_{F\ (ON)}$	7	–	16	mA

To ensure that the LED is turned off properly, even if common mode noise (CM_L) occurs, we recommend applying a reverse bias to the LED within the range indicated by the recommended operating conditions in Table 5.1. Similarly, to ensure that the LED is turned on properly, even if common mode noise (CM_H) occurs, we recommend specifying as large a LED current (I_F) as possible, within the range indicated by the recommended operating conditions in Table 5.1.

If it is not possible to apply a reverse bias to the LED while the LED is off, we recommend configuring the circuit so that the collector and emitter of the LED driver's output transistor are connected respectively to the anode and cathode of the PS9332's LED, as shown in Figure 5.1 (a) below. This is to prevent a malfunction caused by the LED turning on briefly because a potential difference between the GND pins on the primary and secondary sides of the PS9332 has caused a displacement current to flow to the LED from the photo detector, which might occur if the conventional LED driver configuration shown in Figure 5.1 (b) is used. The configuration in Figure 5.1 (a) protects against this malfunction because the output transistor of the LED driver remains on when the LED is off, even if a displacement current flows to the LED from the photo detector, making it difficult for current to flow through the LED. If the conventional LED driver circuit shown in Figure 5.1 (b) must be used due to the specifications of the driver IC, connecting a capacitor of 100 pF and a resistance of several kΩ at the ends of the LED as shown in Figure 5.2 is also effective.



(a) LED drive with high CMR (recommended)

(b) Conventional LED driver (not recommended)

Figure 5.1 LED Driver

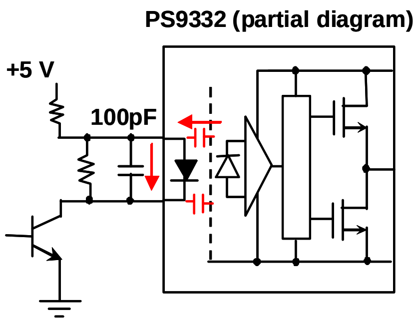
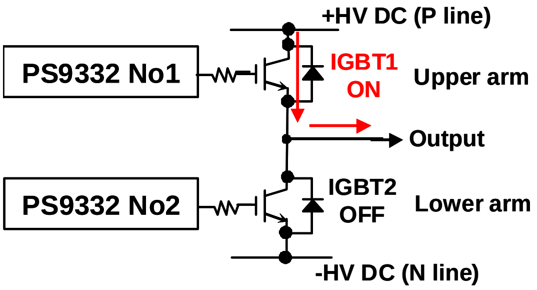


Figure 5.2 Countermeasure for CMR Noise in Conventional LED Driver Circuit

6. Specifying dead time

As shown in Figure 6.1, in the inverter circuit, IGBT 1 and IGBT 2 on the upper and lower arms alternately switch on and off, outputting a signal to the motor or other load. If there is insufficient dead time, IGBT 1 and IGBT 2 on the upper and lower arms switch on at the same time, causing a short-circuit current to flow, damaging the IGBTs (see Figure 6.2).



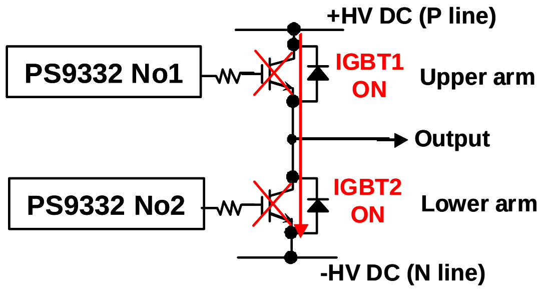


Figure 6.1 Inverter Circuit Operating Normally **Figure 6.2 Inverter Circuit When Short-Circuit Occurs**

Dead time (t_{dead}) (see Figure 6.3) is specified in order to prevent IGBT1 (upper arm) and IGBT2 (lower arm) turning on at the same time, and is usually the difference between the maximum value of the total turn-off time of the PS9332 and the IGBT (t_{off} total MAX.) and the minimum value of the total turn-on time of the PS9332 and the IGBT (t_{on} total MIN.), or higher.

$$t_{dead} \geq t_{off\ total\ MAX.} - t_{on\ total\ MIN.}$$
$$= (t_{PHL\ MAX.(PC)} + t_{off\ MAX.(IGBT)}) - (t_{PLH\ MIN.(PC)} + t_{on\ MIN.(IGBT)})$$
$$= (t_{PHL\ MAX.(PC)} - t_{PLH\ MIN.(PC)}) + (t_{off\ MAX.(IGBT)} - t_{on\ MIN.(IGBT)})$$
$$= PDD_{(PC)} + (t_{off\ MAX.} - t_{on\ MIN.})_{(IGBT)}$$

In the above equation, (PC) is the response time of the PS9332 photocoupler and (IGBT) is the response time of the IGBT.

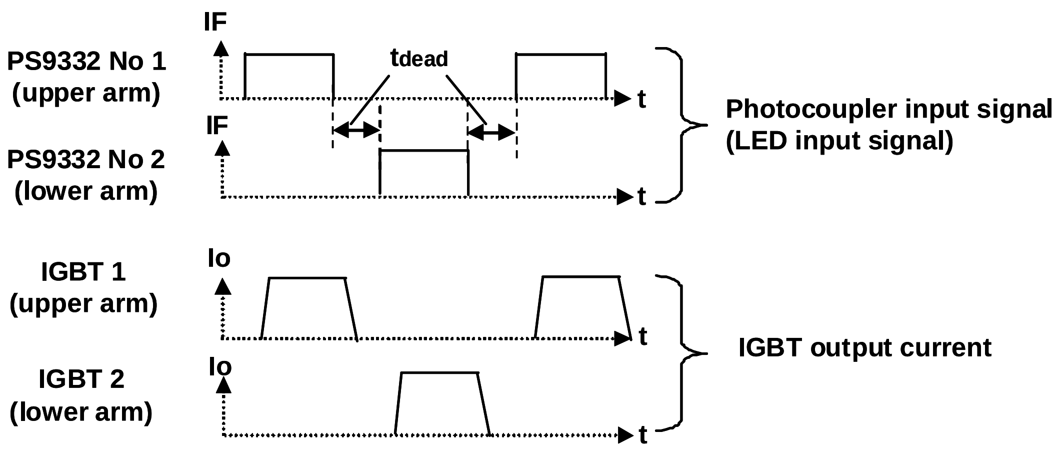


Figure 6.3 Dead Time (t_{dead})

In the PS9332, the propagation delay time difference between any two parts has been prescribed to make specifying dead time easy (this time is PDD = $t_{PHL} - t_{PLH}$ = ±90 ns). See the PS9332's data sheet for details. Note that PDD in the PS9332 must be measured under the same temperature and measurement conditions as t_{PHL} and t_{PLH}. The board must therefore be laid out so that the ambient conditions of the upper and lower arms of the photocoupler are the same. Also be sure to thoroughly evaluate the dead time using the actual device, and allow a sufficient margin in your design.

7. Summary

This application note describes the the features and applications of the PS9332 photocoupler, which is an IGBT-driving photocoupler with built-in IGBT protection circuits. Please use this document when designing your system. The PS9332 aims to facilitate the design of inverter equipment—a market that is expected to grow significantly in the future—and contribute to reducing system scale. In addition to aggressively marketing the PS9332, Renesas Electronics also plans to continue developing photocouplers that support high-end devices.

Caution GaAs Products	This product uses gallium arsenide (GaAs). GaAs vapor and powder are hazardous to human health if inhaled or ingested, so please observe the following points. • Follow related laws and ordinances when disposing of the product. If there are no applicable laws and/or ordinances, dispose of the product as recommended below. 1. Commission a disposal company able to (with a license to) collect, transport and dispose of materials that contain arsenic and other such industrial waste materials. 2. Exclude the product from general industrial waste and household garbage, and ensure that the product is controlled (as industrial waste subject to special control) up until final disposal. • Do not burn, destroy, cut, crush, or chemically dissolve the product. • Do not lick the product or in any way allow it to enter the mouth.

Revision History	PS9332L, PS9332L2 APPLICATION NOTE

Rev.	Date	Description	
		Page	Summary
1.00	Jul 12, 2013	–	First Edition Issued

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

California Eastern Laboratories, Inc.
4590 Patrick Henry Drive, Santa Clara, California 95054, U.S.A.
Tel: +1-408-919-2500, Fax: +1-408-988-0279

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141