IGLOO 2 M2GL050 (T,TS) Device Errata

Introduction

This Errata sheet contains information about known Errata specific to the IGLOO® 2 M2GL050 (T, TS) device family, and provides available fixes and solutions.

Table 1. Revisions Released per Device

Silicon Devices	Revision	Device Status
M2GL050 (T, TS)	All Temperature Grades	Production

Table of Contents

1. Errata for IGLOO 2 M2GL050 (T,TS) All Temperature Grades

The following table lists the specific device Errata and the affected IGLOO 2 M2GL050 (T, TS) revisions of all temperature grade devices.

Table 1-1. Summary of IGLOO 2 M2GL050 (T, TS) Device Errata

Errata No.	Errata	Silicon Revisions M2GL050 (T, TS)		Software Errata
		Rev(0, 1)	Rev2	
1.	MDDR and FDDR AXI interface does not support exclusive access	X	X	–
2.	Apply DEVRST_N after ISP programming	X	–	–
3.	AXI wrap transfers with more than 32 bytes in burst mode are not supported for MDDR and FDDR	X	X	–
4.	The MDDR/FDDR controller must be used with sequential burst mode with BL = 8 and PHY = 32, or PHY = 16	X	X	–
5.	HPMS may reset when ENC_DATA_AUTHENTICATION or DEVICE_INFO STAPL commands are sent	X	–	–
6.	VPP must be set to 2.5V when programming/writing the eNVM at Industrial temperature range	X	–	–
7.	Over-voltage support on MSIOs during Flash*Freeze mode	X	–	–
8.	Verification of the FPGA fabric at junction temperatures higher than 50 °C erroneously indicates a failure	X	–	–
9.	DDR_OUT and I/O-Reg functional Errata due to a software bug	–	–	X
10.	Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug	–	–	X
11.	NVM Ready bit in eNVM Status register can generate a false READY signal	X	–	–
12.	Power-up Digest is not supported	X	–	–
13.	Programming of the eNVM must only occur as part of a bitstream also containing the FPGA fabric	–	–	X
14.	Updating eNVM from the FPGA fabric requires changes in the NV_FREQRNG register	X	X	–
15.	SYSCTRL_RESET_STATUS macro is not supported	X	X	–
16.	Zeroization is not supported	X	X	–
17.	PCIe Hot Reset support requires a soft reset solution	X	X	–
18.	The DDR I/Os in M2GL050 (T, TS)-FG896 are non-compliant with the DDR3 standard	X	X	–
19.	For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM	X	X	–
20.	PCIe hard IP core receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem and cause the PCIe core to ignore subsequent PCIe traffic	X	X	–

Notes:

1. An “X” means that the Errata exists for that particular device and revision number.
2. If you have additional questions, contact Microchip by creating a new case at microchip.my.site.com/s/newcase. To order a specific die, contact your local Microchip sales office.

2. Errata Descriptions and Solutions

This section describes the various erratas and informs about their respective solutions.

2.1 MDDR and FDDR AXI Interface Does Not Support Exclusive Access

The MDDR and FDDR AXI interface in the M2GL050 device is compliant with AMBA AXI Protocol Specification v1.0, except for the exclusive access functionality. The future version of the Errata will have an updated information about the exclusive access functionality for the AXI interface.

2.2 Apply DEVRST_N after ISP Programming

M2GL050 devices support device programming in JTAG, Slave SPI, and ISP programming modes. However, after ISP programming, DEVRST_N needs to be asserted to reset the device, or power cycle the device, to run the new design.

2.3 AXI Wrap Transfers with More than 32 Bytes in Burst Mode Are Not Supported for MDDR and FDDR

Do not use wrap transfers with more than 32 bytes.

2.4 The MDDR/FDDR Controller Must Be Used with Sequential Burst Mode with BL = 8 and PHY = 32, or PHY = 16

Though the MDDR and FDDR controllers in the M2GL050 devices support various burst modes/ lengths and PHY settings (as specified in the *UG0446: SmartFusion2 and IGLOO2 FPGA High Speed DDR Interfaces User Guide*), only a subset of these settings are supported.

Recommendation:

Only use sequential burst mode with BL = 8 for PHY16, or PHY32 modes for the MDDR or FDDR.

2.5 HPMS May Reset When ENC_DATA_AUTHENTICATION or DEVICE_INFO STAPL Commands Are Sent

TheHPMS resets after executing one of the following STAPL actions:

- ENC_DATA_AUTHENTICATION
- DEVICE_INFO

Additionally, if any of these actions are executed while a SmartDebug session is active, HPMS resets are observed.

2.6 VPP Must Be Set to 2.5V When Programming/Writing the eNVM at Industrial Temperature Range

VPP can be set to 2.5V or 3.3V. However, when writing or programming the eNVM of the M2GL050 devices below 0 °C, VPP must be set to 2.5V.

For VPP minimum and maximum settings, refer to the *DS0128: IGLOO 2 FPGA and SmartFusion2 SoC FPGA Datasheet*. Note that the eNVM reading with VPP set to 3.3V or 2.5V operates as intended.

2.7 Over-Voltage Support on MSIOs during Flash*Freeze Mode

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in Flash*Freeze mode.

2.8 Verification of the FPGA Fabric at Junction Temperatures Higher than 50°C Erroneously Indicates a Failure

Standalone verification (STAPL VERIFY action) must run at temperatures lower than 50 °C. If a VERIFY action is run at temperatures higher than 50 °C, a false verify failure may be reported. Note that

the Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

2.9 DDR_OUT and I/O-reg Functional Errata Due to a Software Bug

This Errata is applicable only if you have created or updated the design using Libero®SoC v11.1 SP1 or v11.1 SP2.

The corresponding I/O does not function properly in the silicon due to the wrong software implementation of the I/O macro, if you have one of the following in the design:

- If you use DDR_OUT macro in the design
- If you combine an output or output enable register with an I/O, using the PDC command `set_io<portName>-register yes`

Solution:

Both Errata are fixed in Libero SoC v11.1 SP3. Migrate the design to Libero SoC v11.1 SP3 or a newer version, and re-run **Compile and Layout**.

2.10 Dedicated Differential I/O Driving the Reference Clock of the CCC May Cause a Functional Failure Due to a Software Bug

If the design has a dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug, and the device fails during silicon testing. There are several options to drive the reference clock of the CCC. One of the options is to drive from "Dedicated Input PAD x" (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the reference clock. This Errata exists when you choose the differential I/O option (dedicated differential I/O is used as CCC reference clock input).

This Errata cannot be detected in any functional simulation, and can only be detected in silicon testing

Solution:

This Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to Libero SoC 11.1 SP3 or newer version, and re-run **Compile and Layout**.

2.11 NVM Ready Bit in eNVM Status Register Can Generate a False READY Signal

If you send an instruction to the eNVM controller and then start polling the READY signal (Bit 0 of the eNVM Status register) to check when the eNVM controller is ready for the next function, the first assertion of the READY signal occurs when the eNVM controller is not yet ready, resulting in the generation of a false READY signal. However, the immediate next assertion of the READY signal correctly indicates that the eNVM controller is ready.

Workaround:

Add an extra eNVM Status bit read that polls/reads the eNVM Status bit twice as READY.

2.12 Power-Up Digest Is Not Supported

Workaround:

Use NVM Data Integrity Check System service after the device is switched ON, and check the data integrity.

2.13 Programming of the eNVM Must Only Occur as Part of a Bitstream Also Containing the FPGA Fabric

The Bitstream Configuration Dialog Box in the Libero SoC allows the user to program eNVM and the FPGA fabric separately. However, for the current production of IGLOO 2 FPGAs, the user needs to program the eNVM along with the FPGA fabric. The fabric can be programmed separately if needed.

Solution:
This Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to the Libero SoC 11.1 SP3 or newer version, and re-run **Compile and Layout**.

2.14 Updating eNVM from the FPGA Fabric Requires Changes in the NV_FREQRNG Register

When updating the eNVM from the FPGA fabric, NV_FREQRNG register must be changed from 0x07(default) to 0x0F, eNVM reads are not affected.

2.15 SYSCTRL_RESET_STATUS Macro Is Not Supported

2.16 Zeroization Is Not Supported

2.17 PCIe Hot Reset Support Requires a Soft Reset Solution

On the IGLOO 2 devices, a PCIe® Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

Workaround:
The application note *AC437: Implementing PCIe Reset Sequence in SmartFusion 2 and IGLOO 2 Devices* describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases:

- At Gen1 rates, there are no violations
- At Gen2 rates, there are two PCIe CV violations:
  - Testcase 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg)

2.18 The DDR I/Os in M2GL050 (T,TS)-FG896 Are Non-compliant with the DDR3 Standard

The DDR controller in the M2GL050-FG896 device is non-compliant with the DDR3 standard. For additional information, contact Microchip by creating a new case at microchip.my.site.com/s/newcase.

2.19 For S (Security) Grade Devices, User Must Not Enable Write Protection for Protected 4 K Regions, Also Known as Special Sectors in the eNVM

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write, these regions are known as Protected 4 K Regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

2.20 PCIe Hard IP Core Receive FIFO May Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore Subsequent PCIe Traffic

A condition has been identified with the IGLOO 2 PCIe interface where the PCIe hard IP block's receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem, and cause the PCIe core to ignore subsequent PCIe traffic. This only occurs under very specific conditions as outlined in the associated PCN SYST-18UJME493.

Workaround:
This failure mechanism is isolated to the PCIe hard IP core within the FPGA device, where it cannot be corrected. To avoid this issue, the posted receive buffer must not become full. This can be accomplished using one of the options in PCN SYST-18UJME493. For more details, refer to this PCN: SmartFusion 2, IGLOO 2 and RTG4 FPGA PCIe Receive FIFO Full.

3. Usage Guidelines for IGLOO 2 Devices

Microchip recommends the following conditions for the IGLOO 2 device usage.

3.1 Programming Support

There may be package dependencies that may not expose certain programming interfaces. For device/package specific features, refer to the *DS0124: IGLOO 2 Pin Descriptions Datasheet*.

Table 3-1. Revision 0 and Revision 1 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SC_SPI	SPI_0	SC_SPI	SPI_0
M2GL050 (T,TS)	Yes	Yes	No	No	No	No

Table 3-2. Revision 2 Device

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SC_SPI	SPI_0	SC_SPI	SPI_0
M2GL050 (T,TS)	Yes	Yes	Yes	No	Yes	No

3.2 SHA-256 System Service

Microchip recommends the message required to be on byte boundary when using SHA-256 System Service for the IGLOO 2 devices.

3.3 Accessing the PCIe Bridge Register in High-speed Serial Interface

The PCIe Bridge registers must not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 µs after the device is powered up. Wait for 200 µs before accessing the PCIe Bridge registers.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	05/2024	The following is the summary of changes made in revision A: • The document was updated to Microchip template. • The document number was changed from 55900200 to DS80001127A. • Updated Table 1-1 to add row 20. • Added errata item 2.20 PCIe hard IP core receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem and cause the PCIe core to ignore subsequent PCIe traffic. • Replaced the Microsemi links with Microchip links throughout the document.
1.3	04/2016	Added Errata item 2.19 For S (Security) Grade Devices, User Must Not Enable Write Protection for Protected 4 K Regions, Also Known as Special Sectors in the eNVM.
1.2	01/2016	Updated Table 3-1 and Table 3-2: Auto Programming and 2-Step IAP use SC_SPI programming interface.
1.1	01/2016	The following is the summary of changes made in revision 1.1: • Added information about Revision 2 of the M2GL050 device. • Added Errata item 2.18 The DDR I/Os in M2GL050 (T, TS)-FG896 are Non-compliant with the DDR3 Standard. • Added Table 3-2.
1.0	06/2015	Combined all M2GL050 (T,TS) device Errata.

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic

ISBN: 978-1-6683-4631-0

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	**Australia - Sydney** Tel: 61-2-9868-6733	**India - Bangalore** Tel: 91-80-3090-4444	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393
Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455	**China - Beijing** Tel: 86-10-8569-7000	**India - New Delhi** Tel: 91-11-4160-8631	**Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829
Austin, TX Tel: 512-257-3370	**China - Chengdu** Tel: 86-28-8665-5511	**India - Pune** Tel: 91-20-4121-0141	**Finland - Espoo** Tel: 358-9-4520-820
Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088	**China - Chongqing** Tel: 86-23-8980-9588	**Japan - Osaka** Tel: 81-6-6152-7160	**France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79
Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075	**China - Dongguan** Tel: 86-769-8702-9880	**Japan - Tokyo** Tel: 81-3-6880- 3770	**Germany - Garching** Tel: 49-8931-9700
Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924	**China - Guangzhou** Tel: 86-20-8755-8029	**Korea - Daegu** Tel: 82-53-744-4301	**Germany - Haan** Tel: 49-2129-3766400
Detroit Novi, MI Tel: 248-848-4000	**China - Hangzhou** Tel: 86-571-8792-8115	**Korea - Seoul** Tel: 82-2-554-7200	**Germany - Heilbronn** Tel: 49-7131-72400
Houston, TX Tel: 281-894-5983	**China - Hong Kong SAR** Tel: 852-2943-5100	**Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906	**Germany - Karlsruhe** Tel: 49-721-625370
Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380	**China - Nanjing** Tel: 86-25-8473-2460	**Malaysia - Penang** Tel: 60-4-227-8870	**Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44
Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800	**China - Qingdao** Tel: 86-532-8502-7355	**Philippines - Manila** Tel: 63-2-634-9065	**Germany - Rosenheim** Tel: 49-8031-354-560
Raleigh, NC Tel: 919-844-7510	**China - Shanghai** Tel: 86-21-3326-8000	**Singapore** Tel: 65-6334-8870	**Israel - Hod Hasharon** Tel: 972-9-775-5100
New York, NY Tel: 631-435-6000	**China - Shenyang** Tel: 86-24-2334-2829	**Taiwan - Hsin Chu** Tel: 886-3-577-8366	**Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781
San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270	**China - Shenzhen** Tel: 86-755-8864-2200	**Taiwan - Kaohsiung** Tel: 886-7-213-7830	**Italy - Padova** Tel: 39-049-7625286
Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078	**China - Suzhou** Tel: 86-186-6233-1526	**Taiwan - Taipei** Tel: 886-2-2508-8600	**Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340
	China - Wuhan Tel: 86-27-5980-5300	**Thailand - Bangkok** Tel: 66-2-694-1351	**Norway - Trondheim** Tel: 47-72884388
	China - Xian Tel: 86-29-8833-7252	**Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Poland - Warsaw** Tel: 48-22-3325737
	China - Xiamen Tel: 86-592-2388138		**Romania - Bucharest** Tel: 40-21-407-87-50
	China - Zhuhai Tel: 86-756-3210040		**Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91
			Sweden - Gothenberg Tel: 46-31-704-60-40
			Sweden - Stockholm Tel: 46-8-5090-4654
			UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820