



Product Change Notification / SYST-11BSHV285

Date:

12-Oct-2022

Product Category:

Ethernet Switches

PCN Type:

Document Change

Notification Subject:

ERRATA - KSZ8567R Silicon Errata and Data Sheet Clarification

Affected CPNs:

[SYST-11BSHV285_Affected_CPN_10122022.pdf](#)

[SYST-11BSHV285_Affected_CPN_10122022.csv](#)

Notification Text:

SYST-11BSHV285

Microchip has released a new Errata for the KSZ8567R Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [KSZ8567R Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: This revision includes the following changes

Silicon Errata Issues	Added note regarding configuration of PHY MMD registers.
Module 1	Added the following text to Work Around description: "Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto[negotiation disabled by writing to register 0xN100- 0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above."
Note 1	Updated Module 1's final data address from "0x2001" to "0x2000". Also added note regarding this change.
Module 3	Updated title of section from "Default RGMII ingress timing

	does not comply with the RGMII specification” to “Port 6 Default RGMII ingress timing does not comply with the RGMII specification”
Module 4	Entire Module section rewritten for clarity
Module 6	Added 4 additional addresses to Work Around sec[1]tion: 0xN130 - 0xN133 0xN134 - 0xN137 0xN138 - 0xN13B 0xN13C - 0xN13F
Module 15	Text for Method 2 has been updated from “To detect transmitter lock up, the software should monitor the TxByteCnt (MIB Index 0x81) and the RxByteCnt (MIB Index 0x80). If the RxByteCnt is incrementing but the TxByteCnt remains the same, the software should perform a hard reset of the switch” to “To detect transmitter lockup, see the work around sec[1]tion of Module x: Transmission halt with Half-Duplex and VLAN.”
Module 16	Entire Module section rewritten for updated solution.
Module 18	New Module for I2C usage.
Module 19	New Module for Half-Duplex and VLAN interaction.
Module 20	New Module for Frame Length Check feature.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Oct 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[KSZ8567R Silicon Errata and Data Sheet Clarification](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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