Product Change Notification / SYST-02OGIB823

Date:

14-May-2024

Product Category:

8-Bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

AVR64DB28/32/48/64 Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-02OGIB823_Affected_CPN_05142024.pdf
SYST-02OGIB823_Affected_CPN_05142024.csv

Notification Text:

SYST-02OGIB823

Microchip has released a new Document for the AVR64DB28/32/48/64 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at AVR64DB28/32/48/64 Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change:

• General editorial updates
• Added Silicon Revision: B1
• Added Errata:
– Device: 2.2.2. Write Operation Lost if Consecutive Writes to Specific Address Spaces
– NVMCTRL: 2.5.2. NVM_EEPROM_ERASE Command does Not Respect Write Protect
– SPI: 2.6.1. Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices
– TCD: 2.9.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used
– TWI: 2.10.1. Flush Non-Functional
– USART: 2.11.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field
• Added Data Sheet Clarifications:
– SPI: 3.2.1. SPI - Serial Peripheral Interface
– SPI: 3.2.2. SPI - Serial Peripheral Interface

– Electrical Characteristics: 3.5.1. I/O Pin Characteristics
– Electrical Characteristics: 3.5.3. SPI

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 14 May 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AVR64DB28/32/48/64 Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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