

LAN9645xS/LAN9645xF Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the LAN9645xS/LAN9645xF family of devices, which includes the following:

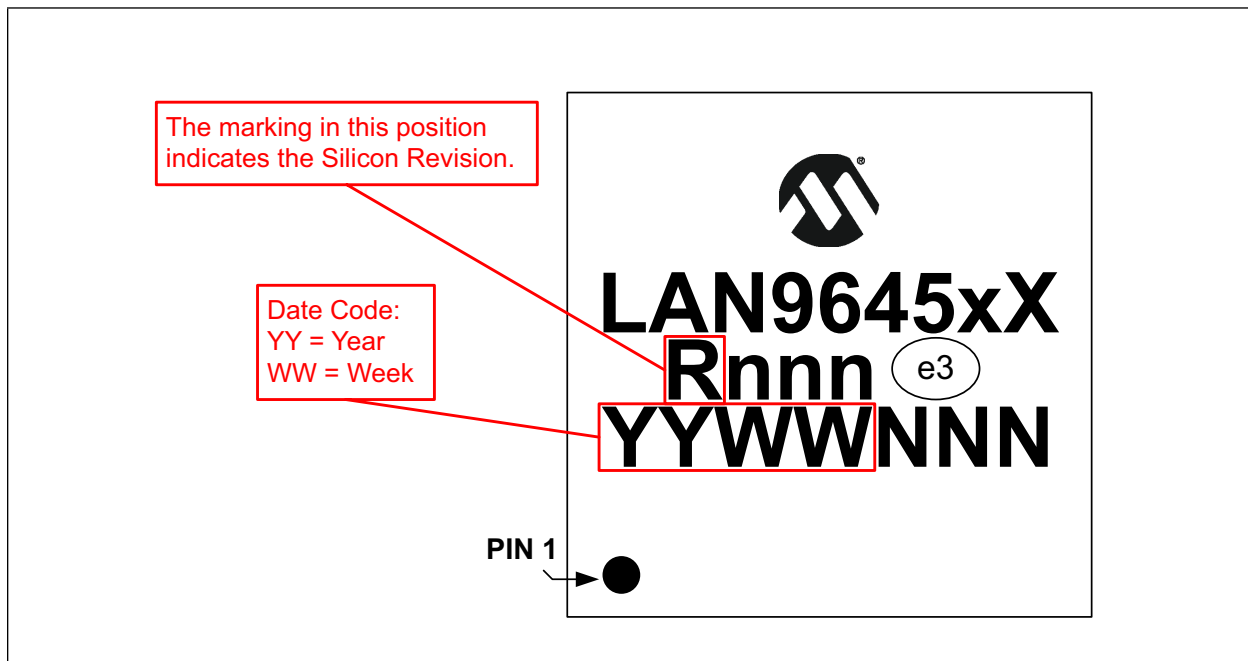
- LAN96455S, LAN96455F
- LAN96457S, LAN96457F
- LAN96459S, LAN96459F

The silicon errata discussed in this document are for silicon revisions listed in [Table 1](#). The silicon revision can be determined by the device's top marking as indicated in [Figure 1](#). A summary of LAN9645xS/LAN9645xF silicon errata is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

| Part Number | Revision |
|--|----------|
| LAN96455S, LAN96455F, LAN96457S, LAN96457F, LAN96459S, LAN96459F | A0 |

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of [Figure 1](#) is to detail the top markings of an example part and highlight the location of the date code. Other top marking values may differ (lot codes, location of manufacture, etc.).

LAN9645XS/LAN9645XF

TABLE 2: SILICON ISSUE SUMMARY

| Item Number | Silicon Issue Summary | Affected SKU |
|-------------|---|--------------|
| 1. | MMD 3.1 PCS Status Register shows faulty LPI indications | ALL |
| 2. | First frame received in 10BASE-T mode may be corrupted | ALL |
| 3. | Preemption in 100Mbit mode does not work correctly on internal CuPHYs | ALL |
| 4. | 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification | ALL |

Silicon Errata Issue

Module 1: MMD 3.1 PCS Status Register shows faulty LPI indications

DESCRIPTION

Received Low Power IDLE (LPI) indications in bits 8 and 10 of register MMD 3.1 PCS Status are invalid.

END USER IMPLICATIONS

These LPI status registers are typically used for reporting the Energy Efficient Ethernet power state of a link. They do not impact actual EEE operation of the PHY.

Work around

None.

PLAN

This erratum is currently under investigation.

Module 2: First frame received in 10BASE-T mode may be corrupted

DESCRIPTION

When operating the PHY in 10BASE-T link, the first frame received may contain data errors due to a receiver initialization error. All frames subsequent to the first frame are received normally.

END USER IMPLICATIONS

This error only occurs in 10BASE-T links and only affects the first frame received after link establishment. It has no other impact. The error is random in occurrence and cannot be predicted upon 10BASE-T link establishment. When the error occurs, the received frame will output on the QSGMII interface of the PHY but will result in a frame error at the host MAC.

Work around

None.

PLAN

This erratum will not be fixed in a future revision.

Module 3: Preemption in 100Mbit mode does not work correctly on internal CuPHYs

DESCRIPTION

Preemption in 100Mbit mode does not work correctly on the internal CuPHYs.

END USER IMPLICATIONS

Using preemption in 100Mbit mode on the internal CuPHYs may lead to corrupted Ethernet packets.

Work around

Use preemption in 1Gbit/s operation. Preemption is working correctly on the internal CuPHYs at 1Gbit/s.

PLAN

This erratum is currently under investigation.

Module 4: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmitter Distortion exceeds the <10mV limit indicated in the IEEE specification.

END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following Application Note has more details regarding the Gigabit Transmit Distortion test:

<https://www.microchip.com/en-us/application-notes/an3455>

Work around

None.

PLAN

This erratum will not be corrected in a future silicon revision.

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APPENDIX A: DOCUMENT REVISION HISTORY

| Revision Level & Date | Section/Figure/Entry | Correction |
|------------------------|----------------------------|--------------------|
| DS80001187B (10-28-25) | Module 4 . | Added new erratum. |
| DS80001187A (10-15-25) | All | Initial release |

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