PIC32CZ CA70/MC70 Family Silicon Errata and Data Sheet Clarifications

PIC32CZ CA70/MC70 Family

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The PIC32CZ CA70/MC70 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001825**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in Silicon Errata Summary.

The errata described in this document will be addressed in future revisions of the PIC32CZ CA70/MC70 silicon family.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CZ CA70/MC70 Family Silicon Device Identification

Devices	Device ID (CHIPID_CIDR[31:0])	Mask Revision (CHIPID_CIDR[4:0]) A0
PIC32CZ2051CA70144	0xA1AF_0E0x	0x0
PIC32CZ2051CA70100	0xA1AF_0E0x	0x0
PIC32CZ2051CA70064	0xA1AF_0E0x	0x0
PIC32CZ2051MC70100	0xA1BF_0E0x	0x0
PIC32CZ2051MC70064	0xA1BF_0E0x	0x0

Note:

1. Refer to the “Chip Identifier (CHIPID)” section in the current device data sheet (DS60001825**D**) for a detailed information on Chip Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Errata Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Errata Number	Summary	Affected Silicon Revisions
				A0
Device	GMAC registers corruption on HSMCI, PMC, XDMAC, and USBHS Registers	2.1.1	Values for the HSMCI, PMC, XDMAC, and USBHS registers with the same offset than some specific GMAC registers, are not read out correctly.	X
XDMAC	Byte and Half-Word Accesses	2.2.1	If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.	X
XDMAC	Request Overflow Error	2.2.2	When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the Request Overflow Error Interrupt Status (ROIS) bit in the XDMAC_CISx register is set incorrectly.	X
USBHS	64-pin TQFP Package	2.3.1	The High-Speed USB (USBHS) module does not function in 64-pin TQFP e-pad package devices.	X
Power	Backup Power	2.4.1	Power consumption is high in Backup mode with backup SRAM On.	X
PORT	GPIO	2.5.1	GPIOs with a pull-up reset state may briefly dip low during reset if they were configured as output-high.	X

2. PIC32CZ CA70/MC70 Errata Issues

The following errata issues apply to the PIC32CZ CA70/MC70 silicon family of devices.

2.1. Device

2.1.1. GMAC Registers Corruption on HSMCI, PMC, XDMAC, and USBHS Registers

Whenever there is any non-zero value in the following registers, values for registers with the same offset in other peripherals (HSMCI, PMC, XDMAC, and USBHS) are not read out correctly:

- 0x0500-0x055C (GMAC Screening Type 1/2 Registers) – GMAC_ST1RPQx or GMAC_ST2RPQx
- 0x06E0-0x06EC (GMAC Screening Type 2 Ether Type Registers) – GMAC_ST2ERx
- 0x0700-0x07BC (GMAC Screening Type 2 Compare Registers) – GMAC_ST2CW0x and GMAC_ST2CW1x

Workaround

While reading the affected registers from other peripherals, the user needs to ensure that the GMAC register with the same offset address have a value of 0x00000000.

Affected Silicon Revisions

A0						
X						

2.2. Extended DMA Controller (XDMAC)

2.2.1. Byte and Half-Word Accesses

If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.

Workaround

The user can resolve this issue by setting the source and destination addressing mode to use microblock and data striding with microblock stride set to 0 and data stride set to -1.

Affected Silicon Revisions

A0						
X						

2.2.2. Request Overflow Error

When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the Request Overflow Error Interrupt Status (ROIS) bit in the XDMAC_CISx register is set incorrectly. The memory transfer proceeds normally and the data area is correctly transferred.

Workaround

Configure the PERID bit to an unused peripheral ID.

Affected Silicon Revisions

A0						
X						

2.3. USB High-Speed (USBHS)

2.3.1. 64-Pin TQFP Package

The High-Speed USB (USBHS) module does not function in 64-pin TQFP e-pad package devices.

Workaround

None.

Affected Silicon Revisions

A0						
X						

2.4. Power

2.4.1. Backup Power

Backup mode with backup SRAM retention is not supported. Enabling this feature (SUPC_MR.BKUPRETON = 1) results in excessive power consumption. This may exceed device specifications and cannot be effectively characterized across devices or operating conditions.

Workaround

None.

Affected Silicon Revisions

A0						
X						

2.5. PORT

2.5.1. GPIO

When a reset event occurs (Software Reset, External Reset/User Reset, Watchdog Reset), a GPIO that has a pull-up as its reset state and is configured as Output-HIGH may momentarily glitch low during the reset transition. The pin may dip low for approximately 5–20 ns, and then returns to a stable high level within about 5–7 µs.

Workaround

None.

Affected Silicon Revisions

A0						
X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001825**D**):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are currently no data sheet clarifications to report.

4. Revision History

Revision E - February 2026

The following updates were performed for this revision:

- Updated the verbiage for the following errata:
  - Power: 2.4.1 Backup Power
- Added a new errata:
  - PORT: 2.5.1 GPIO

Revision D - August 2025

The following updates were performed for this revision:

- Added the following Errata:
  - Power: 2.4.1 Backup Power

Revision C - March 2025

The following updates were performed for this revision:

- Added the following Errata:
  - USBHS: 2.3.1 64-Pin TQFP Package

Revision B - December 2024

The following updates were performed for this revision:

- Updated all references to the data sheet to reflect Data Sheet Revision D
- Removed the NDA Confidential watermark to prepare for public release

Revision A - November 2024

This is the initial released version of the document.

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