PIC18F44/45/54/55Q71

PIC18F44/45/54/55Q71 Silicon Errata and Data Sheet Clarifications

The PIC18F44/45/54/55Q71 devices that you have received conform functionally to the current device data sheet (DS40002350**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F44/45/54/55Q71 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		A1
PIC18F44Q71	0x77A0	0xA001
PIC18F45Q71	0x77E0	0xA001
PIC18F54Q71	0x7820	0xA001
PIC18F55Q71	0x7860	0xA001

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q71 Family Programming Specification"** (DS40002306) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				A1
Universal Timer Module	UTMR	1.1.1	Dead zone exists in level-triggered Start/Reset condition when ERS signal is generated due to an SFR access	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.2.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X
Electrical Specifications	Maximum Input Leakage Current	1.3.1	Increased Maximum Input Leakage Current Specification on 8-bit Digital-to-Analog Converter (DAC) V_{REF-} pins	X
Universal Asynchronous Receiver Transmitter	UART	1.4.1	UART TXDE signal may go low before the STOP bit has been entirely transmitted.	X
PIC18 CPU	FSR Shadow Registers	1.5.1	FSR Shadow Registers are not Writable	X
I^2C	Multi-Master Mode	1.6.1	Multi-Master mode will cause bus failures.	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `'b11` or RESET = `'b01`) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

A1
X

1.2 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.2.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level, while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A1
X

1.3 Module: Electrical Specifications

1.3.1 Increased Maximum Input Leakage Current Specification on 8-bit Digital-to-Analog Converter (DAC) V_{REF-} pins

The 8-bit DAC V_{REF-} pins on this device have a higher sensitivity to ESD than other I/O pins. An ESD event may result in higher Leakage Current than specified (Parameter D340 in the device datasheet). This increased maximum Input Leakage Current is only applicable to the 8-bit DAC V_{REF-} pins. It is recommended that the increased ESD sensitivity on these pins be taken into consideration during design.

The table below shows the updated Input Leakage Current electrical specification on these pins:

Table 1-1. IO PORTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
Input Leakage Current(1)							
D340	I_{IL}	I/O PORTS	—	±5	±125	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C
		I/O PORTS (for 8-bit DAC V_{REF-} pins)	**—**	**± 5**	**± 2000**	**nA**	**$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C**
D341		I/O PORTS	—	±5	±1000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 125°C
		I/O PORTS (for 8-bit DAC V_{REF-} pins)	**—**	**± 5**	**± 2000**	**nA**	**$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 125°C**
D342		$\overline{MCLR}$(2)	—	±50	±200	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, 85°C

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes:

1. Negative current is defined as current sourced by the pin.
2. The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Work around

None.

Affected Silicon Revisions

A1
X

1.4 Module: Universal Asynchronous Receiver Transmitter (UART)

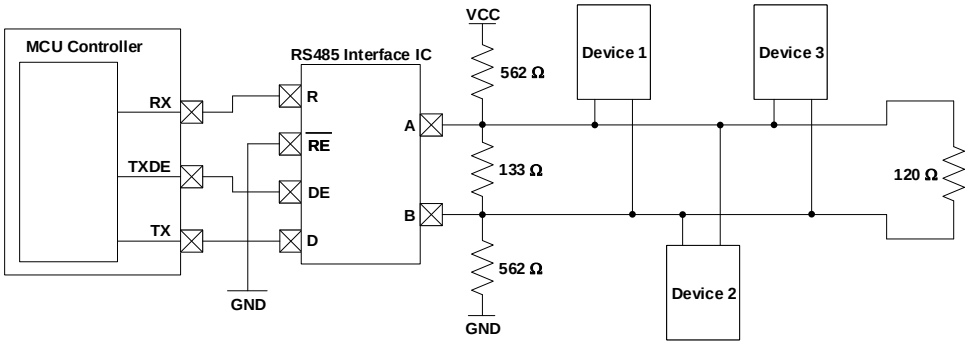
1.4.1 UART TXDE Signal May go Low Before The STOP Bit Has Been Entirely Transmitted.

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

In order to ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below show an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations, and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

A1
X

1.5 Module: PIC18 Core

1.5.1 FSR Shadow Registers are not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below)
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0])
5. Write FSRxH
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1
X

1.6 Module: Inter-Integrated Circuit (I^2C)

1.6.1 Operating in Multi-Master Mode Will Cause Bus Failures

If operating in Multi-Master Mode and a second master drives SDA low at the same time the Start bit is generated, the module will fail to go into Master mode, but will continue to send an address and data as if it won arbitration. I2CCNT fails to decrement, and the module will remain in this state until a bus timeout occurs or the device is reset.

Work around

None.

Affected Silicon Revisions

A1
X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002350**C**):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
A	3/2023	Initial document release. Includes silicon issues 1.1.1 (Universal Timer Module), 1.2.1 (ICSP), 1.3.1 (Electrical Specification), 1.4.1 (UART), 1.5.1 (PIC18 CPU) and 1.6.1 (I2C).

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