PIC32CK SG01/GC01 Family Silicon Errata and Data Sheet Clarifications

PIC32CK SG01/GC01

Introduction

The PIC32CK SG01/GC01 family of devices that you have received conform functionally to the current device data sheet (DS60001795**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32CK SG01/GC01 family of devices.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous, and current.

Data Sheet clarifications and corrections (if applicable) are located in the section Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. PIC32CK SG01/GC01 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])
		A0
PIC32CK2051GC01064	0xX9501053	0x0
PIC32CK2051GC01100	0xX9502053	
PIC32CK2051GC01144	0xX9503053	
PIC32CK2051SG01064	0xX9504053	
PIC32CK2051SG01100	0xX9505053	
PIC32CK2051SG01144	0xX9506053	
PIC32CK1025GC01064	0xX9519053	
PIC32CK1025GC01100	0xX951A053	
PIC32CK1025GC01144	0xX951B053	
PIC32CK1025SG01064	0xX951C053	
PIC32CK1025SG01100	0xX951D053	
PIC32CK1025SG01144	0xX951E053	

Table 2. Silicon DEVREV Values for Devices with 512 KB/256 KB Data Memory

Devices	SRAM Memory Size	Device ID	Silicon Revision ID
PIC32CK2051GC01064	512	0xX9501053	0x0
PIC32CK2051GC01100	512	0xX9502053	0x0
PIC32CK2051GC01144	512	0xX9503053	0x0
PIC32CK2051SG01064	512	0xX9504053	0x0
PIC32CK2051SG01100	512	0xX9505053	0x0
PIC32CK2051SG01144	512	0xX9506053	0x0
PIC32CK1025GC01064	256	0xX9519053	0x0
PIC32CK1025GC01100	256	0xX951A053	0x0
PIC32CK1025GC01144	256	0xX951B053	0x0
PIC32CK1025SG01064	256	0xX951C053	0x0
PIC32CK1025SG01100	256	0xX951D053	0x0
PIC32CK1025SG01144	256	0xX951E053	0x0

Table 3. Silicon DEVREV Values for Devices with 128 KB Data Memory

Devices	SRAM Memory Size	Device ID	Silicon Revision ID
PIC32CK1012GC01048	128	0xX9580053	0x0
PIC32CK1012GC01064	128	0xX9581053	0x0
PIC32CK1012GC01100	128	0xX9582053	0x0
PIC32CK1012SG01048	128	0xX9583053	0x0
PIC32CK1012SG01064	128	0xX9584053	0x0
PIC32CK1012SG01100	128	0xX9585053	0x0

Note: Refer to the “Device Service Unit” chapter in the current device data sheet (DS60001795**H**) for a detailed information on Device Identification and Revision IDs for your specific device.

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1. Silicon Issue Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions	
				SRAM	A0
AC	RESERVED	2.1.1	RESERVED	128	X
				256	X
				512	X
AC	Analog Mux Short	2.1.2	When WRCONFIG.PMUX = 0x1 for PA06 and PA09/PA07 and PA10, a short can occur.	128	X
				256	X
				512	X
CAN	Debug Message Status Register	2.2.1	The CAN register field RXF1S.DMS is not cleared by setting CCCR.CCE.	128	X
				256	X
				512	X
CAN	Sequential CAN Message TX	2.2.2	Message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID.	128	X
				256	X
				512	X
CAN	TX Buffers/TX Queue	2.2.3	Incomplete description in Section 3.5.2 Dedicated Tx Buffers and 3.5.4 Tx Queue of the *M_CAN User's Manual* related to transmission from multiple buffers configured with the same Message ID.	128	X
				256	X
				512	X
DMA	CRC	2.3.1	DMA Channel CRCROUT and CRCXOR settings are applied to CRC data only, and not applied on CRC Append Data.	128	X
				256	X
				512	X
DMA	BYTORD	2.3.2	Byte re-ordering settings incorrectly applied to descriptor data.	128	X
				256	X
				512	X
DMA	Pattern Match	2.3.3	Pattern Match feature doesn't work when channel set to Fixed Word Address Increment.	128	X
				256	X
				512	X
DMA	IP Header Checksum Mode	2.3.4	crcmd 7 is not working correctly with ras = 3.	128	X
				256	X
				512	X
DMA	Descriptor Loading	2.3.5	CHCTRLA.ENABLE = 1 and LLEN = 1 does load the descriptor.	128	X
				256	X
				512	X
DMA	Linked List Event System Abort	2.3.6	Event abort issues in Linked List Operation mode.	128	X
				256	X
				512	X
DMA	When CRCEN = 1 output data is broken	2.3.7	CRC in fixed read addressing modes is broken (CHCTRLBn.RAS).	128	X
				256	X
				512	X
DMA	Event System and Pattern Match Aborts Fail to Clear Internal Flag	2.3.8	If using pattern match or event system aborts, then Channel Event Outputs cannot be used.	128	X
				256	X
				512	X
MCLK	CLKDIV	2.4.1	PSLVERR is generated when RSVD values are written to the CLKDIV registers.	128	X
				256	X
				512	X
MCRAMC	RESERVED	2.5.1	RESERVED	128	X
				256	X
				512	X

Table 1-1. Silicon Errata Summary (continued)

Module	Feature	Item #	Issue Summary	Affected Revisions	
				SRAM	A0
NVMCTRL	RESERVED	2.6.1	RESERVED	128	X
				256	X
				512	X
NVMCTRL	RESERVED	2.6.2	RESERVED	128	X
				256	X
				512	X
NVMCTRL	PFM	2.6.3	Reads to the same address in different NVR regions fail (from same bus master with ADRWS = 1).	128	X
				256	X
				512	X
NVMCTRL	CRCMLEN	2.6.4	CRCMLEN active bits can exceed the PFM size for devices with Flash panels smaller than 8M Bytes.	128	X
				256	X
				512	X
NVMCTRL	CRC	2.6.6	FCR does not check addresses to verify they fall within a valid Flash memory region.	128	X
				256	X
				512	X
NVMCTRL	ECCCTRL	2.6.7	The ECC mode settings 0x10 and 0x01 are not functional for all possible read/write operations.	128	X
				256	X
				512	X
NVMCTRL	DBGCTRL.DBGECC	2.6.8	Bus errors reported to debugger when FCR -> DBGCTRL.DBGECC = 0 (NOERR).	128	X
				256	X
				512	X
NVMCTRL	Fault Address Capture	2.6.9	Fault capture address is incorrect when fault is unveiled by internal CRC read.	128	X
				256	X
				512	X
PDEC	Error Flags	2.7.1	An Error Detection (INTFLAG.ERR = 1) updates the STATUS Error flags (HERR, WINERR,MPERR, IDXERR, QERR) with a variable delay.	128	X
				256	X
				512	X
PDEC	Direction Change	2.7.2	A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay.	128	X
				256	X
				512	X
PDEC	Hall Mode	2.7.3	A Windows Error (WINERR) flag can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0).	128	X
				256	X
				512	X
PDEC	Hall Mode	2.7.4	In HALL mode, the WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection.	128	X
				256	X
				512	X
PDEC	QDEC Mode	2.7.5	In QDEC mode (X4), MC0/MC1 event triggered wrongly prior to angular counter reaching LSB of CC0 and CC1.	128	X
				256	X
				512	X
SDHC	PSR.CARDINS	2.8.1	The card detect status bit and downstream interrupt flag bits are updated only after internal clock is enabled.	128	X
				256	X
				512	X
SQI	DMA	2.9.1	SQI Dual and Quad mode write modes are inoperable.	128	X
				256	X
				512	X
SQI	DMA	2.9.2	When using a DMA descriptor with the status polling option bit set, the PKTCOMPIF interrupt flag will set before the status check has completed.	128	X
				256	X
				512	X

Table 1-1. Silicon Errata Summary (continued)

Module	Feature	Item #	Issue Summary	Affected Revisions	
				SRAM	A0
USB	RESERVED	2.10.1	RESERVED	128	X
				256	X
				512	X
USB	APB	2.10.2	Addressing some PHY registers set the APB clock request permanently.	128	
				256	X
				512	X
TRAM	DRP	2.11.1	When Data Scrambling is enabled, accessing TRAM during DRP routine can lead to corrupted (read or write) data.	128	X
				256	X
				512	X
SERCOM	LIN	2.12.1	LIN Host Mode adds non-conformal delay between break and sync bits.	128	X
				256	X
				512	X
SERCOM	LIN - Two Stop Bits	2.12.2	Two stop bits mode is not supported in SERCOM LIN operation.	128	X
				256	X
				512	X
SERCOM	I2C	2.12.3	Back-to-Back writes to the DATA FIFO generates pslverr when in I^2C Host mode.	128	X
				256	X
				512	X
SERCOM	SPI/I2C Client Mode	2.12.4	SYNCBUSY.ENABLE can get stuck if GCLK is slower than APB clock.	128	X
				256	X
				512	X
FREQM	STATUS.BUSY	2.13.1	If during measurement slot, the STATUS.BUSY will never de-assert and DONE interrupt will not be raised.	128	X
				256	X
				512	X
OSCCTRL	DFLL48M	2.14.1	When the DFLL48M is used dynamically, tuning can be corrupted when re-enabling.	128	X
				256	X
				512	X
NMI	GCLK	2.15.1	If NMI is configured in synchronous edge detection mode, spurious interrupts may occur after a software reset.	128	X
				256	X
				512	X
TMR	Periodic Daily Event	2.16.1	Periodic Daily Event is getting generated at 23:59:58 instead of 23:59:59 in Mode 2.	128	X
				256	X
				512	X
IXS	Frame Detection Error	2.17.1	Race condition between FSYNC and SCK.	128	X
				256	X
				512	X
IXS	I8S	2.17.3	When operating in I8S left/right justified client mode, data from the client is not transmitted properly and is erroneous.	128	X
				256	X
				512	X
SUPC	ADC VREF	2.18.1	Unable to measure Temp Sensor output using ADC in normal mode.	128	
				256	X
				512	X
SUPC	OFFSTDBY	2.18.2	Turning off VREGSW[N-1] during Standby mode will cause PORCORE Reset.	128	
				256	X
				512	X
EVSYS	BUSYCH	2.19.1	The CHBUSY flag never reset upon software events in synchronous/ resynchronized path modes with event detection on falling edges.	128	X
				256	X
				512	X

Table 1-1. Silicon Errata Summary (continued)

Module	Feature	Item #	Issue Summary	Affected Revisions	
				SRAM	A0
EVSYS	OVR	2.19.2	Overrun interrupt flag may be incorrectly set upon software events in synchronous/resynchronized path modes with event detection on both rising and falling edges.	128	X
				256	X
				512	X
GPIO	PB04	2.20.1	Current leakage on the PB04 pin.	128	X
				256	X
				512	X
USBHS	USBHS PHY	2.21.1	USBHS PHY port I/O Toggle generates noise on the USB.	128	
				256	X
				512	X
XOSC	STDBY	2.22.1	CP0 should be kept enable when XOSC is running in Standby mode.	128	X
				256	X
				512	X
XOSC32K	Duty Cycle	2.23.1	SOSC (XOSC32K) duty cycle is >75% for VDD = 3.63V and at hot temperature >= 125°C.	128	X
				256	X
				512	X
XOSC32K	CP0	2.23.2	SOSC (XOSC32K) not working for VDDIO < 2.4V at hot temperature when charge pump is enabled (CP0).	128	X
				256	X
				512	X
ETH	TX CLK	2.24.1	Ethernet data integrity error when toggling PC01/PC02 near ETH_TX_CLK signal (PC00).	128	X
				256	X
				512	X

Notes:

- Cells with ‘X’ indicate the issue is present in this revision of the silicon.
- Cells with ‘– ’ indicate this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

2. Silicon Errata Issues

The following errata issues apply to the PIC32CK SG01/GC01 family of devices.

Notes:

- Cells with 'X' indicate the issue is present in this revision of the silicon.
- Cells with '– ' indicate this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

2.1. AC

2.1.1. RESERVED

2.1.2. Analog Mux Short

When PINCFGn.MUXEN = 0x1 and WRCONFIG.PMUX = 0x1 for the PA06/AC_AIN0 and PA09/ADC_VINP5 pins, or for the PA07/AC_AIN1 and PA10/ADC_VINP6 pins, a potentially destructive short can occur when the AC selects AC_AIN0 or AC_AIN1 as an input.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.2. Controller Area Network (CAN)

2.2.1. Debug Message Status Register

The CAN register field RXF1S.DMS is not cleared by setting CCCR.CCE.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.2.2. Sequential CAN Message TX

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests. The conditions in which multiple Tx Buffers are configured with the same Message ID, the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

Workaround

Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.2.3. TX Buffers/TX Queue

If the dedicated Tx buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

Workaround

If a defined order of transmission is required, the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3. DMA

2.3.1. CRC

DMA Channel, CRCROUT and CRCXOR, settings are applied to CRC data only, and not applied on CRC Append Data.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.2. BYTORD

DMA.BYTORD: The DMA byte reordering settings for CHCTRLBk.BYTORD[1:0] and CHCTRLBk.WBOEN are incorrectly applied to the descriptor data. The byte reordering feature is non-functional.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.3. Pattern Match

When using pattern match feature on a channel with CHCTRLBk.WAS set to 101 (FIXED_WORD_ADDR_INC), incorrect data may be written to the destination. This is the only setting of CHCTRLBk.WAS that exhibits this issue.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.4. IP Header Checksum Mode

Using CRCMD = 7 (IP header checksum mode) should be avoided on v1. The incorrect checksum can be calculated when RAS = 2, 3, or 5.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.5. Descriptor Loading

CHCTRLA.ENABLE = 1 and LLEN = 1 does not load the description.

Workaround

- If software writes LLEN = 1 and ENABLE = 0 (same write), load the next descriptor.
- If software writes LLEN = 1 and ENABLE = 1 (same write), load the next descriptor.
- If software writes LLEN = 0 and ENABLE = 1 (same write), channel completes block transfer, and clears enable. Software should not write LLEN = 1 until after this block transfer completes.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.6. Linked List Event System Abort Issue

DMA Event abort issue in Linked List Operation (CHEVCTRLn. EVAUXACT[1:0] = 11.

Workaround

Linked list event system aborts are not supported (CHEVCTRLn.EVAUXIE = 1 and CHEVCTRLn.EVAUXACT = 11).

Affected Silicon Revisions

SRAM	A0				
128	X				

Linked List Event System Abort Issue (continued)					
SRAM	A0				
256	X				
512	X				

2.3.7. When CRCEN = 1 Output Data is Broken

The CRC in fixed read addressing mode is broken (CHCTRLBn.RAS being either 3, 4, or 5).

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.3.8. Event System and Pattern Match Aborts Fail to Clear Internal Flag

If using pattern match (CHCTRLBn.PATEN = 1) or event system aborts (CHEVCTRLn.EVAUXIE = 1 and CHEVCTRLn.EVAUXACT = 00 or 11), then Channel Event Outputs cannot be used (CHEVCTRLn.EVOE must remain 0).

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.4. MCLK

2.4.1. CLKDIV

PSLVERR is generated when RSVD values are written to the CLKDIV registers.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.5. MCRAMC

2.5.1. RESERVED

2.6. NVMCTRL

2.6.1. RESERVED

2.6.2. RESERVED

2.6.3. PFM

When the Address Wait State Enable bit is set (FCR.CTRLA.ADRWS = 1), AHB peripheral (SQI, HSUSB) access to first 96k of Program Flash Memory (PFM) for each Flash panel is not supported.

Workaround

Ensure that AHB peripherals (if used) do not access first 96k of PFM of each Flash panel. This can be done by reserving first 96k of PFM in the linker file. The following is an example of changes to the linker file that will achieve this:

1. Make the following changes in the linker file.

Default	`#ifndef ROM_ORIGIN`
	`#define ROM_ORIGIN 0xc000000`
	`#endif`
	`#ifndef ROM_LENGTH`
	`#define ROM_LENGTH 0x200000`
	`#elif (ROM_LENGTH > 0x200000)`
	`#error ROM_LENGTH is greater than the max size of 0x200000`
	`#endif`

2 MB Flash Devices	`#ifndef ROM_ORIGIN`
	`#define ROM_ORIGIN 0xc018000`
	`#endif`
	`#ifndef ROM_LENGTH`
	`#define ROM_LENGTH 0x1E8000`
	`#elif (ROM_LENGTH > 0x1E8000)`
	`#error ROM_LENGTH is greater than the max size of 0x1E8000`
	`#endif`

1 MB Flash Devices	`#ifndef ROM_ORIGIN`
	`#define ROM_ORIGIN` **0xc018000**
	`#endif`
	`#ifndef ROM_LENGTH`
	`#define ROM_LENGTH` **0xE8000**
	`#elif (ROM_LENGTH >` **0xE8000**`)`
	`#error ROM_LENGTH is greater than the max size of` **0xE8000**
	`#endif`

512k Flash Devices	`#ifndef ROM_ORIGIN`
	`#define ROM_ORIGIN` **0xc018000**
	`#endif`
	`#ifndef ROM_LENGTH`
	`#define ROM_LENGTH` **0x68000**
	`#elif (ROM_LENGTH >` **0x68000**`)`
	`#error ROM_LENGTH is greater than the max size of` **0x68000**
	`#endif`

2. Add the following code to a 'C' code in the application:

2 MB	`#define PFM2_RESERVED_ADDR` **0x0C100000** `#define PFM2_RESERVED_SIZE 0x18000`
1 MB	`#define PFM2_RESERVED_ADDR` **0x0C080000** `#define PFM2_RESERVED_SIZE 0x18000`
512k	`#define PFM2_RESERVED_ADDR` **0x0C040000** `#define PFM2_RESERVED_SIZE 0x18000`

Then append with the following code:

```
const unsigned char
 __attribute__((section("pfm2_reserved_section"), address(PFM2_RESERVED_ADDR), noload,
space(prog), used,keep))
PFM2_reverved_buffer[PFM2_RESERVED_SIZE];
```

Affected Silicon Revisions

SRAM	A0				
128					
256	X				
512	X				

2.6.4. CRCMLEN

The CRCMLEN active bits can exceed the PFM size for devices with Flash panels smaller than 8M bytes.

Workaround

The value written to CRCMLEN should not exceed the size of the PFM.

Examples: 8M – 0x800000 | 4M – 0x400000 | 2M – 0x200000

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.6.5. CRC

FCR does not check addresses to verify if they fall within a valid Flash memory region.

Workaround

Application code should make certain that configured CRC calculations do not extend beyond the valid PFM address range.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.6.6. ECCCTRL

The ECC mode settings 0x10 (Dynamic Writes with Dynamic Reads but w/o Bus Error) and 0x01 (Dynamic Writes with Dynamic Reads) are not functional for all possible read/write operations.

Workaround

Do not use the ECCCTRL settings 0x10 (Dynamic Writes with Dynamic Reads but w/o Bus Error) and 0x01 (Dynamic Writes with Dynamic Reads).

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.6.7. DBGCTRL.DGBECC

Bus errors reported to debugger when FCR -> DBGCTRL.DBGECC = 0 (NOERR).

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.6.8. Fault Address Capture

When computing CRC on the on-chip Flash and a double ECC error is detected, FFLTCAP.FLTADR does not capture the correct Flash physical address at which a fault occurred.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.7. Position Decoder (PDEC)

2.7.1. Error Flags

An Error Detection (INTFLAG.ERR = 1) updates the STATUS Error flags (HERR, WINERR, MPERR, IDXERR, QERR) with a variable delay.

Workaround

Poll the STATUS Error flags until one of the bits is set.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.7.2. Direction Change

A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay.

Workaround

Do not consider the STATUS.DIR bit status when using the INTFLAG.DIR bit.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.7.3. Hall Mode

A Windows Error (WINERR) flag can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0).

Workaround

Ignore the Windows Error (WINERR) flag in Hall mode after a START command execution, or when leaving standby.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				

Hall Mode (continued)					
SRAM	A0				
512	X				

2.7.4. Hall Mode

In HALL mode, the WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection.

Workaround

Disable the WINERR (INTCLR.WINERR = 1) at first error detection, then re-enable it once the error root cause at the application level is solved.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.7.5. QDEC Mode

With index input enabled, that is EVCTRL.EVEI[2] and operating in X4/X2 mode, angular and revolution counters are incremented/decremented by two separate and unsynchronized sources (Phases and index). This can lead to erroneous generation of MC0 and MC1 events.

Workaround

If the application use case permits, operate PDEC in X4S/X2S mode by setting the CTRLA.CONF[2:0] = 0b001/ 0b011. In this mode, the revolution counter is incremented/decremented by a single source, that is angular counter overflow/underflow.

If the application use case restricts operation in X4/X2 mode, then disable index input event, that is EVCTRL.EVEI[2] = 0. This ensures that revolution counter is incremented/decremented by a single source, that is angular counter overflow/underflow. The first occurrence of the index pulse can be detected using an external interrupt input and the angular counter value can be reset in the corresponding interrupt service routine.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.8. SDHC

2.8.1. SDHC.PSR.CARDINS

The Card Detect Status bit (SDHC.PSR.CARDINS) and downstream interrupt flag bits are updated only after internal clock is enabled (SDHC.CCR.INTCLKEN).

Workaround

The SDHC.CCR.INTCLKEN bit must remain set or be set in order for the Card Detect Status bit (SDHC.PSR.CARDINS) and the Downstream Interrupt Flag bits to function.

Affected Silicon Revisions

SRAM	A0				
128	X				

SDHC.PSR.CARDINS (continued)					
SRAM	A0				
256	X				
512	X				

2.9. SQI

2.9.1. DDR

SQI Dual and Quad mode write modes are inoperable.

Workaround

SQI Single Write mode must be used.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.9.2. DMA

When using a DMA descriptor with the Status Polling Option bit set, the PKTCOMPIF interrupt flag will set before the status check has completed.

Workaround

1. Disable the interrupts for the descriptor that use status check.
2. Add a new descriptor (preferably read) to the list right after the one with the status check bit set.
3. Set the interrupt enable on this descriptor CBD_INT_EN & PKT_INT_EN.
4. The execution of this descriptor will only happen after the previous one is complete (including its corresponding status check).
5. Use the PKTCOMPIF will set after the whole operation has completed.

Note: Ensure to manually clear PKTCOMPIF when starting a DMA operation.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.10. USB

2.10.1. RESERVED

2.10.2. APB

Addressing some PHY registers sets the APB clock request permanently.

Workaround

In the startup code, perform a dummy read to the USB.STATUS register. After accessing a register in the USB, the PHY subspace (starting with PHY00) should always be followed by a dummy read of the USB.STATUS register to clear the APB clock request.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.11. TRAM

2.11.1. DRP

When Data Scrambling is enabled, accessing the RAM during a Data Remanence Prevention (DRP) routine can lead to corrupted (read/write) data.

Workaround

Data Scrambling and DRP should not be used at the same time.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.12. SERCOM

2.12.1. LIN

In SERCOM USART LIN Host mode (CTRLA.FORM = 0x2), in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2), the LIN Host Header delay between the sync and the ID transmission fields is incorrect in the following cases:

- CTRLC.HDRDLY = 0x2: Where the delay between sync and ID transmission fields is 8-bit time instead of 4-bit time.
- CTRLC.HDRDLY = 0x3: Where the delay between sync and ID transmission fields is 14-bit time instead of 4-bit time.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.12.2. LIN - Two Stop Bits

Two stop bits mode (CTRLB.SBMODE = 0x1) is not supported in SERCOM USART LIN Host mode (CTRLA.FORM = 0x2) in the case where break, sync, and identifier fields are automatically transmitted when DATA is written with the identifier (CTRLB.LINCMD = 0x2). Only one stop bit mode is supported.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.12.3. I²C

In I²C host mode, when the FIFO is enabled (CTRLC.FIFOEN = 1), the GCLK clock frequency must be higher or equal than the APB bus clock frequency.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.12.4. SPI/I²C Client Mode

When the GCLK is slowed to less than 10x of the APB clock, SYNCBUSY.ENABLE can get stuck. This is only applicable when the module is configured for I²C or SPI client modes.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.13. FREQM

2.13.1. STATUS.BUSY

If during measurement slot, the measurement clock stalls or is very slow, the STATUS.BUSY will never de-assert and DONE interrupt will not be raised.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.14. OSCCTRL

2.14.1. DFLL48M

When the DFLL48M is used dynamically (enabled and disabled during application run-time, on-demand, or otherwise), tuning can be corrupted when re-enabled.

Workaround

To prevent this issue, it is necessary to use a small step size (recommend DFLLMUL.STEP = 1) and to disable quick lock (DFLLCTRLB.QLDIS = 1) in the case that dynamic operation of the DFLL48M is required.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.15. NMI

2.15.1. GCLK

NMI.GLCK: If the NMI is configured in synchronous edge detection mode (NMICTR.NMISENSE = 1, 2 or 3; NMICTRL.NMIASYNCH = 0), spurious NMI interrupts may occur after a software reset (CTRLA.SWRST = 1).

Workaround

- Configure one dummy EIC External Interrupt x (EXTINTx) in edge detection mode.
- Enable the EIC: CTRLA.ENABLE = 1.
- Wait for synchronization completion (SYNCBUSY.ENABLE = 0).
- Configure the NMI in edge detection mode.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.16. TMR

2.16.1. Periodic Daily Event

Periodic Daily Event has to be generated at time 23:59:59 when CTRLB.CLKREP = 1'b0 in mode 2. But it's getting generated at 23:59:58 when CTRLB.PRESCALER is set to any value other than 4'h1.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.17. (IxS)

2.17.1. Frame Error Detection

If 'hold' timing is violated (which depends on the timing of the connected SPI Host and the user board layout) then frame errors will not be detected. While in Client clock and Client frame mode,

frame errors from the Host will not be detected, but the audio data will be valid regardless of the hold violation. INTFLAG.FRMERR cannot be trusted for this situation.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.17.2. I8S

When operating in I8S left/right justified, client mode, data from the client is not transmitted properly and is erroneous.

Workaround

Use TDM mode rather than I8S mode.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.18. SUPC

2.18.1. ADC VREF

When using ADC in normal mode, Temp Sensor output is offset.

Workaround

ADC calibration values from production should be turned into ADC code, call this Moff. When the user wants to make a temperature measurement, they set en_tsense_mv = 1 (SUPC -> VREGCTRL.TSEN = 1), which will now bring sensor voltage on tsense_ana pin. Use the ADC to measure that voltage. Let's call it Mtsense. Users must also know the value of their external reference by measuring a known internal reference (the 1.2V from bandgap). Using this known value expressed in ADC codes, Moff can be converted in ADC codes and subtracted from the Mtsense to get a corrected value of the temperature sensor.

Affected Silicon Revisions

SRAM	A0				
128					
256	X				
512	X				

2.18.2. OFFSTDBY

Clearing VREGSW.OFFSTDBY[2] will cause PORCORE reset during Standby mode.

Workaround

VREGSW.OFFSTDBY[2] must always be forced to one.

Affected Silicon Revisions

SRAM	A0				
128					
256	X				
512	X				

2.19. EVSYS

2.19.1. BUSYCH

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on falling edges (CHANNELn.EDGESEL = 0x2), the CHSTATUS.CHBUSYn flag will be set but will never come back to 0. It is then impossible to know if the event user for this channel is ready or not to accept new events.

Workaround

Generate software events for this user through a dedicated channel configured with even detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.19.2. OVR

If a software event occurs when the EVSYS is set in synchronous/resynchronized path modes (CHANNELn.PATH = 0x0/0x1) with event detection set on both rising and falling edges (CHANNELn.EDGESEL = 0x3), spurious overrun interrupts may occur (INTFLAG.OVRn).

Workaround

Generate software events for the event user through a dedicated channel configured with even detection set on rising edges (CHANNELn.EDGESEL = 0x1).

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.20. GPIO

2.20.1. VBAT

When voltage on the PB04 pin is close (+/- 6mV) to the VDDIO/AVDD voltage, current Leakage on the PB04 pin can exceed 1uA.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				

VBAT (continued)					
SRAM	A0				
512	X				

2.21. USBHS

2.21.1. USBHS PHY

Toggling on certain PORTD pins can generate noise on the USB.

Workaround

Recommendation to not toggle PD02, PD03, PD04, PD13-16 in I/O mode during USB HS communication.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.22. XOSC

2.22.1. STDBY

When XOSC is in Standby mode, the Charge Pump should be forced on.

Workaround

Force Charge Pump on when XOSC is running in Standby mode.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.23. XOSC32K

2.23.1. Duty Cycle

When VDD is at maximum and the device temperature is greater than or equal to 125°C, the duty cycle drifts to 75%, rendering the peripheral unusable.

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.23.2. CP0

XOSCK32K does not work when Charge Pump is enabled at VDDIO < 2.4V and the device is at hot temperature (125°C).

Workaround

None.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

2.24. ETH

2.24.1. TX CLK

When toggling PC01/PC02, data integrity failure can occur due to the ETH_TX_CLK signal on PC00 being disturbed.

Workaround

When using the Ethernet, the PC01/PC02 slew rate limitation must be enabled at least 8x slower.

Affected Silicon Revisions

SRAM	A0				
128	X				
256	X				
512	X				

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001795**H**), and are showed in **BOLD** type:

Currently, there are no Data Sheet Clarifications to report.

4. Revision History

Revision E - 04/2026

The following updates were performed for this revision:

- Added the following Errata:
  - DMA: 2.3.7 When CRCEN = 1 Output Data is Broken
  - DMA: 2.3.8 Event System and Pattern Match Aborts Fail to Clear Internal Flag

Revision D - 04/2025

The following updates were performed for this revision:

- Updated all Silicon Revision tables throughout the document to reflect differences in SRAM between parts
- Included new Silicon DEVREV tables in the Introduction
- Added the following Silicon Errata Issues:
  - AC: 2.1.2 Analog Mux Short
  - DMA: 2.3.3 Pattern Match
  - DMA: 2.3.4 IP Header Checksum Mode
  - DMA: 2.3.5 Descriptor Loading
  - DMA: 2.3.6 Linked List Event System Abort Issue
  - NVMCTRL: 2.6.9 Fault Address Capture

Revision C - 04/2024

The following updates were performed for this revision:

- Deprecated the following errata due to resolution:
  - AC 2.1.1
  - MCRAMC 2.5.1
  - NVMCTRL 2.6.1
  - NVMCTRL 2.6.2
  - USB 2.10.1
- Added the following new errata:
  - CAN: TX Buffers/TX Queue 2.2.3
  - DMA: BYTORD 2.3.2
  - NVMCTRL: CRCMLEN 2.6.4
  - NVMCTRL: CRC 2.6.6
  - NVMCTRL: ECCCTRL 2.6.7
  - NVMCTRL: DBGCTRL.DBGECC 2.6.8
  - PDEC: QDEC 2.7.5
  - SQI: DMA 2.9.1
  - USB: APB 2.10.2
  - TRAM: DRP 2.11.1
  - SERCOM: LIN 2.12.1
  - SERCOM: LIN - Two Stop Bits 2.12.2
  - SERCOM : I2C 2.12.3

- SERCOM: SPI/I2C Client Mode 2.12.4
- FREQM: STATUS.BUSY 2.13.1
- OSCCTRL: DFLL48M 2.14.1
- NMI: GCLK 2.15.1
- TMR: Periodic Daily Event 2.16.1
- IXS: Frame Detection Error 2.17.1
- IXS: I8S 2.17.2
- SUPC: ADC VREF 2.18.1
- SUPC: OFFSTDBY 2.18.2
- EVSYS: BUSYCH 2.19.1
- EVSYS: OVR 2.19.2
- GPIO: VBAT 2.20.1
- USBHS: USBHS PHY 2.21.1
- XOSC: STDBY 2.22.1
- XOSC32K: Duty Cycle 2.23.1
- XOSC32K: CP0 2.23.2
- ETH: TX CLK 2.24.1

Revision B - 05/2023

The following updates were performed for this revision:

- Updated the Data Sheet Revision version to B throughout the document
- Removed all Confidential markings for public release

Revision A - 12/2022

This is the initial released version of this document.

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