dsPIC33CDVL64MC106

dsPIC33CDVL64MC106 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CDVL64MC106 family devices that you have received conform functionally to the current Device Data Sheet (DS70005441**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CDVL64MC106 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**D2**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool**.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision	
		D1	D2
dsPIC33CDVL64MC106	0x991A	0x0001	0x0002
dsPIC33CDV64MC106	0x991B		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				D1	D2
CPU	`div.sd` Instruction	1.	When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not getting set when an overflow occurs.	X	X
I2C	Interrupt	2.	In Client mode, an incorrect interrupt is generated with DHEN = `1`.	X	X
I2C	Idle	3.	SFRs are reset in Idle mode.	X	X
Oscillator	VCO Dividers	4.	Main and auxiliary PLL external VCO dividers can fail to output the clock signal.	X	X
PWM	Time Base Capture	5.	The PWM Capture Status (CAP) flag will not set again under certain conditions.	X	X
UART	Sleep	6.	When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = `1`.	X	X
UART	IrDA®	7.	IrDA® not functional.	X	X
MOSFET Gate Driver	Sleep Mode	8.	The MOSFET gate driver may not function as expected if Sleep mode is enabled.	X	
MOSFET Gate Driver	XUVLO Fault Detection	9.	After any device Reset, when the High-side driver is enabled for the first time, an erroneous XUVLO FAULT may be triggered.	X	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**D2**).

1. Module: CPU

When using the Signed 32-by-16-Bit Division instruction, `div.sd`, the Overflow bit may not always get set when an overflow occurs. This errata only affects operations in which at least one of the following conditions is true:

- Dividend and divisor differ in sign
- Dividend > 0x3FFFFFFF
- Dividend < 0xC0000000

Work around

The application software must perform both of the following actions to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., the dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient. If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

D1	D2						
X	X						

2. Module: I²C

In Cilent mode with DHEN = `1` (Data Hold Enable), if software sends a NACK, a Client interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Cilent interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

D1	D2						
X	X						

3. Module: I²C

In Client mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL).

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

4. Module: Oscillator

At PLL start-up, the main PLL VCO dividers may occasionally halt and not provide a clock output. The VCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, UART, etc. VCO divider outputs, FVCO/2, FVCO/3, FVCO/4 and FVCODIV, are affected.

Work around

1. Use another clock source, such as the FOSC or PLL Output (FPOLLO), instead of the VCO dividers.
2. If the application requires the VCO divider, test the clock source before using the peripheral in the end application. System resources, including a timer, I/O pin state or interrupts, can be used to detect and verify peripheral activity for a presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, MCLR or POR).

Affected Silicon Revisions

D1	D2						
X	X						

5. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using PWM Generator x interrupt or any of the PWM event interrupts corresponding to the PCI event that triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

D1	D2						
X	X						

6. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

D1	D2						
X	X						

7. Module: UART

The IrDA® module is not functional.

Work around

None.

Affected Silicon Revisions

D1	D2						
X	X						

8. Module: MOSFET Gate Driver

When the MOSFET gate driver HV_{DD} is momentarily sustained at near the POR threshold of 2.7V to 3.2V, followed by device normal operation, and if the MOSFET gate driver entered into Sleep mode, it appears not to wake up from Sleep. The momentarily-sustained HV_{DD} condition could occur with rising or falling HV_{DD}. Only the Sleep mode is affected.

Work around

Use Standby mode of operation for the MOSFET gate driver, if the application desires lower power than the Active mode. Do not use Sleep mode on the MOSFET gate driver.

Affected Silicon Revisions

D1	D2						
X							

9. Module: MOSFET Gate Driver

After any device Reset, when the High-side driver is enabled for the first time, an erroneous XUVLO (External MOSFET Under Voltage Lock Out) FAULT may be triggered. This will disable the HSx outputs. This issue affects only the XUVLO fault on High-side gate drivers.

Work around

Clear the XUVLO upon initiating High-side gate drive sequence using one of the below work around options. After the work around sequence, read the STAT0 and STAT1 registers to ensure the FAULT has been cleared successfully. Once the initial FAULT is cleared, the device will resume normal operation.

Work around #1

1. Monitor $\overline{\text{FAULT}}$ signal until active.
2. Disable Output Enable (OE) pin.
3. Delay up to 400 µS.
4. Enable OE pin.

EXAMPLE 1: WORK AROUND #1 CODE SEQUENCE

```
#define OE   LATCbits.LATC13
#define FAULT PORTDbits.RD1
while(!FAULT){
     OE = 0;                 //disable OE
     __delay_us(400);        //400uS delay to avoid device entering standby mode after OE is put low

     OE = 1;                 //enable OE
        }
```

Work around #2

1. Monitor $\overline{\text{FAULT}}$ signal until active.
2. Disable Output Enable (OE) pin.
3. Send new configuration data to CFG0 via DE2 communication pin.
4. Enable OE pin.

EXAMPLE 2: WORK AROUND #2 CODE SEQUENCE

```
//initialize UART module for DE2 communication. Refer to MOSFET Gate Driver device chapter
describing DE2 communication port
#define OE  LATCbits.LATC13
#define FAULT PORTDbits.RD1

while(!FAULT){
     OE = 0;                          //disable OE
     U1TXREG = 0x81;                  //send first byte,write to CFG0 register of MOSFET gate driver
     while(U1STAHbits.URXBE == 1);    //wait for transmission to complete
     U1TXREG = 0x07;                  //configure MOSFET Gate Driver with XUVLO enabled
     while(U1STAHbits.URXBE == 1);    //wait for transmission to complete
     OE = 1;                          //enable OE
  }
```

Affected Silicon Revisions

D1	D2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005441**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (3/2023)

Initial version of this document; issued for revision D1.

Rev B Document (6/2023)

Added silicon issue 8 (MOSFET Gate Driver).

The I^2C standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

Rev C Document (1/2024)

Added silicon revision D2.

Rev D Document (2/2024)

Added silicon issue 9 (MOSFET Gate Driver).

NOTES:

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