

# PIC16F18056/76 Family Silicon Errata and Data Sheet Clarifications

## PIC16F18056/76



The PIC16F18056/76 devices that you have received conform functionally to the current device data sheet (DS40002325C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18056/76 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1.** Silicon Device Identification

Part Number	Device ID	Revision ID		
		A1	A2	A3
PIC16F18056	0x30FF	0xA001	0xA002	0xA003
PIC16F18076	0x3100	0xA001	0xA002	0xA003

## Silicon Issue Summary

**Table 2.** Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				A1	A2	A3
Charge Pump (CP)	CPON	<a href="#">1.1.1</a>	The CPON Bits Incorrectly Default to OFF Mode	X	X	X
Timer1	Timer1 Gate Source	<a href="#">1.2.1</a>	Changing the Timer1 Gate Source May Cause Unexpected Interrupts	X	X	X
<b>Note:</b> Only those issues indicated in the last column apply to the current silicon revision.						

# 1. Silicon Errata Issues

## NOTICE

This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

## 1.1 Module: Charge Pump (CP)

### 1.1.1 The CPON Bits Incorrectly Default to OFF Mode

The CPON bits incorrectly default to OFF mode (CPON = 00) instead of AUTO mode (CPON = 01) upon power-up or device reset.

#### Work around

User software must configure the charge pump to operate in AUTO mode by writing '01' to the CPON bits of the CPCON register.

#### Affected Silicon Revisions

A1	A2	A3					
X	X	X					

## 1.2 Module: Timer1

### 1.2.1 Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly, and if the TMRxGIE bit is set, an unexpected interrupt will occur.

#### Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

#### Affected Silicon Revisions

A1	A2	A3					
X	X	X					

## 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002325C):

**Note:**

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 2.1 None

There are no known data sheet clarifications as of this publication date.

### 3. Appendix A: Revision History

Doc Rev.	Date	Comments
C	04/2024	Added silicon revision A3; updated data sheet revision letter.
B	12/2023	Added silicon issues 1.1.1 and 1.2.1.
A	04/2022	Initial release of this document.

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