SAMA5D29 Silicon Errata and Data Sheet Clarifications

SAMA5D29

Product Page Links

Scope

The SAMA5D29 devices that you have received conform functionally to the current Device Data Sheet (DS60001764), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in Silicon Issue Summary.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications.

Table 1. SAMA5D29 Silicon Device Identification

Part Number	Silicon Revision	Device Identification
		CHIPID_CIDR[31:0]
ATSAMA5D29-CN	A	0x8A5C08C3
ATSAMA5D29-CNVAO		

Note: Refer to the “Chip Identifier (CHIPID)” and "Product Identification System" sections in the current device data sheet (DS60001764) for detailed information on chip identification and version for your specific device.

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Item/Feature	Summary	Affected Silicon Revisions
			A
FLEXCOM	FLEXCOM SMBUS alert	FLEXCOM SMBUS alert signaling is not functional	X
I^2SC	I^2SC sent data	I^2SC first sent data corrupted	X
MCAN	Debug message handling state machine not reset	Debug message handling state machine not reset to Idle state	X
PMC	PMC_MCKR.PRES field	Change of the field PMC_MCKR.PRES is not allowed if Master/Processor Clock Prescaler frequency is too high	X
PTC	Wrong pull-up value on PD[18:3] during reset	Incorrect pull-up value	X
PWM	Fault Protection to Hi-Z for PWMx output	Fault Protection to Hi-Z for PWMx output is not functional	X
RSTC	RSTC_SR.RSTTYP field	RSTC_SR.RSTTYP does not show GENERAL_RST	X
RTC	RTC_SR.TDERR flag	RTC_SR.TDERR flag is stuck at 0	X
RTC	Truncated read access to RTC_TIMALR (UTC_MODE)	Read access truncated to the first 24 bits for register RTC_TIMALR (UTC_MODE)	X
QSPI	DLYCS delay	QSPI hangs with long DLYCS	X
ROM Code	JTAG_TCK	JTAG_TCK on IOSET 4 pin has a wrong configuration after boot	X
ROM Code	UART connection to SAM-BA Monitor	UART blocks USB connection to SAM-BA Monitor	X
ROM Code	Secure Boot Mode: AES-RSA X.509 Certificate Serial Number Length Limit	The length of serial numbers is limited to 16 bytes by the ROM code	X
SDMMC	Software 'Reset For all' command	Software 'Reset For all' command is not guaranteed	X
SDMMC	Sampling clock tuning procedure	Sampling clock tuning procedure may freeze	X
SDMMC	SDMMC I/O calibration does not work	The impedance calibration mechanism for the SDMMC I/Os does not work	X
SSC	TD output	Unexpected delay on TD output	X
TWIHS	Clear command	The TWI/TWIHS Clear command does not work	X
WDT	Restart command	Restart command of WDT may reset the DDR controller	X

2. Flexible Serial Communication Controller (FLEXCOM)

2.1. FLEXCOM SMBUS alert signalling is not functional

The TWI function embedded in the FLEXCOM does not support SMBUS alert signal management.

Work around

If this signal is mandatory in the application, the user can use one of the standalone TWIs (TWIHS0, TWIHS1) supporting the SMBUS alert signaling.

3. Inter-IC Sound Controller (I^2SC)

3.1. I^2SC first sent data corrupted

Right after I^2SC reset, the first data sent by I^2SC controller on the I2SDO line is corrupted. The following data are not affected.

Work around

None

4. Controller Area Network (MCAN)

4.1. Debug message handling state machine not reset to Idle state when CCCR.INIT is set

Attention: This erratum is applicable for CAN 2.0.

In case MCAN_CCCR.INIT is set by the Host by writing to register MCAN_CCCR or when the CAN enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Setting MCAN_CCCR.CCE does not change MCAN_RXF1S.DMS.

Work around

In case the debug message handling state machine has stopped while MCAN_RXF1S.DMS="01" or MCAN_RXF1S.DMS="10", it can be reset to Idle state by a hardware reset or by reception of debug messages after MCAN_CCCR.INIT is reset to zero.

5. Power Management Controller (PMC)

5.1. Change of the field PMC_MCKR.PRES is not allowed if Master/Processor Clock Prescaler frequency is too high

PMC_MCKR.PRES cannot be changed if the clock applied to the Master/Processor Clock Prescaler (see “Master Clock Controller” in section “Power Management Controller (PMC)” of the SAMA5D2 Series data sheet) is greater than 312 MHz (VDDCORE[1.1, 1.32]) and 394 MHz (VDDCORE[1.2, 1.32]).

Work around

1. Set PMC_MCKR.CSS to MAIN_CLK.
2. Set PMC_MCKR.PRES to the required value.
3. Change PMC_MCKR.CSS to the new clock source (PLLA_CLK, UPLLCK).

6. Peripheral Touch Controller (PTC)

6.1. Wrong pull-up value on PD[18:3] during reset

The PTC ADC includes pull-up resistors (10 kΩ±30%) connected on PD[18:3] which are normally disabled at reset.

Because of an incorrect control of the internal pull-up disable signal, these pull-up resistors are connected temporarily to the pads at reset.

The 10 kΩ pullups are disconnected when the reset phase is completed and the internal resets have been released. The pull-up value is then ~380 kΩ.

Work around

None

7. Pulse Width Modulation Controller (PWM)

7.1. Fault Protection to Hi-Z for PWMx output not functional

While it is possible to force the output of PWMH and PWML to 0 or 1, the feature to set these outputs to Hi-Z by setting the corresponding field in PWM_FPV2 is not functional.

The protection values for PWML and PWMH are by default set to ‘0’.

Work around
None

8. Reset Controller (RSTC)

8.1. RSTC_SR.RSTTYP not showing GENERAL_RST

In the Status register (RSTC_SR), the RSTTYP field shows WKUP_RST instead of GENERAL_RST.

Work around

None

9. Real-Time Clock (RTC)

9.1. RTC_SR.TDERR flag is stuck at 0

The TDERR flag reporting internal free counters errors is stuck at 0. The non-BCD or invalid date/time values are not reported in the RTC Status register (RTC_SR).

Work around

None. A software procedure to check the validity of the RTC time and date values may be implemented.

9.2. Read access truncated to the first 24 bits for register RTC_TIMALR (UTC_MODE)

The register RTC_TIMALR (UTC_MODE) is a 32-bit read/write register but the bits 24:31 are write only.

RTC_TIMALR (UTC_MODE) is functioning properly but any read after write of this register will show the value 0 for the upper byte.

Work around

None.

10. Quad Serial Peripheral Interface (QSPI)

10.1. QSPI hangs with long DLYCS

QSPI hangs if a command is written to any QSPI register during the DLYCS delay. There is no status bit to flag the end of the delay.

Work around

The field DLYCS defines a minimum period for which Chip Select is de-asserted, required by some memories. This delay is generally < 60 ns and comprises internal execution time, arbitration and latencies. Thus, DLYCS must be configured to be slightly higher than the value specified for the slave device. The software must wait for this same period of time plus an additional delay before a command can be written to the QSPI.

11. ROM Code

11.1. JTAG_TCK on IOSET 4 pin has a wrong configuration after boot

The JTAG_TCK signal on IOSET 4 shares its pin (PA22) with the clock signal of the following boot memory interfaces: SDMMC1, SPI1 IOSET 2, QSPI 0 IOSET 3.

If JTAG IOSET 4 is selected by the user as JTAG debug port in the Boot Configuration Word, and if the ROM Code boots, or tries to boot, on any of the external memory interfaces stated above, the JTAG clock pin (TCK) is reset at its default mode (PIO) at the end of the ROM Code execution.

This occurs as soon as EXT_MEM_BOOT_ENABLE is set.

Work around

Do not select or disable external memory boot interface SDMMC1, SPI1 IOSET 2 or QSPI0 IOSET 3. However, if using one of these boot interfaces is required, reconfigure the PA22 pin in JTAG TCK IOSET 4 mode in the bootstrap or application.

11.2. UART blocks USB connection to SAM-BA Monitor

When a UART is used as the ROM Code console interface in the Boot Configuration Word, the USB Device connection may not be properly enabled, and thus the SAM-BA Monitor does not run.

Work around

Pull up the RX line of the UART.

11.3. Secure Boot Mode: AES-RSA X.509 Certificate Serial Number Length Limit

According to the standard RFC 5280 "Internet X.509 Public Key Infrastructure Certificate" section 4.1.2.2, the maximum length for serial numbers in X.509 certificates is 20 bytes.

When parsing the certificate chain in AES-RSA Secure Boot mode, the maximum serial number length allowed by the ROM code is 16 bytes.

Work Around

To use AES-RSA Secure Boot mode, do not use X.509 certificates with a serial number length higher than 16 bytes.

12. Secure Digital MultiMedia Card Controller (SDMMC)

12.1. Software 'Reset For all' command may not execute properly

The software 'Reset For All' command may not execute properly, and, as a result, some registers of the host controller may not reset properly. The setting of the different registers must be checked before reinitializing the SD card.

Work around

None

12.2. Sampling clock tuning procedure

The sampling clock tuning procedure described in the “SD Host Controller Simplified Specification V3.00” may freeze in the latest verification of the “Wait until Buffer Read Ready” condition.

Work around

The condition “Check Execute Tuning = 0“ can be *OR’ed* to “Wait until Buffer Read Ready” condition in the loop issuing the *SEND_TUNING_BLOCK command (CMD19)*.

12.3. SDMMC I/O calibration does not work

The impedance calibration mechanism for the SDMMC I/Os does not work. A fixed calibration code is internally hard-wired and, as a result, the calibration procedure described in the device data sheet, section “ I/O Calibration”, has no effect.

The I/O impedance values are given in the section "Electrical Characteristics" of the data sheet.

With these values and careful PCB design (impedance controlled and matched traces), the SDMMC can be operated in HS200 and in SDR104 modes up to 120 MHz .

Work around

None

13. Synchronous Serial Controller (SSC)

13.1. Unexpected delay on TD output

When SSC is configured with the following conditions:

- RCMR.START = Start on falling edge/Start on Rising edge/Start on any edge,
- RFMR.FSOS = None (input),
- TCMR.START = Receive Start,

an unexpected delay of 2 or 3 system clock cycles is added to the TD output.

Work around

None

14. Two-wire Interface (TWIHS)

14.1. The TWI/TWIHS Clear command does not work

Bus reset using the “CLEAR” bit of the TWI/TWIHS control register does not work correctly during a bus busy state.

Work around

When the TWI master detects the SDA line stuck in low state the procedure to recover is:

1. Reconfigure the SDA/SCL lines as PIO.
2. Try to assert a Logic 1 on the SDA line (PIO output = 1).
3. Read the SDA line state. If the PIO state is a Logic 0, then generate a clock pulse on SCL (1-0-1 transition).
4. Read the SDA line state. If the SDA line = 0, go to Step 3; if SDA = 1, go to Step 5.
5. Generate a STOP condition.
6. Reconfigure SDA/SCL PIOs as peripheral.

15. Watchdog Timer (WDT)

15.1. Restart command of WDT may reset the DDR controller

When using the WDT window with WDD and WDV field of the WDT:

- if 0<WDD<WDV
- and the WDT is restarted in the permitted window 0<wdt counter<WDD

then the WDT is restarted but a reset signal is sent to the fuse controller and the DDR controller, leading to DDR memory access and/or fuse access issues.

Work around

None. Do not use the window mode of the WDT.

16. Data Sheet Clarifications

There are no known data sheet clarifications as of this publication date.

17. Revision History

17.1. Rev. C - 10/2025

Added in Reset Controller (RSTC): - RSTC_SR.RSTTYP not showing GENERAL_RST

17.2. Rev. B - 08/2022

Updated Silicon Issue Summary. Added in Secure Digital MultiMedia Card Controller (SDMMC): - SDMMC I/O calibration does not work Deleted errata: - Fuse matrix programming requires a main clock (MAINCK) frequency between 10 and 15 MHz - Fuse matrix read requires a main clock (MAINCK) frequency below 28 MHz

17.3. Rev. A - 03/2022

First issue.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-2224-3

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Product Page Links

ATSAMA5D29