PIC16F18054/55/74/75 Family Silicon Errata and Data Sheet Clarifications

PIC16F18054/55/74/75

Introduction

The PIC16F18054/55/74/75 devices that you have received conform functionally to the current device data sheet (DS40002338**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18054/55/74/75 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID		
		A0	A1	A2
PIC16F18054	0x30FB	0x2000	0x2001	0x2002
PIC16F18055	0x30FC	0x2000	0x2001	0x2002
PIC16F18074	0x30FD	0x2000	0x2001	0x2002
PIC16F18075	0x30FE	0x2000	0x2001	0x2002

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				A0	A1	A2
Configuration Words (CONFIG)	Sleep	1.1.1	Waking from Sleep may cause unexpected behavior.	X		
Charge Pump (CP)	CPON	1.2.1	The CPON Bits Incorrectly Default to OFF Mode.	X	X	X
Timer1	Timer1 Gate Source	1.3.1	Changing the Timer1 Gate Source May Cause Unexpected Interrupts.	X	X	X
Note: Only those issues indicated in the last column apply to the current silicon revision.						

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Configuration Words (CONFIG)

1.1.1 Waking from Sleep May Cause Unexpected Behavior

Waking from Sleep may cause unexpected behavior.

Work around

Do not use the `SLEEP` instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

Affected Silicon Revisions

A0	A1	**A2**					
X							

1.2 Module: Charge Pump (CP)

1.2.1 The CPON Bits Incorrectly Default to OFF Mode

The CPON bits incorrectly default to OFF mode (CPON = `00`) instead of AUTO mode (CPON = `01`) upon power-up or device reset.

Work around

User software must configure the charge pump to operate in AUTO mode by writing '`01`' to the CPON bits of the CPCON register.

Affected Silicon Revisions

A0	A1	**A2**					
X	X	**X**					

1.3 Module: Timer1

1.3.1 Changing the Timer1 Gate Source May Cause Unexpected Interrupts

When a new value is written into the Timer1 Gate Source Select (GSS) bits of the TxGATE register, the TMRxGIF interrupt flag may be set unexpectedly, and if the TMRxGIE bit is set, an unexpected interrupt will occur.

Work around

User software must clear the TMRxGIF bit immediately after writing the new value to the GSS bits.

Affected Silicon Revisions

A0	A1	**A2**					
X	X	**X**					

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002338**C**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 TMR0

A note box has been added to the section **"Timer0 Output"**. The entire section now reads as follows:

TMR0_out toggles on every match between TMR0L and TMR0H in 8-bit mode or when TMR0H:TMR0L rolls over in 16-bit mode. If the output postscaler is used, the output is scaled by the ratio selected. The Timer0 output can be routed to an I/O pin via the RxyPPS output selection register or internally to a number of Core Independent Peripherals. The Timer0 output can be monitored through software via the OUT output bit.

Important: In 8-bit mode, when PR0 = 0 (either loaded with 0 or resets to 0), the TMR0 output remains high, and no interrupts are generated.

2.2 Electrical Specifications Parameter AD05

The Analog-to-Digital Converter (ADC) Electrical Specification parameter AD05 has been updated as shown below (changes from the data sheet in **bold**):

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C, T_{AD} = 500 ns							
Param. No.	Sym.	Characteristic	Min.	Typ. †	Max.	Units	Conditions
AD05	E_{GN}	Gain Error	—	—	**2.5**	LSb	$ADC_{REF}+$ = 3.0V, $ADC_{REF}-$ = 0V

2.3 CPCON Charge Pump Threshold (CPT) Bit

In the CPCON register, the description of the Charge Pump Threshold (CPT) bit (CPCON[1]) is the opposite of its actual behavior. The correct description of the bit's operation is shown below (changes from the data sheet in **bold**).

Value	Description
1	V_{DD} is **below** the charge pump auto-enable threshold (V_{AUTO})
0	V_{DD} is **above** the charge pump auto-enable threshold (V_{AUTO})

3. Appendix A: Revision History

Doc Rev.	Date	Comments
E	07/2024	Added silicon revision A2; added Data Sheet Clarifications 2.1, 2.2, and 2.3; corrected the REVID values.
D	04/2024	Updated data sheet revision letter to C; added silicon issues 1.2.1 and 1.3.1.
C	10/2022	Added silicon issue 1.1.1.
B	06/2022	Added silicon revision A1.
A	03/2022	Initial release of this document.

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ISBN: 978-1-6683-4945-8

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