dsPIC33CK256MC506

dsPIC33CK256MC506 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK256MC506 family devices that you have received conform functionally to the current Device Data Sheet (70005473**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK256MC506 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision	Part Number	Device ID(1)	Revision ID for Silicon Revision
		A0			A0
dsPIC33CK128MC502	0xA240	0x0000	dsPIC33CK128MC102	0xA200	0x0000
dsPIC33CK128MC503	0xA241		dsPIC33CK128MC103	0xA201	
dsPIC33CK128MC505	0xA242		dsPIC33CK128MC105	0xA202	
dsPIC33CK128MC506	0xA243		dsPIC33CK128MC106	0xA203	
dsPIC33CK256MC502	0xA250		dsPIC33CK256MC102	0xA210	
dsPIC33CK256MC503	0xA251		dsPIC33CK256MC103	0xA211	
dsPIC33CK256MC505	0xA252		dsPIC33CK256MC105	0xA212	
dsPIC33CK256MC506	0xA253		dsPIC33CK256MC106	0xA213	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A0
ADC	Differential-mode	1.	Errors may occur when enabling Differential-mode when FSRC > 50 MHz.	X
CCP	CCP	2.	Timer interrupt not working in Capture mode.	X
CPU	`DIV.SD` Instruction	3.	Overflow bit is not getting set when an overflow occurs.	X
I2C	Idle	4.	Address cannot be received in Idle mode.	X
PWM	Time Base Capture	5.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X
Reset	BOR	6.	BOR may stop functioning when V_{DD} drops within the window between the BOR level and BOR-25 mV.	X
Reset	BOR	7.	BOR may periodically cause device resets when V_{DD} is in a window between the BOR level and BOR-25 mV.	X
Oscillator	POSC	8.	POSCRDY sets early on clock switch to POSC.	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: ADC

When using the ADC in Differential-mode (DIFFx = 1) with an input frequency (FSRC) above 50 MHz, the first result data may be incorrect. The Single-Ended Channel mode is unaffected by this errata.

Work around

Use a slower input frequency of 50 MHz or less during ADC initialization to write to ADMODxL/H registers. After completion of the first data conversion for each channel in Differential-mode, the input frequency (FSRC) can be increased to the maximum specified frequency in the **"Electrical Characteristics"** section of the device data sheet.

Affected Silicon Revisions

A0							
X							

2. Module: CCP

The CCP Timer Interrupt, _CCTxInterrupt, may not occur in Capture mode (CCSEL = 1) when the timer time base prescale is set to anything other than zero (TMRPS[1:0] ≠ 0).

Work around

None.

Affected Silicon Revisions

A0							
X							

3. Module: CPU

When using the signed 32/16-bit division instruction, DIV.SD, the Overflow bit may not always be set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the DIV.SD instruction.

Affected Silicon Revisions

A0							
X							

4. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set to discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0							
X							

5. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status flag, CAP, will not be set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid this condition. The timing of the PGxCAP read operation can be scheduled by using the PWM Generator x (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event that triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

A0							
X							

6. Module: Reset

BOR may stop functioning when VDD drops within the window between the BOR level and BOR-25 mV.

Work around

After start-up, if VDD decreases to a value between VBOR-25 mV and VBOR, the BOR may be unintentionally disabled. The device may incorrectly operate down to 2.0V. However, while operating at a VDD between 3-3.6V, the device will operate as expected. The VBOR specification is listed in the **"Electrical Characteristics"** section of the device data sheet.

Affected Silicon Revisions

A0							
X							

7. Module: Reset

BOR may periodically cause device resets when VDD is in a window between the BOR level and BOR-25 mV.

Work around

If VDD is between VBOR-25 mV and VBOR, a BOR reset may repeatedly occur. However, while operating at a VDD between 3-3.6V, the device will operate as expected. The VBOR specification is listed in the **"Electrical Characteristics"** section of the device data sheet.

Affected Silicon Revisions

A0							
X							

8. Module: Oscillator

POSCRDY sets early on clock switch to POSC.

Work around

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005473**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2021)

Initial version of this document; issued for revision A0.

Rev B Document (1/2022)

Updates data sheet revision from Rev. B to Rev. C.

Rev C Document (10/2025)

Adds silicon issues 6 (Reset), 7 (Reset), and 8 (Oscillator).

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