Silicon Errata and Data Sheet Clarifications

AVR32DB28/32/48

The AVR32DB28/32/48 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002301), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR32DB28/32/48 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002301) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A1(1)	Rev. B0
Device	2.2.1. Increased Current Consumption May Occur When VDD Drops	X	-
	2.2.2. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X
CLKCTRL	2.3.1. The PLL Will Not Run when Using XOSCHF with an External Crystal	X	-
DAC	2.4.1. DAC Output Buffer Lifetime Drift	X	-
NVMCTRL	2.5.1. Flash Multi-Page Erase Can Erase Write Protected Section	X	X
	2.5.2. NVM_EEPROM_ERASE Command does Not Respect Write Protect	X	X
TCA	2.6.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	-
TCB	2.7.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	-
TCD	2.8.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	-
	2.8.2. CMPAEN Controls All WOx for Alternative Pin Functions	X	-
	2.8.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X
TWI	2.9.1. Flush Non-Functional	X	X
USART	2.10.1. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	-
	2.10.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Increased Current Consumption May Occur When V_{DD} Drops

The device may experience increased current consumption of approximately 1.5 mA if V_{DD} drops below 2.1V and is held in the range of 1.9-2.1V. This will only occur if V_{DD} is originally at a higher level and then drops down to the mentioned voltage range.

Work Around

Ensure V_{DD} is always kept above 2.1V by setting the BOR trigger level to 2.2V to keep the device from executing if V_{DD} drops towards the affected voltage range. If operation in voltage range 1.9-2.1V is required, make sure V_{DD} does not rise above 2.1V and then drops down again. Note that the voltage levels given are not absolute values but typical values.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.2.2 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

2.3 CLKCTRL - Clock Controller

2.3.1 The PLL Will Not Run when Using XOSCHF with an External Crystal

When the PLL is configured to run from an external source (SOURCE in CLKCTRL.PLLCTRLA is '1'), the PLL will only run if XOSCHF is configured to use an external clock (SELHF in CLKCTRL.XOSCHFCTRLA is '1'). It will not work with an external crystal.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.4 DAC - Digital-to-Analog Converter

2.4.1 DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over the device's lifetime if powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

2.5.2 NVM_EEPROM_ERASE Command does Not Respect Write Protect

The NVM_EEPROM_ERASE command does not respect the EEPROM Write Protected (EEWP) bit in the Control B (NVMCTRL.CTRLB) register. Content will be erased even though it should not.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

2.6 TCA - 16-Bit Timer/Counter Type A

2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.7 TCB - 16-Bit Timer/Counter Type B

2.7.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.8 TCD - 12-Bit Timer/Counter Type D

2.8.1 Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.8.2 CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around

None.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.8.3 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

2.9 TWI - Two-Wire Interface

2.9.1 Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in the Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around

Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. An ordinary operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	-

2.10.2 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A1	Rev. B0
X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002301).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Device

3.1.1 Features

A clarification has been made to change the Flash endurance specification in the *Memories* bullet point in the *Features* list.

- Memories
  - 32 KB in-system self-programmable Flash memory
  - 512B EEPROM
  - 4 KB SRAM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash: **1,000** cycles
    - EEPROM: 100,000 cycles
  - Data retention: 40 years at 55°C

3.1.2 FUSE - Configuration and User Fuses - SYSCFG0

A clarification of the EEPROM Save During Chip Erase (EESAVE) fuse description in the System Configuration 0 (SYSCFG0, section 8.8.2.4) fuse has been made.

Bit 0 - EESAVE EEPROM Saved During Chip Erase

This bit controls if the EEPROM will be erased or saved during a chip erase.

Value	Name	Description
0	DISABLE	EEPROM is erased during a chip erase
1	ENABLE	EEPROM is saved during a chip erase **regardless of whether the device is locked or not**

3.2 SPI - Serial Peripheral Interface

3.2.1 SPI - Serial Peripheral Interface

A clarification has been made to the *Operation - Client Mode* section. The last sentence is removed.

28.3.2.2 Client Mode

In Client mode, the SPI peripheral receives the SPI clock and Client Select from a Host. Client mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Client mode, the control logic will sample the incoming signal on the SCK pin.

3.2.2 SPI - Serial Peripheral Interface

A clarification has been made to the *Operation - Client Mode - Buffer Mode* section.

28.3.2.2.2 Buffer Mode

To avoid data collisions, the SPI peripheral can be configured in Buffered mode by writing a '1' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register.

In this mode, the SPI has additional interrupt flags and extra buffers. The extra buffers are shown in Figure 28-1. There are two different modes for the Buffer mode, selected with the Buffer mode Wait for Receive (BUFWR) bit. The two different modes are described below with timing diagrams.

Note: When operating as a client in Buffered mode and the SPI clock is close to maximum frequency, the client may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

3.3 AC - Analog Comparator

3.3.1 Analog Comparator Interrupt Control

A clarification of the Interrupt Mode (INTMODE) bit field of the AC Interrupt Control (ACn.INTCTRL, section 32.5.5) register has been made.

Table 32-4. Interrupt Generation with Single Comparator

Value	Name	Description
0x0	BOTHEDGE	Positive and negative inputs crosses
0x1	-	Reserved
0x2	NEGEDGE	Positive input goes **below** negative input
0x3	POSEDGE	Positive input goes **above** negative input

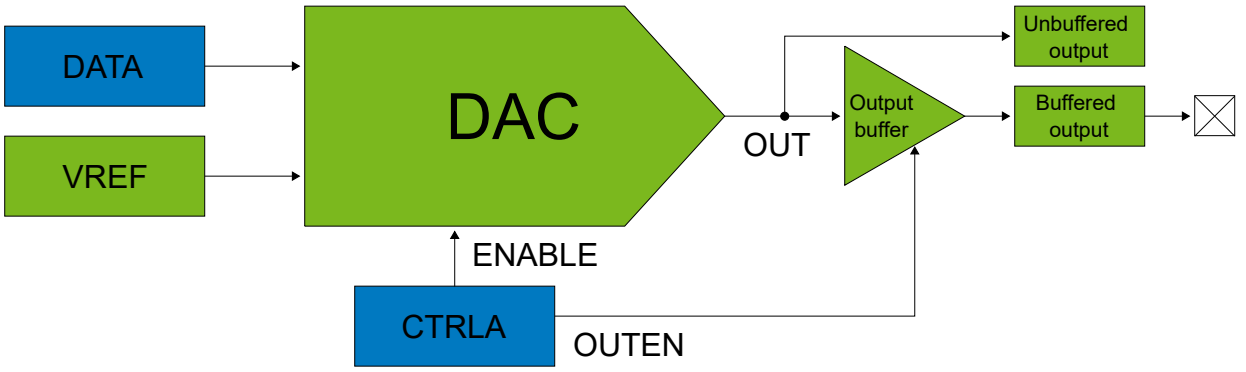
3.4 DAC - Digital to Analog Converter

3.4.1 DAC Output

Clarifications of the block diagram and the DAC Output sub-section of the DAC peripheral has been made:

1. The block diagram is updated with clarifications to the output signal routing (buffered/ unbuffered) and will replace the original block diagram.
2. Sections 34.3.2.3 (DAC as Source For Internal Peripherals) and 34.3.2.4 (DAC Output on Pin) are replaced by section 34.3.2.3 DAC Output.

Figure 34-1. DAC Block Diagram



34.3.2.3 DAC Output

The DAC can be used as an output to a pin and as an input to the peripherals in the table below.

DAC Output	Peripheral Input	Notes
Unbuffered	• **Analog Comparator (AC)** • **Analog to Digital Converter (ADC)**	**The peripheral is connected to the unbuffered DAC output. See section 34.3.2.3.1. Unbuffered Output as Source For Internal Peripherals.**
Buffered	• **Analog Signal Conditioning (OPAMP)**	**The peripheral is connected to the DAC Output pin. See section 34.3.2.3.2. Buffered Output.**

34.3.2.3.1 Unbuffered Output as Source For Internal Peripherals

The unbuffered analog output of the DAC can be internally connected to other peripherals when the ENABLE bit in the Control A (DACn.CTRLA) register is written to '1'. When only the DAC unbuffered analog output is used, the Output Buffer Enable (OUTEN) bit in DACn.CTRLA can be '0', freeing the pin to be used by other peripherals.

34.3.2.3.2 Buffered Output

The buffered analog output of the DAC can be enabled by writing a '1' to the Output Buffer Enable (OUTEN) bit in the Control A (DACn.CTRLA) register. The pin used by the DAC must have the input disabled from the Port peripheral. Refer to the *Electrical Characteristics* section for information about the drive capabilities of the DAC output buffer.

3.5 Electrical Characteristics

3.5.1 I/O Pin Characteristics

Some clarifications have been made to the *I/O Pin Characteristics* table. Note that one footnote has been deleted.

Table 39-7. I/O Pin Characteristics(1)

Symbol	Description	Min.	Typ. †	Max.	Units	Conditions
Input Low Voltage						
V_{IL}	I/O PORT:					
	• With Schmitt Trigger buffer	—	—	$0.2\times V_{DD}$	V	
	• With I^2C levels	—	—	$0.3\times V_{DD}$	V	
	• With SMBus 3.0 levels	—	—	0.8	V	
	$\overline{\text{RESET}}$ Pin	—	—	$0.2\times V_{DD}$	V	
	TTL level	—	—	0.8	V	
Input High Voltage						
V_{IH}	I/O PORT:					
	• With Schmitt Trigger buffer	$0.8\times V_{DD}$	—	—	V	
	• With I^2C levels	$0.7\times V_{DD}$	—	—	V	
	• With SMBus 3.0 levels	1.35	—	—	V	
	$\overline{\text{RESET}}$ Pin	$0.8\times V_{DD}$	—	—	V	
	TTL level	1.6	—	—	V	
Input Leakage Current(2)						

.....continued						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
I_{IL}	I/O PORTS[3]	—	<5	—	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A = 85°C
		—	<5	—	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A = 125°C
	$\overline{\text{RESET}}$ Pin[4]	—	±50	—	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A = 85°C
Pull-up Current						
I_{PUR}		—	140	—	µA	V_{DD} = 3.0V, V_{PIN} = GND
Output Low Voltage						
V_{OL}	Standard I/O Ports	—	—	0.6	V	I_{OL} = 10 mA, V_{DD} = 3.0V
Output High Voltage						
V_{OH}	Standard I/O Ports	V_{DD}-0.7	—	—	V	I_{OH} = 6 mA, V_{DD} = 3.0V
I/O Slew Rate						
t_{SR}	**Rising slew rate**	**—**	**22**	**—**	**ns**	**PORTCTRL.SRL = 0x00**
	Rising slew rate	**—**	**45**	**—**	**ns**	**PORTCTRL.SRL = 0x01**
	Falling slew rate	**—**	**30**	**—**	**ns**	**PORTCTRL.SRL = 0x01**
	Falling slew rate	**—**	**16**	**—**	**ns**	**PORTCTRL.SRL = 0x00**
Pin Capacitance						
C_{IO}	OPAMP output	—	9	—	pF	
	V_{REF}pin	—	7	—	pF	
	XTAL pins	—	4	—	pF	
	Other pins	—	4	—	pF	

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:

1. These figures are valid for all I/O ports regardless of if they are connected to the V_{DD} or V_{DDIO2} power domain.
2. The negative current is defined as the current sourced by the pin.
3. The leakage current numbers for I/O PORTS are valid also when the pin is used as an input to an enabled analog peripheral.
4. The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. A higher leakage current may be measured at different input voltages.

3.5.2 Electrical Characteristics - Memory Programming Specifications

A clarification has been made to change the Flash memory cell endurance specification in the *Memory Programming Specifications* table.

Table 39-8. Memory Programming Specifications

Symbol	Description	Min.	Typ	Max.	Units	Conditions
Data EEPROM Memory Specifications						
E_D	Data EEPROM byte endurance	100k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_RET}	Characteristic retention	—	40	—	Year	Provided no other specifications are violated
N_{D_REF}	Total Erase/Write cycles before refresh	1M	4M	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{D_CE}	Full EEPROM Erase	—	10	—	ms	

.....continued						
Symbol	Description	Min.	Typ	Max.	Units	Conditions
V_{D_RW}	V_{DD} for Read or Erase/ Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
t_{D_BEW}	Byte Erase and Write cycle time	—	11	—	ms	
Program Flash Memory Specifications						
E_P	**Flash memory cell endurance**	**1k**	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +85°C
t_{P_RET}	Characteristic retention	—	40	—	Year	Provided no other specifications are violated
V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
V_{P_REW}	V_{DD} for Erase/Write operation	V_{DD} (2)	—	V_{DDMAX}	V	
t_{P_PE}	Page Erase	—	10	—	ms	
t_{P_CE}	Chip Erase	—	—	—	ms	
t_{P_WRD}	Byte/Word Write	—	70	—	µs	

Notes:

1. These parameters are not tested but ensured by design.
2. During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. If the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0, the erase attempt will fail.

3.5.3 Electrical Characteristics - SPI

Some clarifications have been made to the *Timing Specifications in Host Mode* and *Timing Specifications in Client Mode* tables. Note that some rows have been deleted.

Table 39-20. SPI - Timing Specifications in Host Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SCK} *	SCK clock frequency	—	—	**$f_{CLK\_PER}/2$**	MHz	
T_{SCK} *	SCK period	**2 × T_{CLK_PER}**	—	—	ns	
t_{SCKW}	SCK high/low width	—	0.5 × T_{SCK}	—	ns	
t_{MIS}	MISO setup to SCK	—	**T_{CLK_PER}**	—	ns	
t_{MIH}	MISO hold after SCK	—	**0**	—	ns	
t_{MOS}	MOSI setup to SCK	—	0.5 × T_{SCK}	—	ns	
t_{MOH}	MOSI hold after SCK	—	**0.5 × T_{SCK}**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Table 39-21. SPI - Timing Specifications in Client Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SSCK} *	Client SCK clock frequency	—	—	**$f_{CLK\_PER}/6$**	MHz	
T_{SSCK} *	Client SCK period	**6 × T_{CLK_PER}**	—	—	ns	
t_{SSCKW} *	SCK high/low width	**3 × T_{CLK_PER}**	—	—	ns	
t_{SIS} *	MOSI setup to SCK	**0**	—	—	ns	
t_{SIH} *	MOSI hold after SCK	**3 × T_{CLK_PER}**	—	—	ns	
t_{SSS} *	SS setup to SCK	**T_{CLK_PER}**	—	—	ns	
t_{SSH} *	SS hold after SCK	**T_{CLK_PER}**	—	—	ns	

.....continued						
Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
t_{SOS}	**MISO valid after SCK**	—	**t_{SR}**	—	ns	**$f_{SSCK} \geq f_{CLK\_PER}/6$**
			—			**$f_{SSCK} < f_{CLK\_PER}/6$**
t_{SOSS}	MISO setup after SS low	—	**t_{SR}**	—	ns	
t_{SOSH}	MISO hold after SS low	—	**t_{SR}**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
C	02/2024	• Document: General editorial updates • Added Silicon Revision: B0 – NVMCTRL: 2.5.1. Flash Multi-Page Erase Can Erase Write Protected Section – TCD: 2.8.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used – TWI: 2.9.1. Flush Non-Functional • Added Errata: – Device: 2.2.2. Write Operation Lost if Consecutive Writes to Specific Address Spaces – NVMCTRL: 2.5.2. NVM_EEPROM_ERASE Command does Not Respect Write Protect – USART: 2.10.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Added Data Sheet Clarifications: – Device: • 3.1.1. Features • 3.1.2. FUSE - Configuration and User Fuses - SYSCFG0 – SPI: • 3.2.1. SPI - Serial Peripheral Interface • 3.2.2. SPI - Serial Peripheral Interface – AC: 3.3.1. Analog Comparator Interrupt Control – DAC: 3.4.1. DAC Output – Electrical Characteristics: • 3.5.1. I/O Pin Characteristics • 3.5.2. Electrical Characteristics - Memory Programming Specifications • 3.5.3. Electrical Characteristics - SPI
B	03/2022	• Document: General editorial updates. • Added Errata: – DAC: 2.4.1. DAC Output Buffer Lifetime Drift – NVMCTRL: 2.5.1. Flash Multi-Page Erase Can Erase Write Protected Section – TCD: 2.8.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used – TWI: 2.9.1. Flush Non-Functional • Added data sheet clarifications: – Device: • Features • FUSE - Configuration and User Fuses - SYSCFG0 – AC: Analog Comparator Interrupt Control – DAC: DAC Output – Electrical Characteristics: Memory Programming Specifications
A	02/2021	Initial document release

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