PIC18F27/47/57Q83 Silicon Errata and Data Sheet Clarifications

PIC18F27/47/57Q83

The PIC18F27/47/57Q83 devices that you have received conform functionally to the current device data sheet (DS40002265**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q83 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID			
		B3	B4	B5	C0
PIC18F27Q83	0x9909	0xA043	0xA044	0xA045	0xA080
PIC18F47Q83	0x990A	0xA043	0xA044	0xA045	0xA080
PIC18F57Q83	0x990B	0xA043	0xA044	0xA045	0xA080

Important: Refer to the **Device/Revision ID** section in the current **"PIC18-Q83/84 Family Programming Specification"** (DS40002137) for more detailed information on Device Identification and Revision IDs for a specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B3	B4	B5	C0
UTMR	Hardware Reset condition	1.1.1	Reset does not happen at period match when the prescaler > 0	X			
	Level-triggered ERS Start/Reset condition	1.1.2	Dead zone exists in level-triggered Start/Reset condition when an ERS signal is generated due to an SFR access	X	X	X	X
	Hardware Reset condition	1.1.3	Reset does not happen at period match when the prescaler > 0 and the timer stops at period match (includes One Shot mode)	X	X	X	X
	Pulse output	1.1.4	Pulse output does not occur at period match when the prescaler = 1		X	X	X
	Clear Command	1.1.5	Clear Command may not work properly	X	X	X	X
I^2C	Start and Stop Interrupt Function	1.2.1	The I^2C Start and/or Stop flags may be set when I^2C is enabled	X	X	X	X
SMT	Reset Bit	1.3.1	SMT Stops working if RST is set while prescaler setting is not zero	X	X	X	X
ADCC with Context	Double Sample Conversions	1.4.1	An unexpected acquisition time is added between the first and second conversion	X	X	X	X
PIC18 Core	FSR Shadow Registers	1.5.1	FSR shadow registers are not writable	X	X	X	X
UART	Stop bit	1.6.1	TXDE signal may go low before the STOP bit has been entirely transmitted	X	X	X	X
ICD	Single-Step Function (SSTEP)	1.7.1	Single Step function does not execute at Software Breakpoint	X	X	X	X
PWM	PWM Mode	1.8.1	Wrong Duty Cycle for CCP Module	X	X	X	X
ICSP™	Low-Voltage Programming (LVP)	1.9.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X	X
CAN	Masks/Filters	1.10.1	Filters 8-11 will erroneously accept incoming messages with SID of 0x000	X	X	X	

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Reset Does Not Happen at Period Match When the Prescaler > 0

When the prescaler > 0 and a hardware-based Reset event is selected (RESET = 'b01 or 'b10 or 'b11), the timer does not reset at period match.

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

B3	B4	B5	C0
X			

1.1.2 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = 'b11 or RESET = 'b01) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.1.3 Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the timer is configured to reset at a hardware-based event (RESET = 'b01 or 'b10 or 'b11) and stop at period match (STOP = `b11), the timer stops at period match but does not reset (no pulse output occurs and ZIF interrupt is not generated).

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.1.4 Pulse Output Does Not Occur at Period Match When the Prescaler = 1

The timer output pulse will not occur at period match when prescaler = 1.

Work around

Use prescaler = 0 or prescaler > 1 when a pulse output is desired.

Affected Silicon Revisions

B3	B4	B5	C0
	X	X	X

1.1.5 Clear Command May Not Work Properly in Asynchronous Mode

When operating in asynchronous mode (CSYNC = 0), setting the Clear Command bit (CLR= 1) may not clear the Timer Counter register value.

Work around

Use the Universal Timer module in synchronous mode (CSYNC = 1) when Clear Command bit (CLR) is being used.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.2 Module: Inter-Integrated Circuit (I^2C)

1.2.1 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.3 Module: Signal Measurement Timer (SMT)

1.3.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on or by performing a device reset.

Work around

Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. Either disable the module or the clock before using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.4 Module: Analog-to-Digital Converter with Computation and Context Switching (ADC)

1.4.1 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.5 Module: PIC18 Core

1.5.1 FSR Shadow Registers Are Not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below).
3. Write the shadow FSRxL (data doesn't matter); this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0]).
5. Write FSRxH.
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.6 Module: Universal Asynchronous Receiver Transmitter (UART)

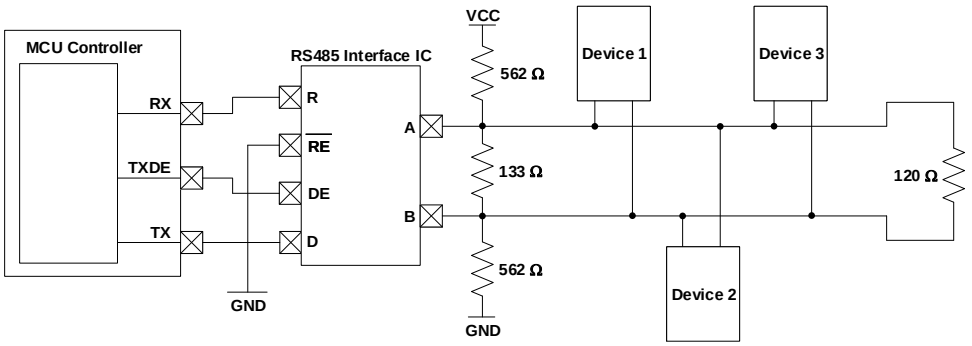
1.6.1 UART TXDE Signal May Go Low before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below shows an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.7 Module: In-Circuit Debug

1.7.1 Single Step Function Does Not Execute at SW Breakpoint

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

Work around

None.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.8 Module: Pulse-Width Modulation (PWM)

1.8.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around

None.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	X

1.9 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.9.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

B3	B4	B5	C0

X	X	X	X

1.10 Module: Controller Area Network (CAN) Module

1.10.1 Filters 8-11 Will Erroneously Accept Incoming Messages With SID of 0x000

When using the CAN RX filters 8-11, any messages where the incoming message after masking is SID 0x000 will trigger a filter match, regardless of the filter ID settings. For example: an incoming message with ID of 0x350 and a mask setting of 0x00F will trigger a filter match regardless of other mask/filter settings. This will occur even if the filter is set to only accept extended IDs.

Work around

If using CAN RX filters 8-11, check the FILHIT bits of C1VECH (or the received message object) upon message reception. If the value of FILHIT is greater than 11, then this error has occurred and the message can be ignored and discarded.

Affected Silicon Revisions

B3	B4	B5	C0
X	X	X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002265**C**):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
F	04/2024	Added silicon revision C0.
E	12/2023	Added silicon erratum 1.1.5 to UTMR module as well as new errata 1.2.1-1.10.1. Added new errata entry to UTMR module.
D	07/2022	Added Data Sheet Clarification 2.1.
C	03/2021	Adding silicon erratum item 1.1.4.
B	01/2021	Adding silicon erratum item 1.1.3.
A	11/2020	Initial document release.

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