Silicon Errata and Data Sheet Clarifications

AVR128DB28/32/48/64

Product Page Links

Introduction

The AVR128DB28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002247), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DB28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002247) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

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1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A4[1]	Rev. A5	Rev. B0
Device	Some Reserved Fuse Bits Are '1'	X	-	-
	Increased Current Consumption May Occur When VDD Drops	X	X	-
	CRC Check During Reset Initialization Is not Functional	X	-	-
	Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X	X
ADC	Increased Offset in Single-Ended Mode	X	-	-
	ADC MUX Selection and Accumulation Number has Delayed Update When Initialization Delay is Used	X	X	X
CCL	The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X	-
	The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices	X	-	-
CLKCTRL	External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready	X	-	-
	RUNSTDBY is Not Functional When Using External Clock Sources	X	-	-
	PLL Status not Working as Expected	X	X	-
	The PLL Will Not Run when Using XOSCHF with an External Crystal	X	X	-
DAC	DAC Output Buffer Lifetime Drift	X	X	-
NVMCTRL	Flash Multi-Page Erase Can Erase Write Protected Section	X	X	-
	NVM_EEPROM_ERASE Command does Not Respect Write Protect	X	X	X
OPAMP	OPAMP Consume More Power Than Expected	X	-	-
	The Input Range Select is Read-Only	X	-	-
PORT	PD0 Input Buffer is Floating	X	X	X
RSTCTRL	BOD Registers not Reset When UPDI Is Enabled	X	-	-
SPI	Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices	X	X	-
TCA	Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X	-
TCB	CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X	-
	TCB4 Waveform Output Alternative 1 Non-Functional	X	X	X
TCD	Asynchronous Input Events not Working When TCD Counter Prescaler Is Used	X	X	-
	CMPAEN Controls All WOx for Alternative Pin Functions	X	X	-
	Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used	X	X	X
TWI	The Output Pin Override Does not Function as Expected	X	X	-
	Flush Non-Functional	X	X	X
USART	Open-Drain Mode Does not Work When TXD Is Configured as Output	X	X	-
	Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X	X	-
	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X	X
ZCD	All ZCD Output Selection Bits Are Tied to the ZCD0 Bit	X	-	-

Note:

1. This revision is the initial release of the silicon.

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2. Silicon Errata Issues

2.1. Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2. Device

2.2.1. Some Reserved Fuse Bits Are '1'

For material with date code 2021 (manufactured in the year 2020, week 21) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (Device will use the OSCHF clock source)
- SYSCFG0 = `0xF6`
- SYSCFG1 = `0xE8`

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.2.2. Increased Current Consumption May Occur When V_{DD} Drops

The device may experience increased current consumption of approximately 1.5 mA if V_{DD} drops below 2.1V and is held in the range of 1.9-2.1V. This will only occur if V_{DD} is originally at a higher level and then drops down to the mentioned voltage range.

Work Around

Ensure V_{DD} is always kept above 2.1V by setting the BOR trigger level to 2.2V to keep the device from executing if V_{DD} drops towards the affected voltage range. If operation in voltage range 1.9-2.1V is required, make sure V_{DD} does not rise above 2.1V and then drops down again. Note that the voltage levels given are not absolute values but typical values.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.2.3. CRC Check During Reset Initialization Is not Functional

For material with date code 2048 (manufactured in the year 2020, week 48) or older, the CRCSRC bit field in the SYSCFG0 fuse is ignored during Reset initialization. A CRC check will not be performed during Reset initialization. CRCSCAN is only available from the software.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

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2.2.4. Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.3. ADC - Analog-to-Digital Converter

2.3.1. Increased Offset in Single-Ended Mode

The ADC result has a typical offset of -3 mV (V_{DD} = 3.0V, temp. = 25°C) when the ADC is operating in Single-Ended mode. The typical offset drift vs. V_{DD} is -0.3 mV/V, and the typical offset drift vs. temperature is -0.02 mV/°C.

Work Around

To reduce the offset, use the ADC in Differential mode and connect the negative ADC input pin externally to GND.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.3.2. ADC MUX Selection and Accumulation Number has Delayed Update When Initialization Delay is Used

If the initialization delay (INITDLY in ADCn.CTRLD register) is non-zero, an update of ADC MUX Selection (ADCn.MUXPOS or ADCn.MUXNEG) or Sample Accumulation Number (ADCn.CTRLB) after enabling ADC or changing reference selection will not take effect until one ADC measurement is completed.

Work Around

Perform one of the following:

1. Change ADC MUX selection (ADCn.MUXPOS or ADCn.MUXNEG) and Sample Accumulation Numbers (ADCn.CTRLB) before enabling the ADC or changing the reference selection.
2. Perform a dummy conversion after enabling the ADC or changing reference selection.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.4. CCL - Configurable Custom Logic

2.4.1. The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

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Work Around
None

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.4.2. The LINK Input Source Selection for LUT3 Is not Functional on 28- and 32-Pin Devices
The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '0x2') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around
Connect LUT0 output to LUT3 input using the Event System.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.5. CLKCTRL - Clock Controller

2.5.1. External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready
If an external clock source is selected (SELHF in XOSCHFCTRLA is '1') and the Run Standby (RUNSTDBY) bit in XOSCHFCTRLA is '1' without the clock source being requested, the External Clock/Crystal Status (EXTS) bit will not be set to '1' when the external clock source is ready.

Work Around
Request the clock from RTC or TCD before checking the EXTS bit.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.5.2. RUNSTDBY is Not Functional When Using External Clock Sources
When using any of the External Clock Sources, the related Run Standby (RUNSTDBY) bit, found in the XOSC32KCTRLA register, will not force the oscillator source to stay on during sleep modes.

Work Around
Enable a peripheral, with the external oscillator as the clock source, to keep the clock source active during sleep modes.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.5.3. PLL Status not Working as Expected
The PLL Status (PLLS) bit in the Main Clock Status (MCLKSTATUS) register will never be set to '1' if the Run Standby (RUNSTDBY) bit in PLL Control A (PLLCTRLA) register is set to '1' and no peripherals are requesting the PLL oscillator.

Work Around
None.

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Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.5.4. The PLL Will Not Run when Using XOSCHF with an External Crystal

When the PLL is configured to run from an external source (SOURCE in CLKCTRL.PLLCTRLA is '1'), the PLL will only run if XOSCHF is configured to use an external clock (SELHF in CLKCTRL.XOSCHFCTRLA is '1'). It will not work with an external crystal.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.6. DAC - Digital-to-Analog Converter

2.6.1. DAC Output Buffer Lifetime Drift

The offset of the DAC output buffer can drift over the device's lifetime if powered with the DAC output buffer disabled.

Work Around

Keep the DAC output buffer enabled (OUTEN in DACn.CTRLA is '1') continuously or compensate by measuring the DAC output voltage offset with the ADC and adjust the DAC data register value (DATA[9:0] in DACn.DATA) accordingly.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.7. NVMCTRL - Nonvolatile Memory Controller

2.7.1. Flash Multi-Page Erase Can Erase Write Protected Section

When using Flash Multi-Page Erase mode, only the first page in the selected address range is verified to be within a section that is not write-protected. If the address range includes any write-protected Application Data pages, it will erase them.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.7.2. NVM_EEPROM_ERASE Command does Not Respect Write Protect

The NVM_EEPROM_ERASE command does not respect the EEPROM Write Protected (EEWP) bit in the Control B (NVMCTRL.CTRLB) register. Content will be erased even though it should not.

Work Around

None.

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Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.8. OPAMP - Analog Signal Conditioning

2.8.1. OPAMP Consume More Power Than Expected

The OPAMP peripheral consumes up to three times more current than specified when the output is driven closer to either the upper or lower rails.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.8.2. The Input Range Select is Read-Only

The Input Range Select (IRSEL) bit is read-only. When the Analog Signal Conditioning (OPAMP) peripheral is active, the input voltage range will be rail-to-rail.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.9. PORT - I/O Configuration

2.9.1. PD0 Input Buffer is Floating

On 28- and 32-pin package parts, the PD0 input buffer is floating. Because the default direction setting for PD0 is as an input pin, this may cause unexpected current consumption.

Work Around

Disable the PD0 input (ISC in PORTD.PIN0CTRL) or configure the pin as an output (bit 0 in PORTD.DIR).

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.10. RSTCTRL - Reset Controller

2.10.1. BOD Registers not Reset When UPDI Is Enabled

If the UPDI is enabled, the VLMCTRL, INTCTRL, and INTFLAGS registers in BOD will not be reset by other reset sources than POR.

Work Around

None

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Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

2.11. SPI - Serial Peripheral Interface

2.11.1. Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices

Alternative 2 Pin Position is non-functional for the SPI1 instance (SPI1 in PORTMUX.SPIROUTEA is 0x2) with 48-pin devices.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.12. TCA - 16-Bit Timer/Counter Type A

2.12.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.13. TCB - 16-Bit Timer/Counter Type B

2.13.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.13.2. TCB4 Waveform Output Alternative 1 Non-Functional

It is impossible to select TCB4 Waveform Output (WO) alternative 1 (TCB4 in PORTMUX.TCBROUTEA is '0x1') even if pin PC6 exists.

Work Around

None.

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Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.14. TCD - 12-Bit Timer/Counter Type D

2.14.1. Asynchronous Input Events not Working When TCD Counter Prescaler Is Used

When configuring TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0', events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.14.2. CMPAEN Controls All WOx for Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '0x0'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.14.3. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from 0 and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.15. TWI - Two-Wire Interface

2.15.1. The Output Pin Override Does not Function as Expected

It overrides the output pin driver but not the output value when TWI is enabled. The output on the line will always be high when the value in the PORTx.OUT register is '1' for the pins corresponding to the SDA or SCL.

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Work Around

Ensure that the values in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.15.2. Flush Non-Functional

Issuing a Flush by writing to the FLUSH bit in TWIn.MCTRLB can cause the TWI Host to be stuck in the Unknown bus state (see BUSSTATE in TWIn.MSTATUS).

Work Around

Disable and re-enable the Host using the ENABLE bit in TWIn.MCTRLA. An ordinary operation does not require the use of FLUSH.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.16. USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.16.1. Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.16.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

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Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	-

2.16.3. Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	X	X

2.17. ZCD - Zero-Cross Detector

2.17.1. All ZCD Output Selection Bits Are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around

Use the Event System or CCL to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A4	Rev. A5	Rev. B0
X	-	-

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3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002247).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1. Device

3.1.1. FUSE - Configuration and User Fuses

A clarification to the text directly after the FUSES heading has been made.

Fuses are part of the nonvolatile memory and hold factory calibration and device configuration. The fuses can be read by the CPU or the UPDI, but can only be programmed or cleared by the UPDI. The configuration values stored in the fuses are written to their respective target registers at the end of the start-up sequence.

The fuses for peripheral configuration (FUSE) are pre-programmed but can be altered by the user. Altered values in the configuration fuse will be effective only after a Reset.

The fuses are not affected by a Chip erase.

Note: When writing the fuses, all reserved bits must be written to '0'.

3.2. CLKCTRL - Clock Controller

3.2.1. Interrupts

A clarification to the CLKCTRL section has been made. The *Interrupts* section is missing from the *Functional Description* section and is added here. Note that the section number is added as "12.3.x", since it was not included in the data sheet.

12.3.x Interrupts

Table 12-1. Available Interrupt Vectors and Sources

Interrupt Vector Name	Interrupt Source Name	Description	Condition
NMI	CFD	External crystal oscillator or clock source failure	The CFD flag in CLKCTRL.MCLKINTFLAGS is '1' and the INTTYPE bit in CLKCTRL.MCLKINTCTRL is '1'
CLKCTRL	CFD	External crystal oscillator or clock source failure	The CFD flag in CLKCTRL.MCLKINTFLAGS is '1' and the INTTYPE bit in CLKCTRL.MCLKINTCTRL is '0'

When an interrupt condition occurs, the corresponding interrupt flag is set in the peripheral's Interrupt Flags (*peripheral*.INTFLAGS) register.

An interrupt source is enabled or disabled by writing to the corresponding enable bit in the peripheral's Interrupt Control (*peripheral*.INTCTRL) register.

An interrupt request is generated when the corresponding interrupt source is enabled, and the interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared. See the peripheral's INTFLAGS register for details on how to clear interrupt flags.

3.3. RSTCTRL - Reset Controller

3.3.1. Domains Affected By Reset

A clarification has been made to the *Logic Domains Affected by Various Resets* table of the *Operation - Reset Sources - Domains Affected By Reset* section.

Table 14-1. Logic Domains Affected by Various Resets

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Reset Type	Reset of BOD configuration	Fuses are Reloaded	Reset of UPDI	Reset of Other Volatile Logic
POR	**X**	X	X	X
BOD	**X**	X	**X**	X
External Reset		X		X
Watchdog Reset		X		X
Software Reset		X		X
UPDI Reset		X		X

3.4. SLPCTRL - Sleep Controller

3.4.1. Sleep Modes

Some clarifications has been made to tables 13-2 and 13-4 in the *Functional Description - Operation - Sleep Modes* section.

Table 13-2. Sleep Mode Activity for Peripherals

Clock	Peripheral	Active in Sleep Mode			
		Idle	Standby	Power-Down	
				HTLLEN=0	HTLLEN=1
CLK_CPU	CPU	-	-	-	-
CLK_RTC	RTC	X	X(1,2)	X(2)	X(2)
CLK_WDT	WDT	X	X	X	X
CLK_BOD(3)	BOD	X	X	X	X
-(4)	CCL	X	X(1)	-	-
CLK_PER	EVSYS	X	X	X	X
	NVM(5)	**X**	**X**	**X**	**X**
	ACn	X	X(1)	-	-
	ADCn				
	DACn				
	OPAMP				
	TCAn				
	TCBn				
	ZCDn				
	All other peripherals	X	-	-	-

Notes:

1. For the peripheral to run in Standby sleep mode, the RUNSTDBY bit of the corresponding peripheral must be set
2. In Standby sleep mode, only the RTC functionality requires the RUNSTDBY bit to be set. In Power-Down sleep mode, only the PIT functionality is available.
3. **CLK_BOD is required only when the BOD is running in Sampled mode**
4. **The clock domain depends on the clock source selected for CCL**
5. **Programming in progress will be completed, then the NVM peripheral will be disabled**

Table 13-4. Sleep Mode Wake-up Sources

Wake-Up Sources	Active in Sleep Mode			
	Idle	Standby	Power-Down	
			HTLLEN=0	HTLLEN=1
PORT Pin interrupt	X	X(1)	X(1)	X(1)

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Sleep Modes (continued)				
Wake-Up Sources	Active in Sleep Mode			
	Idle	Standby	Power-Down	
			HTLLEN=0	HTLLEN=1
BOD VLM interrupt	X	X	X	X
MVIO interrupts	X	X	X	X
RTC interrupts	X	X(2,3)	X(3)	X(3)
TWI Address Match interrupt	X	X	X	-
CCL interrupts	X	X(2)	X(4)	-
USART Start-Of-Frame interrupt	**X**	X	-	-
TCAn interrupts	X	X(2)	-	-
TCBn interrupts				
ADCn interrupts				
ACn interrupts				
ZCD interrupts				
All other interrupts	X	-	-	-

Notes:

1. The I/O pin must be configured according to *Asynchronous Sensing Pin Properties* in the PORT section
2. For the peripheral to run in Standby sleep mode, the RUNSTDBY bit of the corresponding peripheral must be set
3. In Standby sleep mode, only the RTC functionality requires the RUNSTDBY bit to be set. In Power-Down sleep mode, only the PIT functionality is available.
4. CCL will only wake up the device if the path through LUTn is asynchronous (FILTSEL=`0x0` and EDGEDET=`0x0` in the CCL.LUTnCTRLA register)

3.5. SPI - Serial Peripheral Interface

3.5.1. Client Mode

A clarification has been made to the *Operation - Client Mode* section. The last sentence is removed.

28.3.2.2 Client Mode

In Client mode, the SPI peripheral receives the SPI clock and Client Select from a Host. Client mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Client mode, the control logic will sample the incoming signal on the SCK pin.

3.5.2. Buffer Mode

A clarification has been made to the *Operation - Client Mode - Buffer Mode* section.

28.3.2.2.2 Buffer Mode

To avoid data collisions, the SPI peripheral can be configured in Buffered mode by writing a '`1`' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register.

In this mode, the SPI has additional interrupt flags and extra buffers. The extra buffers are shown in Figure 28-1. There are two different modes for the Buffer mode, selected with the Buffer mode Wait for Receive (BUFWR) bit. The two different modes are described below with timing diagrams.

Note: When operating as a client in Buffered mode and the SPI clock is close to maximum frequency, the client may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

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3.6. UPDI - Unified Program and Debug Interface

3.6.1. UPDI - Reset Controller

Some clarifications has been made to the *Functional Description - Enabling of Key Protected Interfaces - Chip Erase* section.

37.3.7.1 Chip Erase

Follow these steps to issue a chip erase:

1. Enter the Chip Erase key by using the `KEY` instruction. See the *Key Activation Signatures* table in the *Enabling of Key Protected Interfaces* section for the CHIPERASE signature.
2. **Enter the NVM Programming key by using the `KEY` instruction. See the *Key Activation Signatures* table in the *Enabling of Key Protected Interfaces* section for the NVMPROG signature. This will prevent a freshly erased device from failing the CRC (if activated).**
3. **Read the ASI Key Status (UPDI.ASI_KEY_STATUS) register to verify that both the Chip Erase (CHIPER) bit and the NVM Programming Key Status (NVMPROG) bits are set.**
4. **Write the signature to the Reset Request (RSTREQ) bit in the ASI Reset Request (UPDI.ASI_RESET_REQ) register. This will issue a System Reset.**
5. Write `0x00` to the ASI Reset Request (UPDI.ASI_RESET_REQ) register to clear the System Reset.
6. Read the NVM Lock Status (LOCKSTATUS) bit from the ASI System Status (UPDI.ASI_SYS_STATUS) register.
7. The chip erase is done when the LOCKSTATUS bit is '`0`'. If the LOCKSTATUS bit is '`1`', return to step 6.
8. Check the Chip Erase Key Failed (ERASEFAIL) bit in the ASI System Status (UPDI.ASI_SYS_STATUS) register to verify if the chip erase was successful.
9. If the ERASEFAIL bit is '`0`', the chip erase was successful.

After a successful chip erase, the lock bits will be cleared, and the UPDI will have full access to the system. Until the lock bits are cleared, the UPDI cannot access the system bus, and only CS-space operations can be performed.

⚠ CAUTION During chip erase, the BOD is forced in ON state by writing to the Active (ACTIVE) bit field from the Control A (BOD.CTRLA) register and uses the BOD Level (LVL) bit field from the BOD Configuration (FUSE.BODCFG) fuse and the BOD Level (LVL) bit field from the Control B (BOD.CTRLB) register. If the supply voltage V_{DD} is below that threshold level, the device is unavailable until V_{DD} is increased adequately. See the *BOD* section for more details.

3.7. Electrical Characteristics

3.7.1. I/O Pins

A clarification has been made to the *I/O Pin Specification* table.

Table 39-6. I/O Pin Specifications[1][5]

Symbol	Description	Min.	Typ. †	Max.	Units	Conditions
Input Low Voltage						

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I/O Pins (continued)						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
V_{IL}	I/O PORT:					
	• With Schmitt Trigger buffer	—	—	0.2 × V_{DD}	V	PINnCTRL.INLVL = 0x00
	• TTL level	—	—	0.8	V	PINnCTRL.INLVL = 0x01 V_{DD} > 2.7V
	TWI PORT:					
	• With I^2C levels	—	—	0.3 × V_{DD}	V	CTRLA.INPUTLVL = 0x0
	• With SMBus 3.0 levels			0.8	V	CTRLA.INPUTLVL = 0x1
	$\overline{\text{RESET}}$ Pin	—	—	0.2 × V_{DD}	V	
Input High Voltage						
V_{IH}	I/O PORT:					
	• With Schmitt Trigger buffer	0.8 × V_{DD}	—	—	V	PINnCTRL.INLVL = 0x00
	• TTL level	2.0	—	—	V	PINnCTRL.INLVL = 0x01 V_{DD} > 2.7V
	TWI PORT:					
	• With I^2C levels	0.7 × V_{DD}	—	—	V	CTRLA.INPUTLVL = 0x0
	• With SMBus 3.0 levels	1.35	—	—	V	CTRLA.INPUTLVL = 0x1 0°C ≤ T_A ≤ +125°C, 2.5V ≤ V_{DD} ≤ 5.5V
		1.45	—	—	V	CTRLA.INPUTLVL = 0x1 0°C ≤ T_A ≤ +125°C, 1.8V ≤ V_{DD} ≤ 5.5V
	$\overline{\text{RESET}}$ Pin	0.8 × V_{DD}	—	—	V	
Input Leakage Current[2]						
I_{IL}	I/O PORTS[3]	—	±5	±125	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A= 85°C
		—	±5	±1000	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A = 125°C
	$\overline{\text{RESET}}$ Pin[4] *	—	±50	±200	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A= 85°C
Pull-up Current						
I_{PUR}		90	150	200	µA	V_{DD} = 3.0V, V_{PIN} = GND
Output Low Voltage						
V_{OL}	Standard I/O Ports	—	—	0.6	V	I_{OL} = 10 mA, V_{DD} = 3.0V
Output High Voltage						
V_{OH}	Standard I/O Ports	V_{DD} - 0.7	—	—	V	I_{OH} = 6 mA, V_{DD} = 3.0V
I/O Slew Rate						
t_{SR}	Rising slew rate	—	22	—	ns	PORTCTRL.SRL = 0x00
	Rising slew rate	—	45	—	ns	PORTCTRL.SRL = 0x01
	Falling slew rate	—	30	—	ns	PORTCTRL.SRL = 0x01
	Falling slew rate	—	16	—	ns	PORTCTRL.SRL = 0x00
Pin Capacitance						
C_{IO}	OPAMP output	—	9	—	pF	
	V_{REF}pin	—	7	—	pF	
	XTAL pins	—	4	—	pF	
	Other pins	—	4	—	pF	

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I/O Pins (continued)						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

***** These parameters are characterized but not tested in production.

Notes:

1. These figures are valid for all I/O ports regardless of if they are connected to the V_{DD} or V_{DDIO2} power domain.
2. The negative current is the current sourced by the pin.
3. The leakage current numbers for I/O PORTS are valid also when the pin is used as an input to an enabled analog peripheral.
4. The leakage current on the $\overline{\text{RESET}}$ pin strongly depends on the applied voltage level. The specified levels represent normal operating conditions. A higher leakage current may be measured at different input voltages.
5. Input voltage threshold is relative to VDDIO2 on MVIO pins (PORTC) and VDD on other pins.

3.7.2. USART

Some clarifications have been made to the *USART in SPI Host Mode - Timing Specifications* table. Note that some rows have been deleted.

Table 39-19. USART in SPI Host Mode - Timing Requirements in Host Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SCK} *	SCK clock frequency	—	—	**$f_{CLK\_PER}/2$**	MHz	
T_{SCK} *	SCK period	**$2 \times T_{CLK\_PER}$**	—	—	ns	
t_{SCKW}	SCK high/low width	—	0.5 × T_{SCK}	—	ns	
t_{MIS}	MISO setup to SCK	—	**T_{CLK_PER}**	—	ns	
t_{MIH}	MISO hold after SCK	—	**0**	—	ns	
t_{MOS}	MOSI setup to SCK	—	0.5 × T_{SCK}	—	ns	
t_{MOH}	MOSI hold after SCK	—	**$0.5 \times T_{SCK}$**	—	ns	

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

* These parameters are characterized but not tested in production.

3.7.3. SPI

Some clarifications have been made to the *Timing Specifications in Host Mode* and *Timing Specifications in Client Mode* tables. Note that some rows have been deleted.

Table 39-20. SPI - Timing Specifications in Host Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SCK} *	SCK clock frequency	—	—	**$f_{CLK\_PER}/2$**	MHz	
T_{SCK} *	SCK period	**$2 \times T_{CLK\_PER}$**	—	—	ns	
t_{SCKW}	SCK high/low width	—	0.5 × T_{SCK}	—	ns	
t_{MIS}	MISO setup to SCK	—	**T_{CLK_PER}**	—	ns	
t_{MIH}	MISO hold after SCK	—	**0**	—	ns	
t_{MOS}	MOSI setup to SCK	—	0.5 × T_{SCK}	—	ns	
t_{MOH}	MOSI hold after SCK	—	**$0.5 \times T_{SCK}$**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Table 39-21. SPI - Timing Specifications in Client Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SSCK} *	Client SCK clock frequency	—	—	**$f_{CLK\_PER}/6$**	MHz	

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SPI (continued)						
Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
T_{SSCK} *	Client SCK period	**6 × T_{CLK_PER}**	—	—	ns	
t_{SSCKW} *	SCK high/low width	**3 × T_{CLK_PER}**	—	—	ns	
t_{SIS} *	MOSI setup to SCK	**0**	—	—	ns	
t_{SIH} *	MOSI hold after SCK	**3 × T_{CLK_PER}**	—	—	ns	
t_{SSS} *	SS setup to SCK	**T_{CLK_PER}**	—	—	ns	
t_{SSH} *	SS hold after SCK	**T_{CLK_PER}**	—	—	ns	
t_{SOS}	**MISO valid after SCK**	—	**t_{SR}**	—	ns	**$f_{SSCK} \geq f_{CLK\_PER}/6$**
			—			**$f_{SSCK} < f_{CLK\_PER}/6$**
t_{SOSS}	MISO setup after SS low	—	**t_{SR}**	—	ns	
t_{SOSH}	MISO hold after SS low	—	**t_{SR}**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

3.7.4. AC

Some clarifications has been made to the *Analog Comparator Specifications* table.

Table 39-23. Analog Comparator Specifications

Operating Conditions: **V_{DD} = 3.0V** **V_{ACREF} = V_{DD}** **T_A = 25°C**						
Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
V_{IN}*	Input voltage range	-0.2	—	V_{DD}	V	
I_L	Input leakage current	—	5	—	nA	
V_{OFF}	Input offset voltage	-11	±5	11	mV	0.7V < V_{IN} < (V_{DD} - 0.7V)
		-15	±5	15		0.1V < V_{IN} < (V_{DD} - 0.1V)
CMRR	Common mode input rejection ratio	—	70	—	dB	0.1V < V_{IN} < (V_{DD} - 0.1V)
V_{HYST}	Hysteresis	—	10	—	mV	CTRLA.HYSMODE = `0x1`
		—	25	—		CTRLA.HYSMODE = `0x2`
		—	50	—		CTRLA.HYSMODE = `0x3`
t_{RESP}*	Response time, rising edge	—	85	120	ns	CTRLA.POWER = `0x0`,
	Response time, falling edge	—	85	120	ns	V_{CM} = V_{DD}/2
	Response time, rising edge	—	250	350	ns	CTRLA.POWER = `0x1`,
	Response time, falling edge	—	220	300	ns	V_{CM} = V_{DD}/2
	Response time, rising edge	—	460	680	ns	CTRLA.POWER = `0x2`,
	Response time, falling edge	—	430	550	ns	V_{CM} = V_{DD}/2
t_{DACREF}(1)	**AC DACREF initialization time**	**—**	**25**	**—**	**µs**	

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

***** These parameters are characterized but not tested in production.

Note:

1. **When DACREF is used with an internal reference, the settling time might be longer depending on whether the bandgap reference is initially running or not. The number given assumes the bandgap reference is initially running. See the *VREF* section for VREF start-up time.**

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3.7.5. ADC

A clarification has been made to the Operating Conditions (heading) of the *ADC Accuracy Specifications* table. One item (t_{ADC_DACREF}) is added to the *ADC Conversion Timing Specifications* table.

Table 39-24. ADC Accuracy Specifications

Operating Conditions: **V_{DD} = 3.0V** **V_{ADCREF} = 3.0V** **T_A = 25°C** **ADC in single ended conversion mode** **f_{CLK_ADC} = 500 kHz**						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
N_R	Resolution	—	—	12	bit	
E_{INL}	Integral non-linearity error	-1.8	0.1	1.8	LSb	
E_{DNL}(1)	Differential non-linearity error	-1	0.1	1	LSb	
E_{OFF}	Offset error	-5	2.5	5	LSb	
E_{GAIN}	Gain error	-5	1.5	5	LSb	
V_{ADCREF} *	ADC reference voltage	1.024	—	V_{DD}	V	$f_{CLK\_ADC} \leq 500$ kHz
		1.8	—	V_{DD}	V	125 kHz ≤ f_{ADC_CLK} ≤ 2 MHz
V_{AIN}	Full-scale range	GND	—	V_{ADCREF}	V	
Z_{AIN}	Recommended impedance of analog voltage source	—	10	—	kΩ	
R_{VREFA}(2)	ADC voltage reference ladder impedance	—	50	—	kΩ	
	V_{DD}/10 divider accuracy (VDDDIV10 / VDDIO2DIV10)	—	±10	—	%	Measured with ADC using on-chip internal reference

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

***** These parameters are characterized but not tested in production.

Notes:

1. The ADC conversion result never decreases with an increase in the input and has no missing codes.
2. This is the impedance seen by the VREFA pin when the external reference is selected.

Table 39-25. ADC Conversion Timing Specifications

Operating Conditions: **V_{DD} = 3.0V** **V_{ADCREF} = 3.0V** **T_A = 25°C**						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
T_{CLK_ADC}*	ADC clock period	1	—	8	µs	
t_{CNV}	Conversion time	—	$13.5T_{CLK\_ADC} + 2T_{CLK\_PER}$	—		
f_{ADC}*	Sample rate	8	—	130	ksps	
t_{SENSE}	Delay for changing MUXPOS to TEMP	—	40	—	µs	
t_{ADC_INIT}	ADC Initialization time	—	6	—	µs	
t_{ADC_DACREF}	**ADC sampling time with DACREFn as input for MUXPOS**	**—**	**30**	**—**	**µs**	

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ADC (continued)						
Operating Conditions: **V_{DD} = 3.0V** **V_{ADCREF} = 3.0V** **T_A = 25°C**						
Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested. * These parameters are characterized but not tested in production.						

3.7.6. DAC

Some clarifications has been made to the Operation Conditions (heading) in the *DAC Electrical Specifications* table.

Table 39-26. DAC Electrical Specifications

Operating Conditions: **V_{DD} = 3.0V** **V_{DACREF} = 3.0V** **T_A = 25°C**						
Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
V_{DD}	Supply voltage	1.8	—	5.5	V	
V_{OUT}	Output voltage range	0.1	—	V_{DD} - 0.1	V	I_{OH} max. (current sourcing) = 1 mA I_{OL} max. (current sinking) = 0.001 mA(2)
V_{LSB}	Resolution	—	10	—	Bit	
V_{ACC}	Absolute accuracy	-10	1	10	LSb	
t_{ST}	Settling Time(1)	—	7	—	µs	V_{DACREF} = V_{DD} = 3.0V, 50 pF Load
		—	10	—	µs	V_{DACREF} = V_{DD} = 5.5V, 50 pF Load
INL	Integral non-linearity	-2.3	1	2.3	LSb	0x030 ≤ DAC.DATA < 0x3D0
DNL	Differential non-linearity	-0.7	0.2	0.7	LSb	0x030 ≤ DAC.DATA < 0x3D0
E_{OFF}	Offset error	-5	2.8	5	LSb	
E_{GAIN}	Gain error	-3.3	-1.1	1.3	LSb	

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are for design guidance only and are not tested.

Notes:

1. Settling time measured while DAC.DATA[9:0] transitions from '0x000' to '0x3FF'.
2. The DAC output has a limited current sinking capability. It is designed to drive against resistive loads connected to ground. It is recommended to increase the sinking capability by placing a suitable resistor between the DAC output pin and ground if the DAC peripheral may sink current.

3.8. Characteristics Graphs

3.8.1. BOD

A clarification was made to the *BOD* section in *Characteristics Graphs*.

One plot has been removed: **Figure 40-51. BOD Response Time vs. Temperature**. As a result, the *BOD* section of the *Characteristics Graphs* section now is reduced from 13 to 12 plots and look like the following.

40.4.4 BOD

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Figure 40-50. BOD Minimum Reset Pulse Width vs. Temperature

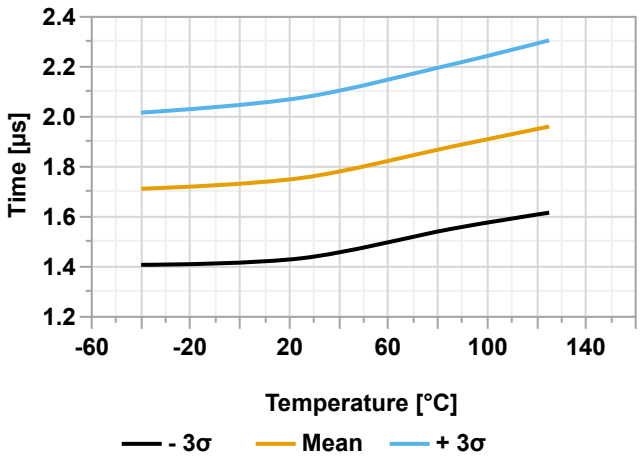

Figure 40-51. BOD Threshold Level vs. Temperature (BODCFG.LVL = 0x00)

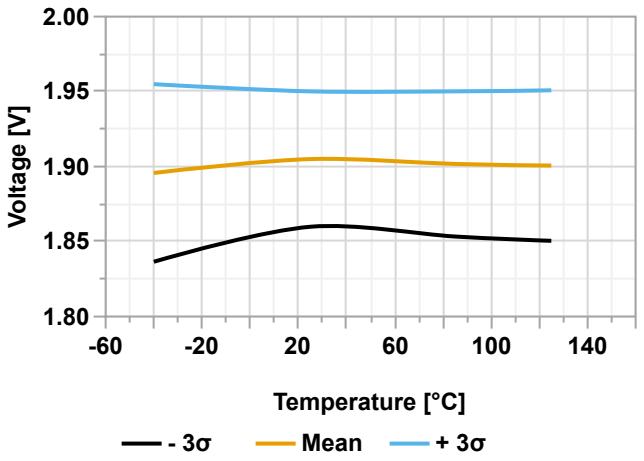

Figure 40-52. BOD Threshold Level vs. Temperature (BODCFG.LVL = 0x01)

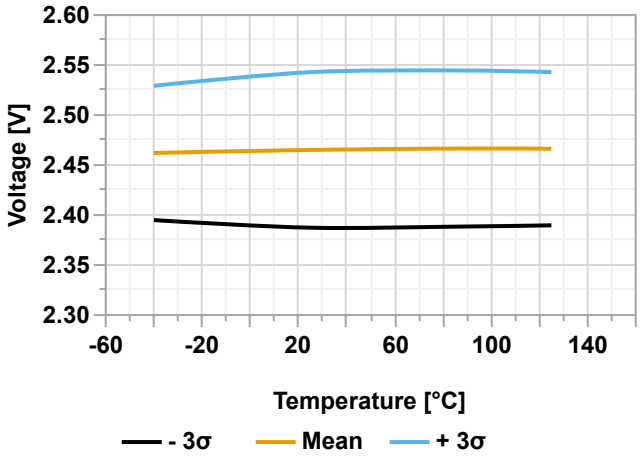

Figure 40-53. BOD Threshold Level vs. Temperature (BODCFG.LVL = 0x02)

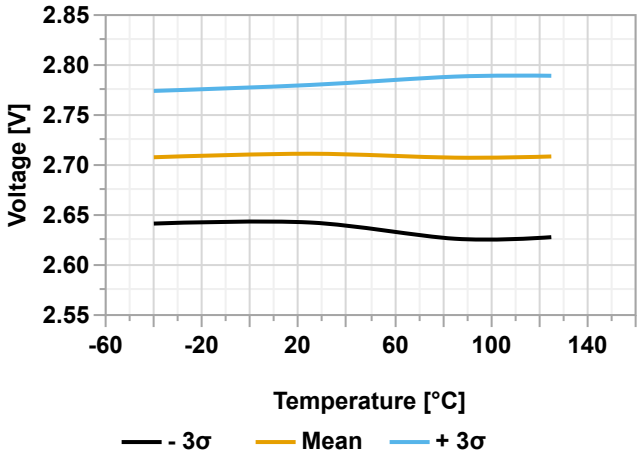

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Figure 40-54. BOD Threshold Level vs. Temperature (BODCFG.LVL = 0x03)

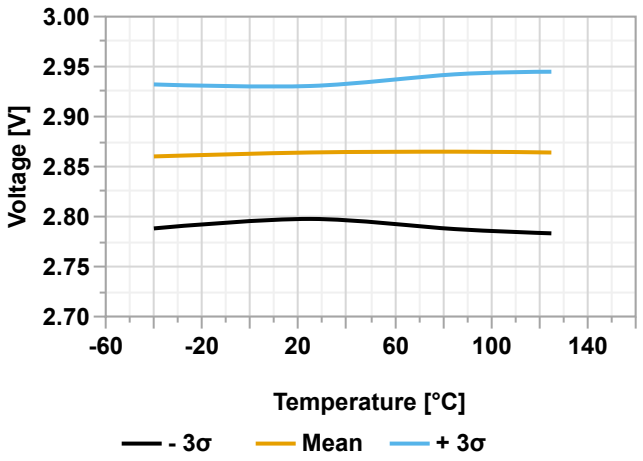

Figure 40-55. BOD Hysteresis vs. Temperature (BODCFG.LVL = 0x00)

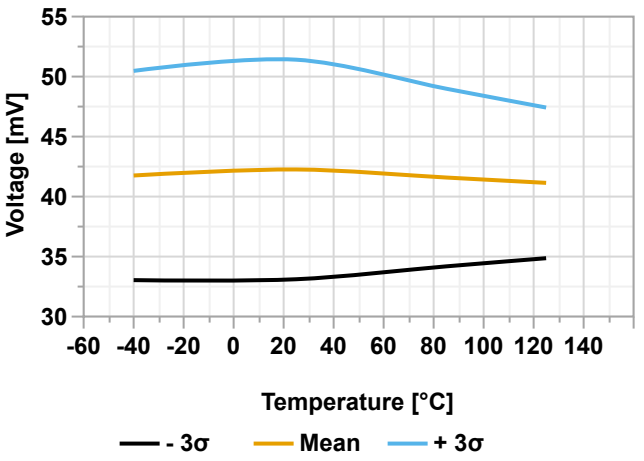

Figure 40-56. BOD Hysteresis vs. Temperature (BODCFG.LVL = 0x01)

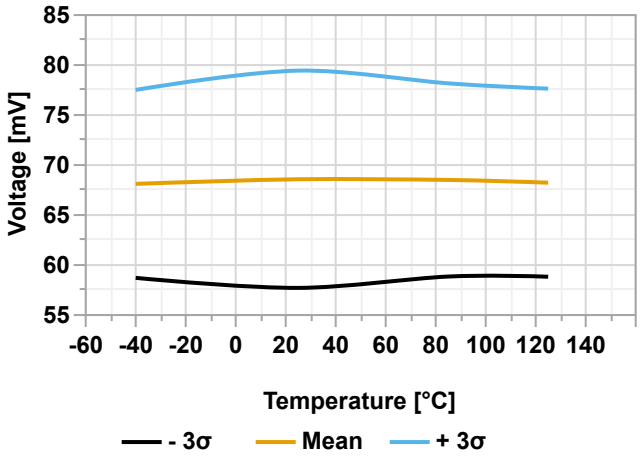

Figure 40-57. BOD Hysteresis vs. Temperature (BODCFG.LVL = 0x02)

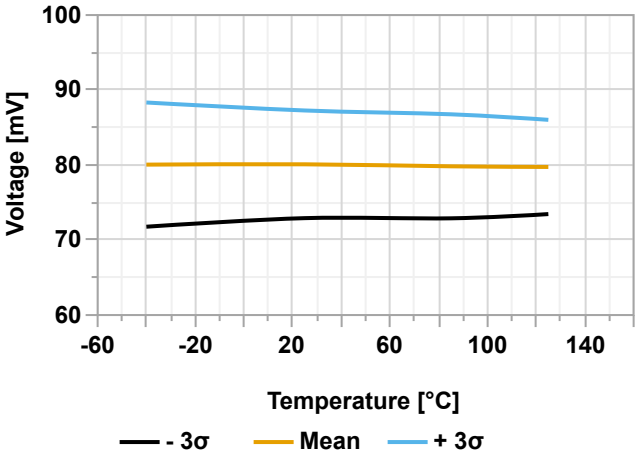

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Figure 40-58. BOD Hysteresis vs. Temperature (BODCFG.LVL = 0x03)

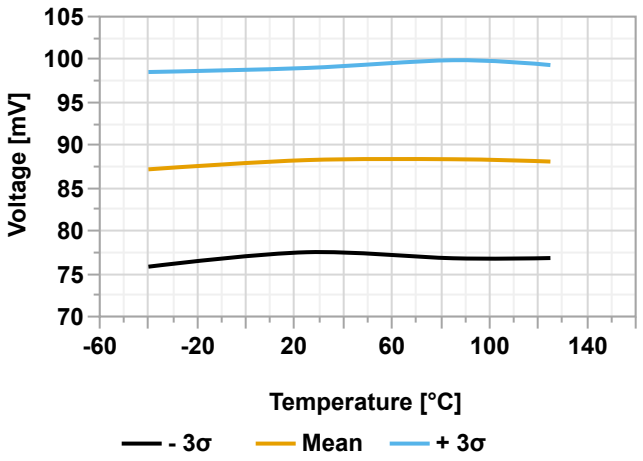


Figure 40-59. VLM Threshold vs. Temperature (VLMCTRL.VLMLVL = 0x01)

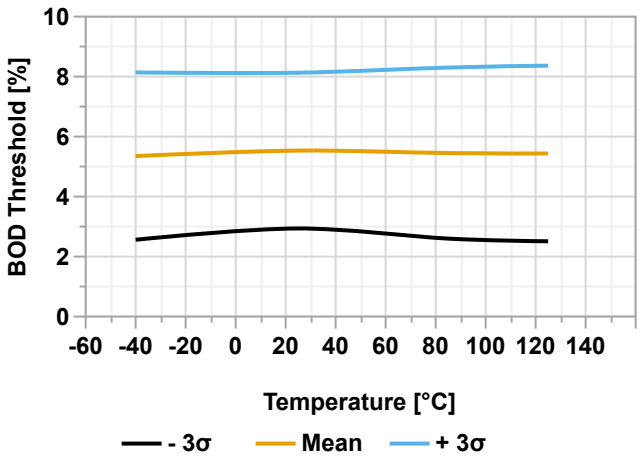


Figure 40-60. VLM Threshold vs. Temperature (VLMCTRL.VLMLVL = 0x02)

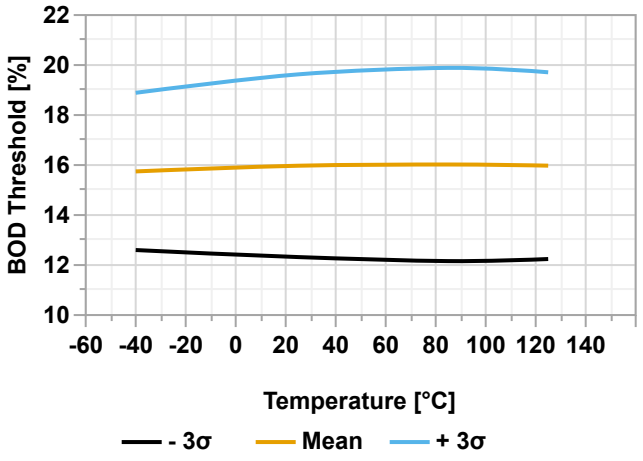
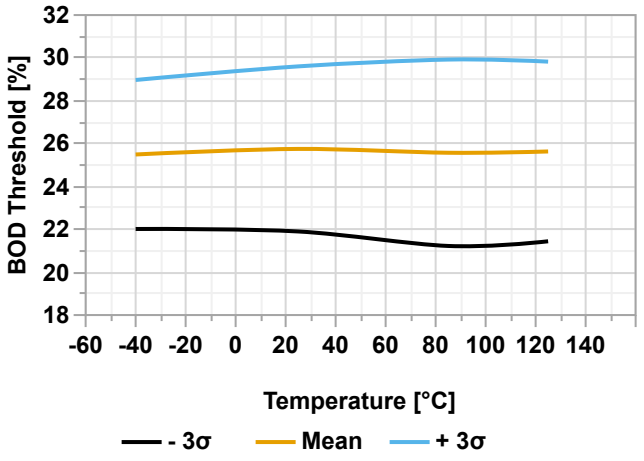


Figure 40-61. VLM Threshold vs. Temperature (VLMCTRL.VLMLVL = 0x03)



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4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1. Revision History

Doc. Rev.	Date	Comments
F	04/2025	• Document: – General editorial updates – Back Matter and PDF front cover updates • Added Erratum for silicon Rev. A4, Rev. A5 and Rev. B0: – ADC: ADC MUX Selection and Accumulation Number has Delayed Update When Initialization Delay is Used – TCB: TCB4 Waveform Output Alternative 1 Non-Functional • Added Data Sheet Clarifications: – Device: FUSE - Configuration and User Fuses – CLKCTRL - Clock Controller: Interrupts – RSTCTRL - Reset Controller: Domains Affected By Reset – SLPCTRL - Sleep Controller: Sleep Modes – SPI - Serial Peripheral Interface: Client Mode – SPI - Serial Peripheral Interface: Buffer Mode – UPDI - Unified Program and Debug Interface: UPDI - Reset Controller – Electrical Characteristics: USART – Electrical Characteristics: AC – Electrical Characteristics: ADC – Electrical Characteristics: DAC – Characteristics Graphs: BOD
E	04/2024	• Document: General editorial updates • Added Errata for silicon Rev. B0: – Device: Write Operation Lost if Consecutive Writes to Specific Address Spaces – NVMCTRL: NVM_EEPROM_ERASE Command does Not Respect Write Protect – PORT: PD0 Input Buffer is Floating – TCD: Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used – TWI: Flush Non-Functional – USART: Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Added Data Sheet Clarifications: – SPI: Client Mode – SPI: Buffer Mode – Electrical Characteristics: I/O Pins – Electrical Characteristics: SPI
D	12/2022	• Added Errata: – SPI: Alternative 2 Pin Position is Non-Functional for SPI1 with 48-Pin Devices – USART: Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Document: General editorial updates • Removed all data sheet clarifications as they are fixed in the device data sheet revision B

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Revision History (continued)

Doc. Rev.	Date	Comments
C	03/2022	Document: General editorial updates. Added errata: • Device: CRC Check During Reset Initialization Is not Functional • CLKCTRL: PLL Status not Working as Expected • DAC: DAC Output Buffer Lifetime Drift • NVMCTRL: Flash Multi-Page Erase Can Erase Write Protected Section • TCA: Restart Will Reset Counter Direction in NORMAL and FRQ Mode • TCD: Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is 0 or Dual Slope Mode is Used • TWI: Flush Non-Functional Updated errata: • USART: Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode Added data sheet clarifications: • Features • FUSE - Configuration and User Fuses - SYSCFG0 • Peripherals and Architecture - REVID • Voltage Regulator Control (VREGCTRL) • Single-Shot Mode • Analog Comparator Interrupt Control • DAC Output • Electrical Characteristics - Memory Programming Specifications
B	10/2020	Added errata: • Device: *Increased Current Consumption May Occur When VDD Drops* • CLKCTRL: *The PLL Will Not Run When Using XOSCHF With an External Crystal* • TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* • TCD: – *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – *CMPAEN Controls All WOx For Alternative Pin Functions* Updated errata: • CCL: – *The CCL Must be Disabled to Change the Configuration of a Single LUT* – *The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32- pin Devices* • ZCD: *All ZCD Output Selection Bits are Tied to the ZCD0 Bit* Added data sheet clarification: Added Typical Characteristics section with additional plots for OPAMP peripheral.
A	08/2020	Initial document release

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