

# Silicon Errata and Data Sheet Clarifications

ATtiny1624/1626/1627



[Product Page Links](#)

## Introduction

The ATtiny1624/1626/1627 devices you have received conform functionally to the current device data sheet ([www.microchip.com/DS40002234](http://www.microchip.com/DS40002234)), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny1624/1626/1627 devices.

### Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet ([www.microchip.com/DS40002234](http://www.microchip.com/DS40002234)) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

# 1. Silicon Issue Summary

## Legend

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. E <sup>(1)</sup>
Device	IDD Power-Down Current Consumption	X
	Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
ADC	ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode	X
CCL	The CCL Must be Disabled to Change the Configuration of a Single LUT	X
NVMCTRL	Wrong Reset Value of NVMCTRL.CTRLA Register	X
TCA	Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X
USART	Open-Drain Mode Does not Work When TXD Is Configured as Output	X
	Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X
	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

### Note:

1. This revision is the initial release of the silicon.

## 2. Silicon Errata Issues

### 2.1. Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

### 2.2. Device

#### 2.2.1. IDD Power-Down Current Consumption

For material with date code 2045 (manufactured in the year 2020, week 45) or older, the IDD power-down leakage can exceed the targeted maximum value of 1.5  $\mu$ A.

##### Work Around

None.

##### Affected Silicon Revisions

Rev. E
X

#### 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

##### Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when the OSC20M oscillator is used as the Main Clock source.

##### Affected Silicon Revisions

Rev. E
X

### 2.3. ADC - Analog-to-Digital Converter

#### 2.3.1. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode

If the Low Latency bit (LOWLAT in ADCn.CTRLA) is '1', the ADC stays active when the device enters Power-Down or Standby sleep modes. If the Free-Running bit (FREERUN in ADCn.CTRLF) is '1', the ADC continues to run in Standby sleep mode even if the Run in Standby bit (RUNSTDBY in ADCn.CTRLA) is '0'. In both cases, the interrupts will not trigger when the device enters Power-Down or Standby sleep mode.

##### Work Around

None.

##### Affected Silicon Revisions

Rev. E
X

## 2.4. CCL - Configurable Custom Logic

### 2.4.1. The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

#### Work Around

None

#### Affected Silicon Revisions

Rev. E
X

## 2.5. NVMCTRL - Nonvolatile Memory Controller

### 2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the reset value of NVMCTRL.CTRLA will not be '0'. Even reserved bits can be read as '1' after Reset.

#### Work Around

Ignore the initial value.

#### Affected Silicon Revisions

Rev. E
X

## 2.6. TCA - 16-Bit Timer/Counter Type A

### 2.6.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

#### Work Around

None.

#### Affected Silicon Revisions

Rev. E
X

## 2.7. TCB - 16-Bit Timer/Counter Type B

### 2.7.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

#### Work Around

Use 16-bit register access. Refer to the data sheet for further information.

#### Affected Silicon Revisions

Rev. E

X

## 2.8. USART - Universal Synchronous and Asynchronous Receiver and Transmitter

### 2.8.1. Open-Drain Mode Does not Work When TXD Is Configured as Output

When configured as an output, the USART TXD pin can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

#### Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

#### Affected Silicon Revisions

Rev. E
X

### 2.8.2. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

#### Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

#### Affected Silicon Revisions

Rev. E
X

### 2.8.3. Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

#### Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

#### Affected Silicon Revisions

Rev. E

X

### 3. Data Sheet Clarifications

Note the following typographical corrections and clarifications for the latest version of the device data sheet ([www.microchip.com/DS40002234](http://www.microchip.com/DS40002234)).

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

#### 3.1. EVSYS - Event Sysytem

### 3.1.1. User Channel MUX

**Name:** USER  
**Offset:** 0x20 + n\*0x01 [n=0..19]  
**Reset:** 0x00  
**Property:** -

A clarification is made in the table of *User Channel MUX* section. Functional change is shown in **bold**.

Each event user can be connected to one channel, and several users can be connected to the same channel. The following table lists all Event System users with their corresponding user ID numbers and names. The user name is formed by combining USER with Peripheral and Input from the table below in the following way: USERPERIPHERALINPUT.

Bit	7	6	5	4	3	2	1	0
	USER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 7:0 – USER[7:0] User Channel Selection

Configures which Event System channel the user is connected to.

USER			Async/Sync	Description
#	Name	Input		
	Peripheral	Input		
0x00	CCL	LUT0A	Async	CCL LUT0 event input A
0x01		LUT0B		CCL LUT0 event input B
0x02		LUT1A		CCL LUT1 event input A
0x03		LUT1B		CCL LUT1 event input B
0x04		LUT2A		CCL LUT2 event input A
0x05		LUT2B		CCL LUT2 event input B
0x06		LUT3A		CCL LUT3 event input A
0x07		LUT3B		CCL LUT3 event input B
0x08	ADC0	START	Async	ADC start on event
0x09	EVSYS	EVOUTA	Async	EVSYS pin output A
0x0A		EVOUTB		EVSYS pin output B
0x0B		EVOUTC <sup>(1)</sup>		EVSYS pin output C
0x0C	USART0	IRDA	Sync	USART0 IrDA event input
0x0D	USART1	IRDA	Sync	USART1 IrDA event input
0x0E	TCA0	CNTA	Sync	Count on event or control count direction
0x0F		CNTB		Restart on event or control count direction
0x10	TCB0	CAPT	Both <sup>(2)</sup>	Start, stop, capture, restart or clear counter
0x11		COUNT	Sync	Count on event
0x12	TCB1	CAPT	Both <sup>(2)</sup>	Start, stop, capture, restart or clear counter
0x13		COUNT	Sync	Count on event

#### Notes:

- Not all peripheral instances are available for all pin counts. Refer to the *Peripherals and Architecture* section for details.
- Depends on the timer operational mode.

Value	Description
0	OFF, No channel is connected to this Event System user
n	The event user is connected to CHANNEL(n-1)

## 3.2. I/O Multiplexing and Considerations

### 3.2.1. I/O Multiplexing

A clarification is made in *Table 3-1. PORT Function Multiplexing*. The “footnote 4” is also valid for LUT0-OUT on pin PB4. Functional change is shown in **bold**.

**Table 3-1. PORT Function Multiplexing**

VQFN 24-pin	VQFN 20-pin	SSOP/SOIC 20-pin	TSSOP/SOIC 14-pin	Pin Name (1,2)	Other/ Special	ADC0 <sup>(3)</sup>	AC0	USART0	USART1	SPI0	TWI0	TCA0	TCBn	CCL
23	19	16	10	PA0	RESET UPDI									LUT0-IN0
24	20	17	11	PA1		AIN1		TXD <sup>(4)</sup>	TXD	MOSI				LUT0-IN1
1	1	18	12	PA2	EVOUTA	AIN2		RxD <sup>(4)</sup>	RXD	MISO				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3		XCK <sup>(4)</sup>	XCK	SCK		WO3	1,WO	
3	3	20	14	GND										
4	4	1	1	VDD										
5	5	2	2	PA4		AIN4		XDIR <sup>(4)</sup>	XDIR	SS		WO4		LUT0-OUT
6	6	3	3	PA5	VREFA	AIN5	OUT					WO5	0,WO	LUT3-OUT <sup>(4)</sup>
7	7	4	4	PA6		AIN6	AINN0							
8	8	5	5	PA7	EVOUTA <sup>(4)</sup>	AIN7	AINP0							LUT1-OUT
9				PB7	EVOUTB <sup>(4)</sup>									
10				PB6			AINP3							LUT2-OUT <sup>(4)</sup>
11	9	6		PB5	CLKOUT	AIN8	AINP1					WO2 <sup>(4)</sup>		
12	10	7		PB4	RESET <sup>(4)</sup>	AIN9	AINN1					WO1 <sup>(4)</sup>		LUT0-OUT <sup>(4)</sup>
13	11	8	6	PB3	TOSC1			RxD				WO0 <sup>(4)</sup>		LUT2-OUT
14	12	9	7	PB2	TOSC2 EVOUTB			TxD				WO2		LUT2-IN2
15	13	10	8	PB1		AIN10	AINP2	XCK			SDA	WO1		LUT2-IN1
16	14	11	9	PB0		AIN11	AINN2	XDIR			SCL	WO0		LUT2-IN0
17	15	12		PC0		AIN12			XCK <sup>(4)</sup>	SCK <sup>(4)</sup>			0,WO <sup>(4)</sup>	LUT3-IN0
18	16	13		PC1		AIN13			RxD <sup>(4)</sup>	MISO <sup>(4)</sup>				LUT1-OUT <sup>(4)</sup> LUT3-IN1
19	17	14		PC2	EVOUTC	AIN14			TxD <sup>(4)</sup>	MOSI <sup>(4)</sup>				LUT3-IN2
20	18	15		PC3		AIN15			XDIR <sup>(4)</sup>	SS <sup>(4)</sup>		WO3 <sup>(4)</sup>		LUT1-IN0
21				PC4								WO4 <sup>(4)</sup>	1,WO <sup>(4)</sup>	LUT1-IN1 LUT3-OUT
22				PC5								WO5 <sup>(4)</sup>		LUT1-IN2

#### Notes:

1. Pin names are Pxn type, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx\_PINn.
2. All pins can be used for external interrupt where pins Px2 and Px6 of each port have full asynchronous detection. All pins can be used as event input.
3. AIN[15:8] can not be used as negative ADC input for differential measurements.
4. Alternative pin location. For selecting an alternative pin location, refer to the PORTMUX section.

### 3.3. Electrical Characteristics

#### 3.3.1. I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor is made in *Table 33-16 in the Electrical Characteristics* section. Functional change is shown in **bold**.

Operating conditions:

- $T_A = [-40, 125]^\circ\text{C}$
- $V_{DD} = [1.8, 5.5]\text{V}$ , unless otherwise specified

**Table 33-16. I/O Pin Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low-voltage, except $\overline{\text{RESET}}$ pin as I/O		-0.2	-	$0.3 \times V_{DD}$	V
$V_{IH}$	Input high-voltage, except $\overline{\text{RESET}}$ pin as I/O		$0.7 \times V_{DD}$	-	$V_{DD} + 0.2\text{V}$	V
$I_{IH} / I_{IL}$	I/O pin Input leakage current, except $\overline{\text{RESET}}$ pin as I/O	$V_{DD} = 5.5\text{V}$ , Pin high	-	< 0.05	-	$\mu\text{A}$
		$V_{DD} = 5.5\text{V}$ , Pin low	-	< 0.05	-	
$V_{OL}$	I/O pin drive strength	$V_{DD} = 1.8\text{V}$ , $I_{OL} = 1.5\text{ mA}$	-	-	0.36	V
		$V_{DD} = 3.0\text{V}$ , $I_{OL} = 7.5\text{ mA}$	-	-	0.6	
		$V_{DD} = 5.0\text{V}$ , $I_{OL} = 15\text{ mA}$	-	-	1	
$V_{OH}$	I/O pin drive strength	$V_{DD} = 1.8\text{V}$ , $I_{OH} = 1.5\text{ mA}$	1.44	-	-	V
		$V_{DD} = 3.0\text{V}$ , $I_{OH} = 7.5\text{ mA}$	2.4	-	-	
		$V_{DD} = 5.0\text{V}$ , $I_{OH} = 15\text{ mA}$	4	-	-	
$I_{total}$	Maximum combined I/O sink current per pin group <sup>(1)</sup>		-	-	100	mA
	Maximum combined I/O source current per pin group <sup>(1)</sup>		-	-	100	
$V_{IL2}$	Input low-voltage on $\overline{\text{RESET}}$ pin as I/O		-0.2	-	$0.3 \times V_{DD}$	V
$V_{IH2}$	Input high-voltage on $\overline{\text{RESET}}$ pin as I/O		$0.7 \times V_{DD}$	-	$V_{DD} + 0.2\text{V}$	V
$V_{OL2}$	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	$V_{DD} = 1.8\text{V}$ , $I_{OL} = 0.1\text{ mA}$	-	-	0.36	V
		$V_{DD} = 3.0\text{V}$ , $I_{OL} = 0.25\text{ mA}$	-	-	0.6	
		$V_{DD} = 5.0\text{V}$ , $I_{OL} = 0.5\text{ mA}$	-	-	1	
$V_{OH2}$	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	$V_{DD} = 1.8\text{V}$ , $I_{OH} = 0.1\text{ mA}$	1.44	-	-	V
		$V_{DD} = 3.0\text{V}$ , $I_{OH} = 0.25\text{ mA}$	2.4	-	-	
		$V_{DD} = 5.0\text{V}$ , $I_{OH} = 0.5\text{ mA}$	4	-	-	
$t_{RISE}$	Rise time	$V_{DD} = 3.0\text{V}$ , load = 20 pF	-	2.5	-	ns
		$V_{DD} = 5.0\text{V}$ , load = 20 pF	-	1.5	-	
$t_{FALL}$	Fall time	$V_{DD} = 3.0\text{V}$ , load = 20 pF	-	2.0	-	ns
		$V_{DD} = 5.0\text{V}$ , load = 20 pF	-	1.3	-	
$C_{PIN}$	I/O pin capacitance, unless otherwise specified		-	4	-	pF
$C_{PIN\_TOSC}$	I/O pin capacitance on TOSC pins <sup>(2)</sup>		-	5	-	pF
$C_{PIN\_TWI}$	I/O pin capacitance on TWI pins <sup>(2)</sup>		-	12	-	pF
$C_{PIN\_AC}$	I/O pin capacitance on AC pins <sup>(2)</sup>	PB0 and PB1	-	12	-	pF
		other AC pins	-	4	-	
$C_{PIN\_VREFA}$	I/O pin capacitance on ADC VREFA pin		-	14	-	pF
$R_p$	Pull-up resistor		20	35	<b>60</b>	k $\Omega$

**Notes:**

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.
2. This capacitance is valid for pins with this functionality, even when that functionality is unused.

### 3.3.2. SPI - Timing Characteristics

A clarification regarding the SPI clock is made in *Table 33-18. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

**Table 33-18. SPI - Timing Characteristics<sup>(1)</sup>**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$f_{SCK}$	SCK clock frequency	Host	-	-	10	MHz
$t_{SCK}$	SCK period	Host	100	-	-	ns
$t_{SCKW}$	SCK high/low width	Host	-	$0.5 \times t_{SCK}$	-	ns
$t_{SCKR}$	SCK rise time	Host	-	2.7	-	ns
$t_{SCKF}$	SCK fall time	Host	-	2.7	-	ns
$t_{MIS}$	MISO setup to SCK	Host	-	10	-	ns
$t_{MIH}$	MISO hold after SCK	Host	-	10	-	ns
$t_{MOS}$	MOSI setup to SCK	Host	-	$0.5 \times t_{SCK}$	-	ns
$t_{MOH}$	MOSI hold after SCK	Host	-	1.0	-	ns
$f_{SSCK}$	Client SCK clock frequency	Client	-	-	5	MHz
$t_{SSCK}$	Client SCK Period	Client	<b><math>6 \times t_{CLK\_PER}</math></b>	-	-	ns
$t_{SSCKW}$	SCK high/low width	Client	<b><math>3 \times t_{CLK\_PER}</math></b>	-	-	ns
$t_{SSCKR}$	SCK rise time	Client	-	-	1600	ns
$t_{SSCKF}$	SCK fall time	Client	-	-	1600	ns
$t_{SIS}$	MOSI setup to SCK	Client	<b>0.0</b>	-	-	ns
$t_{SIH}$	MOSI hold after SCK	Client	<b><math>3 \times t_{CLK\_PER}</math></b>	-	-	ns
$t_{SSS}$	SS setup to SCK	Client	-	<b><math>t_{CLK\_PER}</math></b>	-	ns
$t_{SSH}$	SS hold after SCK	Client	-	<b><math>t_{CLK\_PER}</math></b>	-	ns
$t_{SOS}$	MISO setup to SCK	Client	-	8.0	-	ns
$t_{SOH}$	MISO hold after SCK	Client	-	13	-	ns
$t_{SOSS}$	MISO setup after SS low	Client	-	11	-	ns
$t_{SOSH}$	MISO hold after SS low	Client	-	8.0	-	ns

**Note:**

1. These parameters are for design guidance only and are not production-tested.

### 3.3.3. Programming Time

A clarification of the *Programming Time* section is made. *Table 33-34* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional changes are shown in **bold**.

**Table 33-34. Memory Programming Specifications**

Symbol	Description	Min.	Typ.†	Max.	Unit	Conditions
<b>Data EEPROM Memory Specifications</b>						
$E_{EE}^*$	<b>Data EEPROM byte endurance</b>	<b>100k</b>	—	—	<b>Erase/Write cycles</b>	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
$t_{EE\_RET}$	<b>Characteristic retention</b>	—	<b>40</b>	—	<b>Year</b>	$T_A = 55^{\circ}\text{C}$
$t_{EE\_PBC}$	Page Buffer Clear (PBC)	—	7	—	CLK <sub>CPU</sub> cycles	
$t_{EE\_EEER}$	Full EEPROM Erase (EEER)	—	4	—	ms	
$t_{EE\_WP}$	Page Write (WP)	—	2	—	ms	
$t_{EE\_ER}$	Page Erase (ER)	—	2	—	ms	
$t_{EE\_ERWP}$	Page Erase-Write (ERWP)	—	4	—	ms	
<b>Program Flash Memory Specifications</b>						
$E_{FL}^*$	<b>Flash memory cell endurance</b>	<b>10k</b>	—	—	<b>Erase/Write cycles</b>	$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$
$t_{FL\_RET}$	<b>Characteristic retention</b>	—	<b>40</b>	—	<b>Year</b>	$T_A = 55^{\circ}\text{C}$
$V_{FL\_UPDI}$	<b>V<sub>DD</sub> for Chip Erase operation</b>	$V_{BODLEVEL0}^{(1)}$	—	$V_{DDMAX}$	<b>V</b>	
$t_{FL\_PBC}$	Page Buffer Clear (PBC)	—	7	—	CLK <sub>CPU</sub> cycles	
$t_{FL\_CHER}$	<b>Chip Erase (CHER)</b>	—	<b>4</b>	—	<b>ms</b>	
$t_{FL\_WP}$	Page Write (WP)	—	2	—	ms	
$t_{FL\_ER}$	Page Erase (ER)	—	2	—	ms	
$t_{FL\_ERWP}$	Page Erase/Write (ERWP)	—	4	—	ms	
$t_{FL\_UPDI}$	Chip Erase with UPDI	—	30	—	ms	16 KB Flash
† Data in the “Typ.” column is at $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 3.0\text{V}$ unless otherwise specified. These parameters are not tested and are for design guidance only.						
* These parameters are characterized but not tested in production.						
<b>Note:</b>						
1. The Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON during Chip Erase. The erase attempt will fail if the supply voltage $V_{DD}$ is below $V_{BOD}$ for BODLEVEL0.						

## 4. Document Revision History

**Note:** The document revision is independent of the silicon revision.

### 4.1. Revision History

Doc. Rev.	Date	Comments
F	03/2026	<ul style="list-style-type: none"> <li>Document: <ul style="list-style-type: none"> <li>Editorial updates</li> </ul> </li> <li>Added new data sheet clarification: <ul style="list-style-type: none"> <li>EVSYS - Event System: <ul style="list-style-type: none"> <li><a href="#">User Channel MUX</a></li> </ul> </li> </ul> </li> </ul>
E	05/2024	<ul style="list-style-type: none"> <li>Document: <ul style="list-style-type: none"> <li>Editorial updates</li> </ul> </li> <li>Added new errata: <ul style="list-style-type: none"> <li>Device: <a href="#">Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values</a></li> <li>NVMCTRL: <a href="#">Wrong Reset Value of NVMCTRL.CTRLA Register</a></li> <li>USART: <a href="#">Receiver Non-Functional after Detection of Inconsistent Synchronization Field</a></li> </ul> </li> <li>Added new data sheet clarifications: <ul style="list-style-type: none"> <li>I/O Multiplexing and Considerations: <ul style="list-style-type: none"> <li><a href="#">I/O Multiplexing</a></li> </ul> </li> <li>Electrical Characteristics: <ul style="list-style-type: none"> <li><a href="#">I/O Pin Characteristics</a></li> <li><a href="#">SPI - Timing Characteristics</a></li> <li><a href="#">Programming Time</a></li> </ul> </li> </ul> </li> </ul>
D	01/2022	<ul style="list-style-type: none"> <li>Added erratum: <ul style="list-style-type: none"> <li>ADC: <a href="#">ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode</a></li> </ul> </li> <li>Updated erratum: <ul style="list-style-type: none"> <li>Device: <a href="#">IDD Power-Down Current Consumption</a></li> </ul> </li> <li>Updated data sheet clarification: <ul style="list-style-type: none"> <li>Removed <i>Fuses - Correct Factory Default Value for Reserved Fuse Bits is '1'</i></li> </ul> </li> </ul>
C	06/2021	<ul style="list-style-type: none"> <li>Updated errata: <ul style="list-style-type: none"> <li>Device: <a href="#">IDD Power-Down Current Consumption</a></li> <li>USART: <a href="#">Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode</a></li> </ul> </li> </ul>
B	12/2020	<ul style="list-style-type: none"> <li>Silicon revision D not released to production. Silicon revision E is the initial release: <ul style="list-style-type: none"> <li>Removed silicon revision D from <i>Silicon Issues Summary</i> and all <i>Affected Versions</i> tables</li> <li>Removed all errata only applicable to silicon revision D</li> </ul> </li> <li>Added errata: <ul style="list-style-type: none"> <li>Device: <a href="#">IDD Power-Down Current Consumption</a></li> <li>CCL: <a href="#">The CCL Must be Disabled to Change the Configuration of a Single LUT</a></li> <li>TCA: <a href="#">Restart Will Reset Counter Direction in NORMAL and FRQ Mode</a></li> <li>TCB: <a href="#">CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode</a></li> <li>USART: <a href="#">Open-Drain Mode Does Not Work When TXD is Configured as Output</a></li> </ul> </li> <li>Added data sheet clarification: <ul style="list-style-type: none"> <li>Fuses: <a href="#">Correct Factory Default Value for Reserved Fuse Bits is '1'</a></li> </ul> </li> </ul>

**Revision History (continued)**

Doc. Rev.	Date	Comments
A	07/2020	Initial document release

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ISBN: 979-8-3371-3007-1

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