Automotive Silicon Errata and Data Sheet Clarifications

ATtiny3216/3217 Automotive

www.microchip.com Product Pages: ATtiny3216, ATtiny3217

Introduction

The ATtiny3216/3217 Automotive devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002212), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny3216/3217 Automotive devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002212) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- Erratum is not applicable.

X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. C(1)
Device	Writing the OSCLOCK Fuse in FUSE.OSCCFG to ‘1’ Prevents Automatic Loading of Calibration Values	X
	Write Operation Lost if Consecutive Writes to Specific Address Spaces	X
	Frequency Drift of 16/20 MHz Oscillator at High Supply and High Temperature	X
ADC	ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
	One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
CCL	The CCL Must be Disabled to Change the Configuration of a Single LUT	X
NVMCTRL	Wrong Reset Value of NVMCTRL.CTRLA Register	X
TCA	Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	Minimum Event Duration Must Exceed the Selected Clock Period	X
	The TCA Restart Command Does Not Force a Restart of TCB	X
	CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X
TCD	Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X
	Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is ‘0’ or Dual Slope Mode is Used	X
USART	TXD Pin Override Not Released When Disabling the Transmitter	X
	Open-Drain Mode Does Not Work When TXD is Configured as Output	X
	Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X
	Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to ‘1’ Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to ‘`1`’ prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK to lock the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to ‘`1`’ when using the OSC20M oscillator as the Main Clock source.

Affected Silicon Revisions

Rev. C
X

2.2.2 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by an ST/STD instruction to address < 64 or SLPCTRL.CTRLA register will cause loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. C
X

2.2.3 Frequency Drift of 16/20 MHz Oscillator at High Supply and High Temperature

The frequency of the internal 16/20 MHz oscillator may drift out of the given specifications when the oscillator is disabled or stopped when VDD is above 4.5V and the temperature is above 85°C.

Work Around

Keep the oscillator running by setting the Run Standby (RUNSTDBY) bit to ‘`1`’ in the 16/20 MHz Oscillator Control A (CLKCTRL.OSC20MCTRLA) register and avoid using Power-Down sleep mode.

Affected Silicon Revisions

Rev. C
X

2.3 ADC - Analog-to-Digital Converter

2.3.1 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to ‘`1`’.

Work Around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to ‘`0`’ (50% duty cycle).

Affected Silicon Revisions

Rev. C
X

2.3.2 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around

Write ADCn.CTRLA.ENABLE to ‘`0`’ to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. C
X

2.4 CCL - Configurable Custom Logic

2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

The CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to ‘`0`’) to reconfigure a LUT. Writing ENABLE to ‘`0`’ will disable all the LUTs and affect the LUTs not under reconfiguration.

Work Around

None.

Affected Silicon Revisions

Rev. C
X

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the NVMCTRL.CTRLA reset value will not be ‘`0x00`’. Even reserved bits can be read as ‘`1`’ after Reset.

Work Around

Ignore the initial value.

Affected Silicon Revisions

Rev. C
X

2.6 TCA - Timer/Counter A

2.6.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '`0x0`' or '`0x1`'), a RESTART command or Restart event will reset the direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. C
X

2.7 TCB - Timer/Counter B

2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement*.

Work Around

Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. C
X

2.7.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. C
X

2.7.3 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '`0x7`'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. C
X

2.8 TCD - Timer/Counter D

2.8.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When configuring the TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '`0x2`') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '`0x0`' events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '`0x2`') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. C
X

2.8.2 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '`0x7`') does not work if compare value A is `0` (CMPASET in TCDn.CMPASET is '`0x0`') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '`0x3`').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from '`0`' and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '`0x3`').

Affected Silicon Revisions

Rev. C
X

2.9 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.9.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '`0`' while the USART receiver is disabled (RXEN in USART.CTRLB is '`0`')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '`0`'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '`1`') while disabling the transmitter (writing TXEN in USART.CTRLB to '`0`')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. C
X

2.9.2 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '`0`' when using Open-Drain mode.

Affected Silicon Revisions

Rev. C
X

2.9.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '`0`' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '`0`' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '`1`' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. C
X

2.9.4 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set.

The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud mode (GENAUTO), or LIN Constrained Auto-Baud mode (LINAUTO), and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '`0`' and then a '`1`' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. C
X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002212).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Memories

3.1.1 Fuses - Factory Default Values

A clarification has been made for the *Fuse Description* section concerning the fuse default values. The data sheet refers to these values as reset values when they should have been referred to as factory-programmed values. Also, they are given in both hexadecimal and binary values, which contradicts each other.

The following sentence has been added to each sub-section of the *Fuse Description* section.

The default value given in this fuse description is the factory-programmed value and should not be mistaken for the Reset value.

The table below lists the reset values given by the data sheet and the actual factory-programmed default values.

Fuse	Stated Reset Value in Data Sheet		Actual Factory Default on Device	
	Hexadecimal	Binary	Hexadecimal	Binary
WDTCFG	-	`` `b00000000 ``	**`0x00`**	**`` `b00000000 ``**
BODCFG	-	`` `b00000000 ``	**`0x00`**	**`` `b00000000 ``**
OSCCFG	-	`` `b0XXXXX10 ``	**`0x01`**	**`` `b00000001 ``**
TCD0CFG	-	`` `b00000000 ``	**`0x00`**	**`` `b00000000 ``**
SYSCFG0	`0xC4`	`` `b11X101X0 ``	**`0xF6`**	**`` `b11110110 ``**
SYSCFG1	-	`` `bXXXXX111 ``	**`0x07`**	**`` `b00000111 ``**
APPEND	-	`` `b00000000 ``	**`0x00`**	**`` `b00000000 ``**
BOOTEND	-	`` `b00000000 ``	**`0x00`**	**`` `b00000000 ``**
LOCKBIT	-	`` `b00000000 ``	**`0xC5`**	**`` `b11000101 ``**

3.2 SLPCTRL - Sleep Controller

3.2.1 Sleep Mode Activity Overview

A clarification has been made to Table 12-2 *Sleep Mode Activity Overview*, where the single table has been split into three separate tables for clarity. Functional changes are shown in **bold**.

Table 3-1. Sleep Mode Activity Overview for Peripherals

Peripheral	Active in Sleep Mode		
	Idle	Standby	Power-Down
CPU	-	-	-
RTC	X	X(1)	X(2)
WDT	X	X	X
BOD	X	X	X
EVSYS	**X**	**X**	**X**

Table 3-1. Sleep Mode Activity Overview for Peripherals (continued)

Peripheral	Active in Sleep Mode		
	Idle	Standby	Power-Down
CCL	X	X(1)	-
ACn			
ADCn/PTC			
TCBn			
All other peripherals	X	-	-

Notes:

1. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
2. PIT only.

Table 3-2. Sleep Mode Activity Overview for Clock Sources

Clock Source	Active in Sleep Mode		
	Idle	Standby	Power-Down
Main clock source	X	X(1)	-
RTC clock source	X	X(1)	X(2)
WDT oscillator	X	X	X
BOD oscillator(3)	**X**	**X**	**X**
CCL clock source	**X**	**X(1)**	-

Notes:

1. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
2. PIT only.
3. **The BOD oscillator runs only in Sampled mode.**

Table 3-3. Sleep Mode Wake-Up Sources

Wake-Up Sources	Active in Sleep Mode		
	Idle	Standby	Power-Down
PORT Pin Interrupt	X	X	X(1)
BOD VLM interrupt	**X**	**X**	**X**
RTC interrupts	X	X(2)	X(3)
TWIn Address Match interrupt	X	X	X
USARTn Start-of-Frame interrupt	**-**	**X**	-
TCBn interrupts	X	X(2)	**-**
ADCn/PTC interrupts	X	X(2)	-
ACn interrupts	**X**	**X(4)**	-
All other interrupts	X	-	-

Notes:

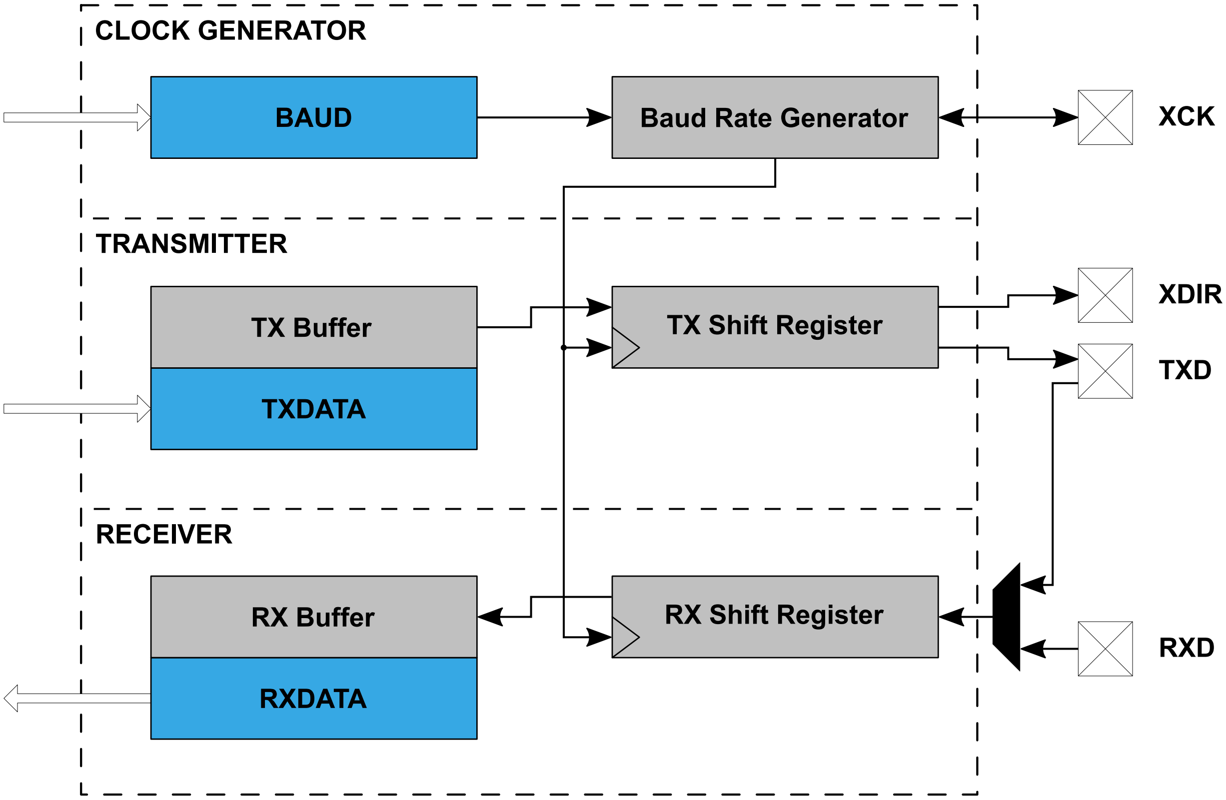
1. **The I/O pin must be configured according to *Asynchronous Sensing Pin Properties* in the PORT section.**
2. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
3. PIT only.
4. **When the RUNSTDBY bit is set, the AC will operate without updating its Status register or triggering interrupts. If another peripheral has requested CLK_PER, the AC will use the clock to update the Status register and trigger interrupts.**

3.3 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

3.3.1 TXDATA Buffer

The block diagram is missing that USART TX is double-buffered from *Figure 25-1. USART Block Diagram* in the data sheet. The figure below shows the added **TX Buffer**.

Figure 25-1. USART Block Diagram



The following text is changed in the *Overview* section:

The transmitter consists of a **two-level** write buffer.

The following text is changed in the *Data Transmission* section:

The data transmission is initiated by loading the **Transmit Data (USARTn.TXDATAL and USARTn.TXDATAH)** registers with the data to be sent. The data in the **Transmit Data registers are moved to the TX Buffer** once emptied and then to the Shift register once it is empty and ready to send a new frame.

3.4 SPI - Serial Peripheral Interface

3.4.1 SPI Clock

Clarifications regarding the SPI clock have been made in the *Operation - Slave Mode* and *Operation - Slave Mode - Buffer Mode* sections. Functional changes are shown in **bold**.

26.3.2.2 Slave Mode

In Slave mode, the SPI peripheral receives the SPI clock and Slave Select from a Master. Slave mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Slave mode, the control logic will sample the incoming signal on the SCK pin. ~~**To ensure correct sampling of this clock signal, the minimum low and high periods must each be longer than two peripheral clock cycles.**~~

26.3.2.2.2 Buffer Mode

To avoid data collisions, the SPI peripheral can be configured in Buffered mode by writing a '`1`' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register. In this mode, the SPI has additional interrupt flags and extra buffers. The extra buffers are shown in *Figure 26-1*. There are two different modes for the Buffer mode, selected with the Buffer mode Wait for Receive (BUFWR) bit. The two different modes are described below with timing diagrams.

Note: When operating as a slave in Buffered mode and the SPI clock is close to maximum frequency, the slave may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

3.5 ADC - Analog-to-Digital Converter

3.5.1 Temperature Sensor

A clarification has been made to remove documentation from the following ADC sections related to a temperature sensor (TEMPSENSE) as the ATtiny3216/3217 Automotive devices do not have any internal temperature sensor.

- **Features**
- **Block Diagram**
- **Temperature Measurement**

The affected ADC sections are listed below, with functional corrections shown in **bold**.

Features

- 10-Bit Resolution
- 0V to VDD Input Voltage Range
- Multiple Internal ADC Reference Voltages
- External Reference Input
- Free-Running and Single Conversion Mode
- Interrupt Available on Conversion Complete
- Optional Interrupt on Conversion Results
- **~~Temperature Sensor Input Channel~~**
- Optional Event-Triggered Conversion
- Window Comparator Function for Accurate Monitoring or Defined Thresholds
- Accumulation of up to 64 Samples per Conversion

Block Diagram

The analog input channel is selected by writing to the MUXPOS bits in the MUXPOS (ADCn.MUXPOS) register. Any ADC input pins, GND, internal Voltage Reference (VREF), **~~or temperature sensor,~~** can be selected as a single-ended input to the ADC. The ADC is enabled by writing a '`1`' to the ADC ENABLE bit in the Control A (ADCn.CTRLA) register. The voltage reference and input channel selections will not take effect before the ADC is enabled. The ADC does not consume power when the ENABLE bit in ADCn.CTRLA is '`0`'.

Temperature Measurement

The entire section has been removed.

3.5.2 Events

As the ADC cannot generate any events, a clarification has been made to the ADCs *Events* section. Functional changes are shown in **bold**.

An ADC conversion can be triggered automatically by an event input if the Start Event Input (STARTEI) bit in the Event Control (ADCn.EVCTRL) register is written to '`1`'.

~~**When a new result can be read from the Result (ADCn.RES) register, the ADC will generate a result ready event. The event is a pulse with a length of one clock period and handled by the Event System (EVSYS). The ADC result ready event is always generated when the ADC is enabled.**~~

See also the description of the Asynchronous User Channel n Input Selection in the Event System (EVSYS.ASYNCUSERn).

3.6 UPDI - Unified Program and Debug Interface

3.6.1 Chip Erase

As it refers to ERASE_FAILED, a status bit that does not exist in the UPDI, a clarification has been made to the *Chip Erase* section. Functional changes are shown in **bold**.

Follow these steps to issue a chip erase:

1. Enter the Chip Erase key by using the `KEY` instruction. See *Key Activation Signatures* for the CHIPERASE signature.
2. **Optional:** Read the Chip Erase (CHIPERASE) bit in the ASI Key Status (UPDI.ASI_KEY_STATUS) register to see that the key is successfully activated.
3. Write the signature to the Reset Request (RSTREQ) bit in the ASI Reset Request (UPDI.ASI_RESET_REQ) register, which will issue a System Reset.
4. Write `0x00` to the ASI Reset Request (UPDI.ASI_RESET_REQ) register to clear the System Reset.
5. Read the NVM Lock Status (LOCKSTATUS) bit from the ASI System Status (UPDI.ASI_SYS_STATUS) register.
6. The chip erase is done when the LOCKSTATUS bit is ‘`0`’. If the LOCKSTATUS bit is ‘`1`’, return to step 5.
7. ~~**Check the Chip Erase Key Failed (ERASE_FAILED) bit in the ASI System Status (UPDI.ASI_SYS_STATUS) register to verify if the chip erase was successful.**~~
8. ~~**If the ERASE_FAILED bit is ‘`0`’, the chip erase was successful.**~~

After a successful chip erase, the lock bits will be cleared, and the UPDI will have full access to the system. Until the lock bits are cleared, the UPDI cannot access the system bus, and only CS-space operations can be performed.

⚠ CAUTION During chip erase, the BOD is forced into ON state by writing to the Active (ACTIVE) bit field from the Control A (BOD.CTRLA) register and uses the BOD Level (LVL) bit field from the BOD Configuration (FUSE.BODCFG) fuse and the BOD Level (LVL) bit field from the Control B (BOD.CTRLB) register. If the supply voltage V_{DD} is below that threshold level, the device is unavailable until V_{DD} is increased adequately. See the *BOD* section for more details.

3.7 Electrical Characteristics

3.7.1 Power Consumption

A clarification of the power consumption in the Power-Down sleep mode has been made in *Table 37-5. Power Consumption in Power-Down, Standby and Reset Mode*. Functional change is shown in **bold**.

Table 37-5. Power Consumption in Power-Down, Standby and Reset Mode

Mode	Description	Condition		Typ. 25°C	Max. 25°C	Max. 85°C(1)	Max. 125°C	Unit
Standby	Standby power consumption	RTC running at 1.024 kHz from external XOSC32K (C_L = 7.5 pF)	V_{DD} = 3V	0.7	-	-	-	µA
		RTC running at 1.024 kHz from internal OSCULP32K	V_{DD} = 3V	0.7	3.0	6.0	8.0	µA
Power Down/ Standby	Power down/Standby power consumption is the same when all peripherals are stopped	All peripherals stopped	V_{DD} = 3V	0.1	**1.0**	5.0	7.0	µA
Reset	Reset power consumption	Reset line pulled down	V_{DD} = 3V	100	-	-	-	µA

Note:

1. These values are based on characterization and are not covered by production test limits.

3.7.2 I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor is made in *Table 37-16. I/O Pin Characteristics* in the *Electrical Characteristics* section. Functional change is shown in **bold**.

Table 37-16. I/O Pin Characteristics (T_A = [-40, 105]°C, V_{DD} = [2.7, 5.5]V Unless Otherwise Stated)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-voltage, except $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH}	Input high-voltage, except $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
I_{IH} / I_{IL}	I/O pin input leakage current, except $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 5.5V, pin high	-	< 0.05	-	µA
		V_{DD} = 5.5V, pin low	-	< 0.05	-	
V_{OL}	I/O pin drive strength	V_{DD} = 3.0V, I_{OL} = 7.5 mA	-	-	0.6	V
		V_{DD} = 5.0V, I_{OL} = 15 mA	-	-	1	
V_{OH}	I/O pin drive strength	V_{DD} = 3.0V, I_{OH} = 7.5 mA	2.4	-	-	V
		V_{DD} = 5.0V, I_{OH} = 15 mA	4	-	-	
I_{total}	Maximum combined I/O sink current per pin group(1)		-	-	100	mA
	Maximum combined I/O source current per pin group(1)		-	-	100	
V_{IL2}	Input low-voltage on $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH2}	Input high-voltage on $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
V_{OL2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 3.0V, I_{OL} = 0.25 mA	-	-	0.6	V
		V_{DD} = 5.0V, I_{OL} = 0.5 mA	-	-	1	
V_{OH2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 3.0V, I_{OH} = 0.25 mA	2.4	-	-	V
		V_{DD} = 5.0V, I_{OH} = 0.5 mA	4	-	-	
t_{RISE}	Rise time	V_{DD} = 3.0V, load = 20 pF	-	2.5	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.5	-	
t_{FALL}	Fall time	V_{DD} = 3.0V, load = 20 pF	-	2.0	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.3	-	
C_{PIN}	I/O pin capacitance except TOSC and TWI pins		-	3	-	pF
C_{PIN}	I/O pin capacitance on TOSC pins		-	5.5	-	pF
C_{PIN}	I/O pin capacitance on TWI pins		-	10	-	pF
R_P	Pull-up resistor		20	35	**60**	kΩ

Note:

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.

3.7.3 SPI - Timing Characteristics

A clarification regarding the SPI clock has been made in *Table 37-19. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

Table 37-19. SPI - Timing Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Master	-	-	10	MHz
t_{SCK}	SCK period	Master	100	-	-	ns
t_{SCKW}	SCK high/low width	Master	-	0.5 × t_{SCK}	-	ns
t_{SCKR}	SCK rise time	Master	-	2.7	-	ns
t_{SCKF}	SCK fall time	Master	-	2.7	-	ns
t_{MIS}	MISO setup to SCK	Master	-	10	-	ns
t_{MIH}	MISO hold after SCK	Master	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Master	-	0.5 × t_{SCK}	-	ns
t_{MOH}	MOSI hold after SCK	Master	-	1.0	-	ns
f_{SSCK}	Slave SCK clock frequency	Slave	-	-	**f_{CLK_PER} / 6**	MHz
t_{SSCK}	Slave SCK Period	Slave	**6 × t_{CLK_PER}**	-	-	ns
t_{SSCKW}	SCK high/low width	Slave	**3 × t_{CLK_PER}**	-	-	ns
t_{SSCKR}	SCK rise time	Slave	-	-	1600	ns
t_{SSCKF}	SCK fall time	Slave	-	-	1600	ns
t_{SIS}	MOSI setup to SCK	Slave	**0.0**	-	-	ns
t_{SIH}	MOSI hold after SCK	Slave	**3 × t_{CLK_PER}**	-	-	ns
t_{SSS}	SS setup to SCK	Slave	**-**	**t_{CLK_PER}**	-	ns
t_{SSH}	SS hold after SCK	Slave	**-**	**t_{CLK_PER}**	-	ns
t_{SOS}	MISO setup to SCK	Slave	-	8.0	-	ns
t_{SOH}	MISO hold after SCK	Slave	-	13	-	ns
t_{SOSS}	MISO setup after SS low	Slave	-	11	-	ns
t_{SOSH}	MISO hold after SS low	Slave	-	8.0	-	ns

3.7.4 Programming Time

A clarification of the *Programming Time* section has been made. *Table 37-37* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional change is shown in **bold**.

Table 37-37. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_{EE}*	**Data EEPROM byte endurance**	**100k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{EE_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
t_{EE_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{EE_EEER}	Full EEPROM Erase (EEER)	—	4	—	ms	
t_{EE_WP}	Page Write (WP)	—	2	—	ms	
t_{EE_ER}	Page Erase (ER)	—	2	—	ms	
t_{EE_ERWP}	Page Erase-Write (ERWP)	—	4	—	ms	
Program Flash Memory Specifications						
E_{FL}*	**Flash memory cell endurance**	**10k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{FL_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
V_{FL_UPDI}	**V_{DD} for Chip Erase operation**	**$V_{BODLEVEL0}$**(1)	**—**	**V_{DDMAX}**	**V**	
t_{FL_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{FL_CHER}	Chip Erase (CHER)	—	4	—	ms	
t_{FL_WP}	Page Write (WP)	—	2	—	ms	
t_{FL_ER}	Page Erase (ER)	—	2	—	ms	
t_{FL_ERWP}	Page Erase/Write (ERWP)	—	4	—	ms	
t_{FL_UPDI}	**Chip Erase with UPDI**	**—**	**280**	**—**	**ms**	

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Note:

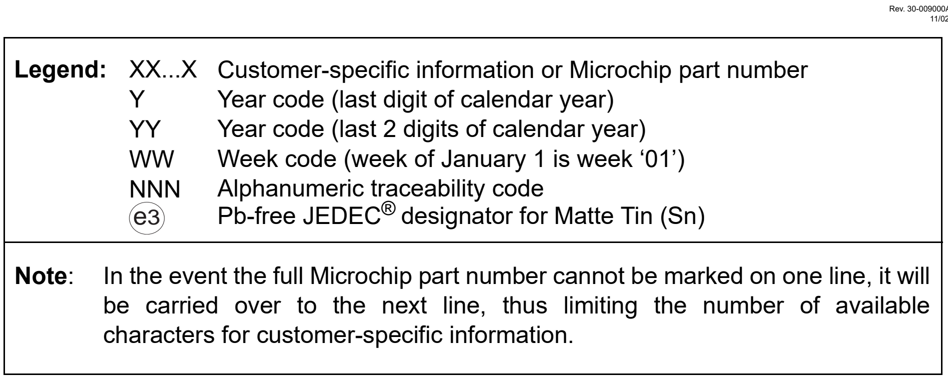
1. **During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.**

3.8 Package Drawings

3.8.1 Package Marking Information

Package marking information is missing in the data sheet. This section contains all package marking information for ATtiny3216/3217 Automotive devices.

Figure 3-1. Package Marking Information



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Legend:		
	XX...X	Customer-specific information or Microchip part number
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Figure 3-2. 20-Pin SOIC

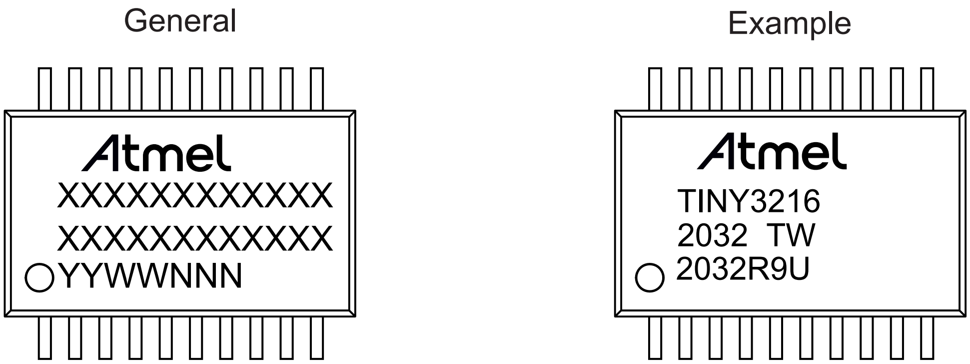
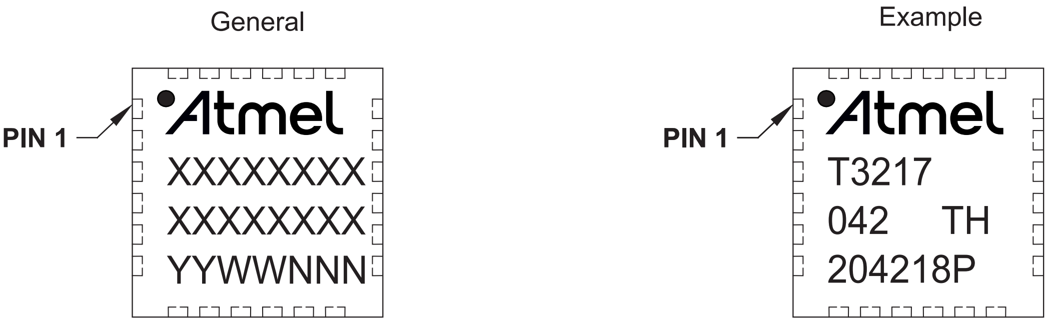


Figure 3-3. 24-Pin VQFN - Wettable Flanks



4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	03/2025	• Document: Editorial updates • Added errata: – Device: • Write Operation Lost if Consecutive Writes to Specific Address Spaces • Frequency Drift of 16/20 MHz Oscillator at High Supply and High Temperature • Added data sheet clarifications: – ADC: • Temperature Sensor • Events – SPI: SPI Clock – UPDI: Chip Erase – Electrical Characteristics: • Power Consumption • I/O Pin Characteristics • SPI - Timing Characteristics • Programming Time
C	06/2022	• Updated errata: – Device - Writing the OSCLOCK Fuse in FUSE.OSCCFG to ‘1’ Prevents Automatic Loading of Calibration Values – USART - Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode • Added errata – NVMCTRL - Wrong Reset Value of NVMCTRL.CTRLA Register – TCD - Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is ‘0’ or Dual Slope Mode is Used – USART - Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Added data sheet clarifications: – Memories - Fuses - Factory Default Values – SLPCTRL - Sleep Mode Activity Overview

Revision History (continued)

Doc. Rev.	Date	Comments
B	12/2020	• Added errata – CCL - The CCL Must be Disabled to Change the Configuration of a Single LUT – TCA - Restart Will Reset Counter Direction in NORMAL and FRQ Mode – TCB - CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode – TCD - Asynchronous Input Events Not Working When TCD Counter Prescaler is Used – USART - Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode • Added data sheet clarifications – Package marking information – USART TX is double-buffered
A	05/2020	Initial document release

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