dsPIC33CK64MP105

dsPIC33CK64MP105 Family
Silicon Errata and Data Sheet Clarification

The dsPIC33CK64MP105 family devices that you have received conform functionally to the current Device Data Sheet (DS70005363**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK64MP105 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK64MP105 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision			
		A0	A2	A4	A5
dsPIC33CK32MP102	0x8E00	0x0000	0x0002	0x0004	0x0005
dsPIC33CK32MP103	0x8E01				
dsPIC33CK32MP105	0x8E02				
dsPIC33CK64MP102	0x8E10				
dsPIC33CK64MP103	0x8E11				
dsPIC33CK64MP105	0x8E12				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions			
				A0	A2	A4	A5
I2C	Interrupt	1.	In Client mode, an incorrect interrupt is generated when DHEN = 1.	X	X	X	X
I2C	Idle	2.	Module SFR registers are reset in Idle mode.	X	X	X	X
I2C	SMBus 3.0	3.	When Configuration bit SMB3EN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X			
Oscillator	XT, HS	4.	Removed.				
PWM	Dead Time	5.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X	X	X	X
UART	Frame Error	6.	FERR bit will not get set if a Stop bit is received.	X	X	X	X
UART	Sleep	7.	SLPEN needs to be set when waking from Sleep with a UART reception.	X	X	X	X
UART	Address Detect	8.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X	X	X	X
UART	IrDA®	9.	When the UART is operating in IrDA mode, the received data may be corrupted.	X	X	X	X
I/O	POR	10.	Spike on I/O at POR.	X			
ICSP™ Flash Write Inhibit	Flash Write Inhibit	11.	Flash memory cannot be protected against reprogramming.	X			
CPU	FLIM Instruction	12.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X	X	X	X
CPU	DIV.SD Instruction	13.	Overflow bit is not getting set when an overflow occurs.	X	X	X	X
CPU	MAXAB/MINAB/ MINZAB Instructions	14.	MAXAB, MINAB and MINZAB do not work for different sign operands.	X	X	X	X
CPU	Byte Mode Instructions	15.	Upper byte of the destination register may not be persistent.	X	X	X	X
DMA	ADC Triggers	16.	DMA is triggered continuously from ADC.	X			
I2C	I^2C	17.	All instances of I^2C may exhibit errors and should not be used.	X	X		
Oscillator	VCO and AVCO Dividers	18.	Main and auxiliary PLL external VCO dividers can fail to output the clock.	X	X		
Reset	BOR	19.	BOR may stop functioning when VDD drops in the window between the BOR level and BOR-25 mV.	X	X		
Reset	BOR	20.	BOR may periodically cause device resets when the VDD is in a window between the BOR level and BOR-25 mV.	X	X	X	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Client interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

2. Module: I²C

In Client mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

3. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit SMB3EN (FDEVOPT[10]), the Voltage Input High (V_{IH}) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X							

4. Module: Oscillator

This errata is no longer applicable to any silicon revisions of this product. See **Section 2.5 External Oscillator Pins** in the current device data sheet for guidance on oscillator design to avoid start-up related issues.

5. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

6. Module: UART

When UART is operating with STSEL[1:0] = 2, (two Stop bits sent, two checked at receive) and STPMD = 0, the FERR bit will not get set if a Stop bit is received.

Work around

Use STPSEL = 3 instead of STSEL = 2. When operating with STSEL = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

7. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

8. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

9. Module: UART

When the UART is operating in IrDA® mode, the received data may be corrupted.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

10. Module: I/O

At device power-up, the I/O pins may drive a pulse up to 0.8V for a duration of up to 100 µSec.

Work around

It is recommended to ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® DSC to avoid the issue.

Behavior is specific to each part and not affected by aging.

Affected Silicon Revisions

A0	A2	A4	A5				
X							

11. Module: ICSP™ Flash Write Inhibit

The ICSP Write Inhibit feature does not prevent ICSP Flash erase and program operations, even if the lock values are written.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X							

12. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

13. Module: CPU

When using the Signed 32-by-16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the div.sd instruction.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

14. Module: CPU

When operating on signed operands of different sign values, the output for MAXAB, MINAB and MINZAB instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

15. Module: CPU

When using Byte mode instructions, the upper byte of the destination register may not be persistent.

Work around

None.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

16. Module: DMA

The DMA receives multiple continuous triggers from ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A0	A2	A4	A5				
X							

17. Module: I^2C

All instances of I^2C/SMBus may exhibit errors and should not be used. When operating I^2C/SMBus in a noisy environment, the I^2C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I^2C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I^2C pins. Both Host and Client I^2C/SMBus modes may exhibit this issue.

Work around

If I^2C is required, use a software I^2C implementation. An example I^2C software library is available from Microchip: www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

A0	A2	A4	A5				
X	X						

18. Module: Oscillator

At PLL start-up, the main and auxiliary PLL VCO dividers may occasionally halt and not provide a clock output. The VCO and AVCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, UART, etc. VCO and AVCO dividers, FVCO/2, FVCO/3, FVCO/4, FVCODIV, AFVCO/2, AFVCO/3, AFVCO/4 and AFVCODIV outputs, are affected.

Work around

1. Use another clock source, such as the FOSC, PLL or APLL output (FPLLO and AFPLLO) instead of the VCO or AVCO dividers.
2. If the application requires the VCO or AVCO divider, test this clock source. System resources, such as a timer, I/O pin state or interrupts can be used to detect and verify peripheral activity for presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, MCLR or POR).

Affected Silicon Revisions

A0	A2	A4	A5				
X	X						

19. Module: Reset

After start-up, if VDD decreases to a value between VBOR-25 mV and VBOR, the BOR may be unintentionally disabled. The device may incorrectly operate down to 2.0V. However, while operating at a VDD between 3-3.6V, the device will operate as expected. The VBOR specification is listed in the **"Electrical Characteristics"** section in the device data sheet.

Work around

An external voltage monitor IC may be used as a work around. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X						

20. Module: Reset

If V_{DD} is between VBOR-25 mV and V_{BOR}, a BOR Reset may repeatedly occur. However, while operating at a V_{DD} between 3-3.6V, the device will operate as expected. The V_{BOR} specification is listed in the **"Electrical Characteristics"** section in the device data sheet.

Work around

An external voltage monitor IC may be used as a work around. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A0	A2	A4	A5				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005363**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Pin Diagrams

Shading has been added to RB4 in all pin diagrams to indicate 5V tolerance.

2. Module: Memory Organization

Table 4-11: SFR BLOCK D00h has been updated to reflect the existence of RPOR17, RPOR18, and RPOR19 (see example below).

TABLE 4-11: SFR BLOCK D00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
PPS			RPINR21	D2E	1111111111111111	RPOR4	D88	--000000--000000
RPCON	D00	----0----------	RPINR22	D30	1111111111111111	RPOR5	D8A	--000000--000000
RPINR0	D04	11111111--------	RPINR23	D32	--------11111111	RPOR6	D8C	--000000--000000
RPINR1	D06	1111111111111111	RPINR26	D38	--------11111111	RPOR7	D8E	--000000--000000
RPINR2	D08	11111111--------	RPINR27	D3A	1111111111111111	RPOR8	D90	--000000--000000
RPINR3	D0A	1111111111111111	RPINR29	D3E	1111111111111111	RPOR9	D92	--000000--000000
RPINR4	D0C	1111111111111111	RPINR30	D40	--------11111111	RPOR10	D94	--000000--000000
RPINR5	D0E	1111111111111111	RPINR32	D44	11111111--------	RPOR11	D96	--000000--000000
RPINR6	D10	1111111111111111	RPINR33	D46	--------11111111	RPOR12	D98	--000000--000000
RPINR7	D12	1111111111111111	RPINR37	D4E	1111111111111111	RPOR13	D9A	--000000--000000
RPINR8	D14	1111111111111111	RPINR38	D50	--------11111111	RPOR14	D9C	--000000--000000
RPINR9	D16	1111111111111111	RPINR42	D58	1111111111111111	RPOR15	D9E	--000000--000000
RPINR10	D18	1111111111111111	RPINR43	D5A	1111111111111111	RPOR16	DA0	--000000--000000
RPINR11	D1A	1111111111111111	RPINR44	D5C	1111111111111111	RPOR17	DA2	--000000--000000
RPINR12	D1C	1111111111111111	RPINR45	D5E	1111111111111111	RPOR18	DA4	--000000--000000
RPINR13	D1E	1111111111111111	RPINR46	D60	1111111111111111	RPOR19	DA6	--000000--000000
RPINR14	D20	1111111111111111	RPINR47	D62	1111111111111111	RPOR20	DA8	--000000--000000
RPINR15	D22	1111111111111111	RPINR48	D64	1111111111111111	RPOR21	DAA	--000000--000000
RPINR16	D24	1111111111111111	RPINR49	D66	--------11111111	RPOR22	DAC	--000000--000000
RPINR17	D26	1111111111111111	RPOR0	D80	--000000--000000	RPOR23	DAE	--000000--000000
RPINR18	D28	1111111111111111	RPOR1	D82	--000000--000000	RPOR24	DB0	--000000--000000
RPINR19	D2A	1111111111111111	RPOR2	D84	--000000--000000	RPOR25	DB2	--000000--000000
RPINR20	D2C	1111111111111111	RPOR3	D86	--000000--000000	RPOR26	DB4	--000000--000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address values are in hexadecimal. Reset values are in binary.

3. Module: Flash Program Memory

The WRERR bit in Register 5-1: NVMCON has been updated to show an access attribute of R-C/0 (read/clear-able).

4. Module: Interrupt Controller

The VHOLD bit in Register 7-7: INTTREG has been updated to show an access attribute of R/W-0 (read/write).

5. Module: Oscillator with High-Frequency PLL

Section 9.6: “Low-Power RC (LPRC) Oscillator text has been updated as follows:

The dsPIC33CK64MP105 family devices contain one instance of the Low-Power RC (LPRC) Oscillator, which provides a nominal clock frequency of 32 kHz and serves as the clock source for the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FCSM) circuits in the clock subsystem. The LPRC Oscillator is shut off in Sleep mode.

- The LPRC Oscillator remains enabled under the following conditions:
- The FCSM is enabled
- The WDT is enabled
- The LPRC Oscillator is selected as the system clock

6. Module: Oscillator with High-Frequency PLL

The CF bit in Register 9-1: OSCCON has been updated to show an access attribute of R-0 (read-only). Note 3 has been updated to: “This bit should only be cleared in software.”

7. Module: High-Resolution PWM with Fine Edge Placement

Register 11-12: PGxCONL has been updated to show bit 14, FRZ.

REGISTER 11-12: PGxCONL: PWM GENERATOR x CONTROL REGISTER LOW

R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ON	FRZ	—	—	—	TRGCNT2	TRGCNT1	TRGCNT0
bit 15							bit 8

bit 14 **FRZ:** Freeze bit
1 = PGx stops operation in Debug mode
0 = PGx continues operation in Debug mode

8. Module: High-Speed, 12-Bit Analog-to-Digital Converter (ADC)

The CNVRTCH and SWCTRG bits in Register 12-5: ADCON3L have been updated to show an access attribute of R/W/HC-0 (read/write by software; cleared by hardware).

9. Module: High-Speed Analog Comparator with Slope Compensation DAC

The CMPSTAT bit in Register 13-5: DACxCONL has been updated to show an access attribute of R-0 (read-only).

10. Module: Quadrature Encode Interface (QEI)

The bit description for the bitfield INTDIV[2:0] in Register 14-1: QEIxCON has been updated as follows:

INTDIV[2:0]: Timer Input Clock Prescale Select bits
(interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)
111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

Option 0b111 has been updated from 1:256 to 1:128.

11. Module: Universal Asynchronous Receiver Transmitter (UART)

References to “Direct Matrix Architecture (DMX)” have been updated to “Digital Multiplex (DMX)”.

12. Module: Peripheral Trigger Generator

The bit description for PTGSWT in Register 22-1: PTGCST has been updated as follows:

bit 10 **PTGSWT:** PTG Software Trigger bit(2)
1 = If the PTG state machine is executing the “Wait for software trigger” Step command (OPTION[3:0] = 1010 or 1011), the command will complete and execution will continue
0 = No action other than to clear the bit

13. Module: Electrical Characteristics

In Table 31-18: Program Flash Memory Specifications, the maximum ratings for D138a TWW and D138b TRW have been updated to 52.3 µs and 2.2 ms, respectively.

14. Module: Electrical Characteristics

In Table 31-32: UARTx Module Timing Requirements, the maximum rating for UA11 FBAUD has been updated from 25 Mbps to 40 Mbps.

15. Module: Electrical Characteristics

In Table 31-35: DAC Module Specifications, the units for DA06 EG have been updated from % to LSB.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (1/2019)

Initial version of this document; issued for revision A0.

Rev B Document (2/2019)

Updated device data sheet revision from B to C.

Rev C Document (3/2019)

Added silicon issue 16 (DMA).

Rev D Document (1/2020)

Added silicon issue 17 (I2C).

Rev E Document (6/2020)

Added silicon issue 18 (Oscillator).

Removed silicon issue 4 (Oscillator) since it is no longer applicable.

Rev F Document (7/2020)

Added silicon revision A2.

Rev G Document (2/2020)

Added silicon issues 19 (Reset) and 20 (Reset).

Added A2 to affected silicon revisions in silicon issue 17 (I2C).

The I^2C standard uses the terminology *"Master"* and *"Slave."* The equivalent Microchip terminology used in this document is *"Host"* and "*Client*", respectively.

Rev H Document (6/2022)

Added silicon revision A4.

Updated silicon issues 19 (Reset) and 20 (Reset).

Rev J Document (8/2025)

Added silicon revision A5.

Added data sheet clarifications 1-15.

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