

PIC16F18154/55/74/75 Silicon Errata and Data Sheet

Clarifications

PIC16F18154/55/74/75



The PIC16F18154/55/74/75 devices that you have received conform functionally to the current device data sheet (DS40002491B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18154/55/74/75 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID			
		B0	B1	B2	D1
PIC16F18154	0x310A	0xA040	0xA041	0xA042	0xA0C1
PIC16F18155	0x310F	0xA040	0xA041	0xA042	0xA0C1
PIC16F18174	0x310B	0xA040	0xA041	0xA042	0xA0C1
PIC16F18175	0x3110	0xA040	0xA041	0xA042	0xA0C1



Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				B0	B1	B2	D1
Analog-to-Digital Converter with Computation (ADCC)	Acquisition Time	1.1.1	Acquisition time cannot be changed through either the ADACQ or the ADPRE registers	X			
Analog-to-Digital Converter with Computation (ADCC)	ADC Voltage Reference	1.1.2	RA2 is not working as V_{REF^-} in Single-Ended mode	X	X		
Digital-to-Analog Converter (DAC)	DAC Auto Enable	1.2.1	Mid-band voltage spike at code 128 may occur when $DACAUTOEN$ is enabled and the application is incrementing the $DACxDATL$ register from 127 to 129	X			
Fixed Voltage Reference (FVR)	ADC Buffer	1.3.1	Power-down current (I_{PD}) for the ADC FVR Buffer may be higher than the current data sheet limits		X		
Note: Only those issues indicated in the last column apply to the current silicon revision.							

1. Silicon Errata Issues

NOTICE

This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Acquisition Time Cannot Be Changed through Either the ADACQ or the ADPRE Registers

ADC acquisition (sample) time cannot be modified by writing to either the ADPRE or ADACQ registers. Writes to the ADPRE or ADACQ registers will correctly delay the next conversion but will have no affect on increasing the actual sample time of the current conversion. For example, if the ADCRC is used as the clock source, the sample time will be nominally 3.33 μ s, regardless of the values in either of the ADACQ or ADPRE registers.

Work around

There is essentially no work around for increasing the sample times via the ADPRE or ADACQ registers; however, there are various work arounds and/or techniques that can be implemented to acquire a more accurate ADC measurement.

- If the ADC is using the F_{osc} , reducing the clock speed at the time of measurement will increase the overall sampling time.
 - Use the NOSC/NDIV bits of OSCCON1 to reduce the oscillator speed
 - Adjust the ADCLK divider value to reduce the oscillator speed
 - Switch the ADC clock to the ADCRC
- The source input impedance (R_s) directly effects the amount of time it takes to charge the C_{hold} capacitor. Reducing the input impedance to a minimum will help reduce the sample time needed for the ADC measurement.

Affected Silicon Revisions

B0	B1	B2	D1				
X							

1.1.2 RA2 Is Not Working as V_{REF^-} in Single-Ended Mode

V_{REF^-} cannot be connected externally to the V_{REF^-} pin (RA2) in Single-Ended mode (IC = 0). V_{REF^-} can only be connected to the external V_{REF^-} pin in Differential mode (IC = 1).

Work around

No work around available for Single-Ended mode.

Affected Silicon Revisions

B0	B1	B2	D1				
X	X						

1.2 Module: Digital-to-Analog Converter (DAC)

1.2.1 Mid-band Voltage Spike at Code 128 May Occur When DACAUTOEN Is Enabled and the Application Is Incrementing the DACxDATL Register from 127 to 129

When the DACAUTOEN bit is enabled, a voltage glitch on the DACxOUT pin may occur at code 128 when the application is incrementing the DACxDATL register from 127 to 129 and the alternate

DACxOUT pin is either tied to GND or V_{DD} . If the alternate pin is tied to V_{DD} , the glitch will be positive; if the pin is tied to GND, the glitch will be negative.

Work around

None.

Affected Silicon Revisions

B0	B1	B2	D1				
X							

1.3 Module: Fixed Voltage Reference (FVR)

1.3.1 Power-down Current (I_{PD}) for the ADC FVR Buffer May Be Higher than the Current Data Sheet Limits

When using the ADC FVR Buffer as an ADC reference, the I_{PD} current may be higher than the current data sheet limits. The parameters for **B1** silicon are as follows:

Param. No.	Sym.	Device Characteristics	Min.	Typ.t	Max. +85°C	Max. +125°C	Units	Conditions	
								V_{DD}	Note
D204	$I_{PD_FVR_BUF1}$	FVR Buffer 1 (ADC)	—	171	420	485	μA	3.0V	

Work around

None.

Affected Silicon Revisions

B0	B1	B2	D1				
	X						

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002491B):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
D	04/2024	Added new silicon revision D1.
C	02/2024	Added new silicon revision B2.
B	08/2023	Added new silicon revision B1; added errata issue 1.3.1.
A	05/2023	Initial release of this document.

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