Silicon Errata and Data Sheet Clarifications

ATtiny3224/3226/3227

The ATtiny3224/3226/3227 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002345), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny3224/3226/3227 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002345) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

-	Erratum is not applicable.
X	Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
Device	2.2.1. IDD Power-Down Current Consumption	X
	2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
	2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X
ADC	2.3.1. Low Latency Mode Must Be Set Before Changing ADC Configuration	X
	2.3.2. The PGA Initialization Delay Does Not Work Outside Low Latency Mode	X
	2.3.3. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode	X
CCL	2.4.1. The CCL Must be Disabled to Change the Configuration of a Single LUT	X
CRCSCAN	2.5.1. Running CRC Scan on Part of The Flash is Non-Functional	X
NVMCTRL	2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X
TCA	2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.8.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.9.1. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X
	2.9.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 IDD Power-Down Current Consumption

For material with date code 2045 (manufactured in the year 2020, week 45) or older, the IDD power-down leakage can exceed the targeted maximum value of 1.5 µA.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when the OSC20M oscillator is used as the Main Clock source.

Affected Silicon Revisions

Rev. A
X

2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A
X

2.3 ADC - Analog-to-Digital Converter

2.3.1 Low Latency Mode Must Be Set Before Changing ADC Configuration

If using the low latency mode in the ADC, the initialization delay does not start for settings configured before the Low Latency (LOWLAT) bit in the Control A (ADCn.CTRLA) register. This may result in a conversion starting before the initialization time has ended and give a corrupt result.

Work Around

Enable the low latency bit (LOWLAT) in the Control A (ADCn.CTRLA) register at the start of ADC initialization before configuring any other register in the ADC.

Affected Silicon Revisions

Rev. A
X

2.3.2 The PGA Initialization Delay Does Not Work Outside Low Latency Mode

The initialization delay for the PGA does not start when the LOWLAT bit is '0'. This may cause a corrupt conversion when the PGA is the module with the slowest initialization time. When using the internal references, this is not an issue because of a slower initialization delay.

Work Around

Set the ADC in low latency mode by setting the Low Latency (LOWLAT) bit in the Control A (CTRLA) register to '1'.

Affected Silicon Revisions

Rev. A
X

2.3.3 ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode

If the Low Latency bit (LOWLAT in ADCn.CTRLA) is '1', the ADC stays active when the device enters Power-Down or Standby sleep modes. If the Free-Running bit (FREERUN in ADCn.CTRLF) is '1', the ADC continues to run in Standby sleep mode even if the Run in Standby bit (RUNSTDBY in ADCn.CTRLA) is '0'. In both cases, the interrupts will not trigger when the device enters Power-Down or Standby sleep mode.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.4 CCL - Configurable Custom Logic

2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. A
X

2.5 CRCSCAN - Cyclic Redundancy Check Memory Scan

2.5.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from 0x00
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from 0x00
- Running CRC scan on the entire Flash works

Work Around
None

Affected Silicon Revisions

Rev. A
X

2.6 NVMCTRL - Nonvolatile Memory Controller

2.6.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the reset value of NVMCTRL.CTRLA will not be '0'. Even reserved bits can be read as '1' after Reset.

Work Around
Ignore the initial value.

Affected Silicon Revisions

Rev. A
X

2.7 TCA - 16-Bit Timer/Counter Type A

2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A
X

2.8 TCB - 16-Bit Timer/Counter Type B

2.8.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A
X

2.9 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.9.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A
X

2.9.2 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A
X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002345).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 I/O Multiplexing and Considerations

3.1.1 I/O Multiplexing

A clarification is made in *Table 3-1. PORT Function Multiplexing*. The "footnote 4" is also valid for LUT0-OUT on pin PB4. Functional change is shown in **bold**.

Table 3-1. PORT Function Multiplexing

VQFN 24-pin	VQFN 20-pin	SSOP/SOIC 20-pin	TSSOP/SOIC 14-pin	Pin Name (1,2)	Other/ Special	ADC0(3)	AC0	USART0	USART1	SPI0	TWI0	TCA0	TCBn	CCL
23	19	16	10	PA0	$\overline{\text{RESET}}$ UPDI									LUT0-IN0
24	20	17	11	PA1		AIN1		TXD(4)	TXD	MOSI				LUT0-IN1
1	1	18	12	PA2	EVOUTA	AIN2		RxD(4)	RXD	MISO				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3		XCK(4)	XCK	SCK		WO3	1,WO	
3	3	20	14	GND										
4	4	1	1	VDD										
5	5	2	2	PA4		AIN4		XDIR(4)	XDIR	$\overline{\text{SS}}$		WO4		LUT0-OUT
6	6	3	3	PA5	VREFA	AIN5	OUT					WO5	0,WO	LUT3-OUT(4)
7	7	4	4	PA6		AIN6	AINN0							
8	8	5	5	PA7	EVOUTA(4)	AIN7	AINP0							LUT1-OUT
9				PB7	EVOUTB(4)									
10				PB6			AINP3							LUT2-OUT(4)
11	9	6		PB5	CLKOUT	AIN8	AINP1					WO2(4)		
12	10	7		PB4	$\overline{\text{RESET}}$(4)	AIN9	AINN1					WO1(4)		LUT0-OUT**(4)**
13	11	8	6	PB3	TOSC1			RxD				WO0(4)		LUT2-OUT
14	12	9	7	PB2	TOSC2 EVOUTB			TxD				WO2		LUT2-IN2
15	13	10	8	PB1		AIN10	AINP2	XCK			SDA	WO1		LUT2-IN1
16	14	11	9	PB0		AIN11	AINN2	XDIR			SCL	WO0		LUT2-IN0
17	15	12		PC0		AIN12			XCK(4)	SCK(4)			0,WO(4)	LUT3-IN0
18	16	13		PC1		AIN13			RxD(4)	MISO(4)				LUT1-OUT(4) LUT3-IN1
19	17	14		PC2	EVOUTC	AIN14			TxD(4)	MOSI(4)				LUT3-IN2
20	18	15		PC3		AIN15			XDIR(4)	$\overline{\text{SS}}$(4)		WO3(4)		LUT1-IN0
21				PC4								WO4(4)	1,WO(4)	LUT1-IN1 LUT3-OUT
22				PC5								WO5(4)		LUT1-IN2

Notes:

1. Pin names are P*xn* type, with *x*being the PORT instance (A, B) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*.
2. All pins can be used for external interrupt where pins P*x*2 and P*x*6 of each port have full asynchronous detection. All pins can be used as event input.
3. AIN[15:8] can not be used as negative ADC input for differential measurements.
4. Alternative pin location. For selecting an alternative pin location, refer to the PORTMUX section.

3.2 Electrical Characteristics

3.2.1 I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor is made in *Table 33-16 in the Electrical Characteristics* section. Functional change is shown in **bold**.

Operating conditions:

- T_A = [-40, 125]°C
- V_{DD} = [1.8, 5.5]V, unless otherwise specified

Table 33-16. I/O Pin Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-voltage, except $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH}	Input high-voltage, except $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
I_{IH} / I_{IL}	I/O pin Input leakage current, except $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 5.5V, Pin high	-	< 0.05	-	µA
		V_{DD} = 5.5V, Pin low	-	< 0.05	-	
V_{OL}	I/O pin drive strength	V_{DD} = 1.8V, I_{OL} = 1.5 mA	-	-	0.36	V
		V_{DD} = 3.0V, I_{OL} = 7.5 mA	-	-	0.6	
		V_{DD} = 5.0V, I_{OL} = 15 mA	-	-	1	
V_{OH}	I/O pin drive strength	V_{DD} = 1.8V, I_{OH} = 1.5 mA	1.44	-	-	V
		V_{DD} = 3.0V, I_{OH} = 7.5 mA	2.4	-	-	
		V_{DD} = 5.0V, I_{OH} = 15 mA	4	-	-	
I_{total}	Maximum combined I/O sink current per pin group(1)		-	-	100	mA
	Maximum combined I/O source current per pin group(1)		-	-	100	
V_{IL2}	Input low-voltage on $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH2}	Input high-voltage on $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
V_{OL2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 1.8V, I_{OL} = 0.1 mA	-	-	0.36	V
		V_{DD} = 3.0V, I_{OL} = 0.25 mA	-	-	0.6	
		V_{DD} = 5.0V, I_{OL} = 0.5 mA	-	-	1	
V_{OH2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 1.8V, I_{OH} = 0.1 mA	1.44	-	-	V
		V_{DD} = 3.0V, I_{OH} = 0.25 mA	2.4	-	-	
		V_{DD} = 5.0V, I_{OH} = 0.5 mA	4	-	-	
t_{RISE}	Rise time	V_{DD} = 3.0V, load = 20 pF	-	2.5	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.5	-	
t_{FALL}	Fall time	V_{DD} = 3.0V, load = 20 pF	-	2.0	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.3	-	
C_{PIN}	I/O pin capacitance, unless otherwise specified		-	4	-	pF
C_{PIN_TWI}	I/O pin capacitance on TWI pins(2)		-	12	-	pF
C_{PIN_AC}	I/O pin capacitance on AC pins(2)	PB0 and PB1	-	12	-	pF
		other AC pins	-	4	-	
C_{PIN_VREFA}	I/O pin capacitance on ADC VREFA pin		-	14	-	pF
R_P	Pull-up resistor		20	35	**60**	kΩ

Notes:

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.
2. This capacitance is valid for pins with this functionality, even when that functionality is unused.

3.2.2 SPI - Timing Characteristics

A clarification regarding the SPI clock is made in *Table 33-18. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

Table 33-18. SPI - Timing Characteristics(1)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Host	-	-	10	MHz
t_{SCK}	SCK period	Host	100	-	-	ns
t_{SCKW}	SCK high/low width	Host	-	0.5 × t_{SCK}	-	ns
t_{SCKR}	SCK rise time	Host	-	2.7	-	ns
t_{SCKF}	SCK fall time	Host	-	2.7	-	ns
t_{MIS}	MISO setup to SCK	Host	-	10	-	ns
t_{MIH}	MISO hold after SCK	Host	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Host	-	0.5 × t_{SCK}	-	ns
t_{MOH}	MOSI hold after SCK	Host	-	1.0	-	ns
f_{SSCK}	Client SCK clock frequency	Client	-	-	5	MHz
t_{SSCK}	Client SCK Period	Client	**6 × t_{CLK_PER}**	-	-	ns
t_{SSCKW}	SCK high/low width	Client	**3 × t_{CLK_PER}**	-	-	ns
t_{SSCKR}	SCK rise time	Client	-	-	1600	ns
t_{SSCKF}	SCK fall time	Client	-	-	1600	ns
t_{SIS}	MOSI setup to SCK	Client	**0.0**	-	-	ns
t_{SIH}	MOSI hold after SCK	Client	**3 x t_{CLK_PER}**	-	-	ns
t_{SSS}	SS setup to SCK	Client	**-**	**t_{CLK_PER}**	-	ns
t_{SSH}	SS hold after SCK	Client	**-**	**t_{CLK_PER}**	-	ns
t_{SOS}	MISO setup to SCK	Client	-	8.0	-	ns
t_{SOH}	MISO hold after SCK	Client	-	13	-	ns
t_{SOSS}	MISO setup after SS low	Client	-	11	-	ns
t_{SOSH}	MISO hold after SS low	Client	-	8.0	-	ns

Note:

1. These parameters are for design guidance only and are not production-tested.

3.2.3 Programming Time

A clarification of the *Programming Time* section is made. *Table 33-34* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional changes are shown in **bold**.

Table 33-34. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_{EE}*	**Data EEPROM byte endurance**	**100k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{EE_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
t_{EE_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{EE_EEER}	Full EEPROM Erase (EEER)	—	4	—	ms	
t_{EE_WP}	Page Write (WP)	—	2	—	ms	
t_{EE_ER}	Page Erase (ER)	—	2	—	ms	
t_{EE_ERWP}	Page Erase-Write (ERWP)	—	4	—	ms	
Program Flash Memory Specifications						
E_{FL}*	**Flash memory cell endurance**	**10k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{FL_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
V_{FL_UPDI}	**V_{DD} for Chip Erase operation**	**$V_{BODLEVEL0}$(1)**	**—**	**V_{DDMAX}**	**V**	
t_{FL_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{FL_CHER}	**Chip Erase (CHER)**	**—**	**4**	**—**	**ms**	
t_{FL_WP}	Page Write (WP)	—	2	—	ms	
t_{FL_ER}	Page Erase (ER)	—	2	—	ms	
t_{FL_ERWP}	Page Erase/Write (ERWP)	—	4	—	ms	
t_{FL_UPDI}	Chip Erase with UPDI	—	40	—	ms	32 KB Flash

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Note:

1. **The Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON during Chip Erase. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.**

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
B	05/2024	• Document: – Editorial updates • Added new errata: – Device: • 2.2.1. IDD Power-Down Current Consumption • 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values • 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces – ADC: 2.3.3. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode – CRCSCAN: 2.5.1. Running CRC Scan on Part of The Flash is Non-Functional – NVMCTRL: 2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register – TCA: 2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode – USART: 2.9.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field • Added new data sheet clarifications: – I/O Multiplexing and Considerations: • 3.1.1. I/O Multiplexing – Electrical Characteristics: • 3.2.1. I/O Pin Characteristics • 3.2.2. SPI - Timing Characteristics • 3.2.3. Programming Time
A	09/2021	Initial document release

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