

## **ZL40292/293/294/295 Silicon Errata**

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The ZL4029x family of devices that you have received conform functionally to the current device data sheet, except for the anomaly described in this document.

### **1.0 SMBUS GLITCH**

#### **1.1 Problem Description**

During the power on reset, ZL4029x will generate a glitch on the SMBUS SDA line with duration from 300 ns to 490 ns. The glitch occurs 230 ns to 480 ns after the control signal PWRGD\_PWRDN# fed to ZL4029x goes high upon the power up. Subsequent toggling of PWRGD\_PWRDN# will not cause the glitch unless the power supply is cycled again. This glitch could potentially affect some other devices that share the same SMBUS during the power up.

#### **1.2 Affected Silicon Revisions**

Device Revision Code: Byte 5, bits 7:4

**TABLE 1: AFFECTED SILICON REVISIONS**

Device Revision	Code	Affected or Unaffected
A0	0b0010	Affected
A1	0b0011	Affected
A2	0b0100	Unaffected

#### **1.3 Work Around**

If you do not see any problem on the power up in your system, the issue can be ignored. Each ZL4029x device is not sensitive to this glitch, and there will not be any consequences if multiple ZL4029x devices are connected to the same SMBUS.

If another device connected to the same SMBUS experiences this issue during the power up, sequence the PWRGD\_PWRDN# control signal such that the device in question gets PWRGD\_PWRDN# at least 1  $\mu$ s after the ZL4029x device.

#### **1.4 Fix**

All production devices with the following Device Revision Code (Byte 5, bits 7:4) have eliminated the power on glitch on the SMBUS SDA line.

Device Revision Code: 0b0100.

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## APPENDIX A: REVISION HISTORY

### Revision A (February 2023)

- Converted errata document from acquired company to Microchip format.

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