AVR64EA28/32/48

Silicon Errata and Data Sheet Clarifications

The AVR64EA28/32/48 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002443), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR64EA28/32/48 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002443) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. B1(1)
Device	2.2.1. NVM Programming Does Not Work Below 2.7V	X
	2.2.2. Reduced Flash Endurance for VDD Below BODLEVEL3	X
CRCSCAN	2.3.1. Running CRC Scan on Part of The Flash is Non-Functional	X
NVMCTRL	2.4.1. Flash Multi Page Erase Non-Functional from UPDI	X
	2.4.2. Flash Page Erase/Write Operation Non-Functional	X
USART	2.5.1. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 NVM Programming Does Not Work Below 2.7V

Performing an erase or write operation when V_{DD} is below 2.7V may fail. It is recommended to ensure that V_{DD} is above 2.7V before starting an erase or write operation. Alternatively BOD can be enabled with level set to BODLEVEL2, or higher.

Work Around
None.

Affected Silicon Revisions

Rev. B1
X

2.2.2 Reduced Flash Endurance for V_{DD} Below BODLEVEL3

If operating at V_{DD} below BODLEVEL3, Flash endurance is reduced to 1k erase/write cycles. The reduction is independent of the V_{DD} level during erase/write.

Work Around
None

Affected Silicon Revisions

Rev. B1
X

2.3 CRCSCAN - Cyclic Redundancy Check Memory Scan

2.3.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from `0x00`
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from `0x00`
- Running CRC scan on the entire Flash works

Work Around
None

Affected Silicon Revisions

Rev. B1
X

2.4 NVMCTRL - Nonvolatile Memory Controller

2.4.1 Flash Multi Page Erase Non-Functional from UPDI

Performing a Flash multi-page erase (writing the CMD bitfield in NVMCTRL.CTRLA to FLMPERn) from UPDI does not work on the boot section. It is not recommended to use multi-page erase on any Flash section.

Work Around
Use Flash page erase (writing the CMD bitfield in NVMCTRL.CTRLA to `0x08`).

Affected Silicon Revisions

Rev. B1
X

2.4.2 Flash Page Erase/Write Operation Non-Functional

If the Flash NRWW section is read during a Flash page erase/write operation (the CMD bitfield in NVMCTRL.CTRLA is `0x05`), the page write will be ignored.

Work Around
Perform Flash page erase (writing the CMD bitfield in NVMCTRL.CTRLA to `0x08`) and write (writing the CMD bitfield in NVMCTRL.CTRLA to `0x04`) as two separate operations. Alternatively, enter a sleep mode after the Flash page erase/write operation has been started, with NVMREADY as the only interrupt source.

Affected Silicon Revisions

Rev. B1
X

2.5 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.5.1 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around
When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '`0`' and then a '`1`' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. B1

X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002443).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Electrical Characteristics - RSTCTRL and BOD

A clarification has been made to change the Brown-out Detect Voltage (V_{BOD}) in the *Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-out Detector Specifications* table.

Table 35-15. Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-out Detector Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
t_{RST} *	$\overline{\text{RESET}}$ pin pulse-width low to ensure a Reset	2.5	—	—	µs	
R_{RST_UP} *	$\overline{\text{RESET}}$ pin pull-up resistor	—	35	—	kΩ	
T_{OST} *	Oscillator start-up timer period(1)	—	1024	—	cycles	
V_{BOD+}	Brown-out Detect Voltage, rising slope(2)	—	1.75	**—**	V	BODLEVEL0
			1.90	**2.10**	V	BODLEVEL1
			2.60	**2.80**	V	BODLEVEL2
			4.30	**4.60**	V	BODLEVEL3
V_{BOD-}	Brown-out Detect Voltage, falling slope(2)	**1.62**	1.75	—	V	BODLEVEL0
		1.80	1.90		V	BODLEVEL1
		2.43	2.60		V	BODLEVEL2
		4.05	4.30		V	BODLEVEL3
V_{BOD_HYS}	Brown-out Detect hysteresis	—	25	—	mV	
t_{BOD_ST}	Brown-out Detect start-up time from sleep	—	30	—	µs	
t_{BOD}	BOD sampling time when used in Sampling mode	—	$1/f_{BOD}$	—	ms	
t_{BOD_RST}	Brown-out Reset response time	—	4	—	µs	$V_{DD} = V_{BOD}$ - 0.1V

† Data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

* These parameters are characterized but not tested in production.

Notes:

1. By design, the Oscillator Start-up Timer (T_{OST}) counts the first 1024 cycles, independent of frequency.
2. VDD and GND must be capacitively decoupled as close to the device as possible to ensure these voltage tolerances. Recommended values are 0.1 µF and 0.01 µF in parallel.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
A	02/2023	Initial document release

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