

PIC16F17126/46 Silicon Errata and Datasheet Clarifications

The PIC16F17126/46 devices that you have received conform functionally to the current device data sheet (DS40002343D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F17126/46 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		B0	B2
PIC16F17126	0x30E0	0xA040	0xA042
PIC16F17146	0x30E1	0xA040	0xA042



Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				B0	B2
Analog-to-Digital Converter with Computation (ADCC)	Double Sample Conversions	1.1.1	An unexpected acquisition time is added between the first and second conversions.	X	
Host Synchronous Serial Port (MSSP)	I ² C Start and Stop Interrupt Function	1.2.1	A race condition can cause the Start and/or Stop flags to be set when I ² C is enabled.	X	
Configuration Words (CONFIG)	Sleep	1.3.1	Waking from Sleep may cause unexpected behavior.	X	

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

1.1.1 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

- Method 1: Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.
- Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

B0	B2						
X							

1.2 Module: MSSP

1.2.1 The I²C Start and/or Stop Flags May Be Set When I²C Is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

- Disable the Start and Stop conditions interrupt functions.
- Enable the I²C module.
- Wait 250 ns + six instruction cycles (F_{osc}/4).
- Clear the Start and Stop conditions interrupt flags.
- Enable the Start and Stop conditions interrupt functions if used.

```

SSPxCON3bits.SCIE = 0;           // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;           // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;          // Enable I2C
Delay();                         // Wait for 250 ns + 6 instruction cycles (Fosc/4)
PIRxbits.SSPxIF = 0;             // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;           // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;           // Enable Stop condition interrupt if used

```

Affected Silicon Revisions

B0	B2						
X							

1.3 Module: Configuration Words (CONFIG)**1.3.1 Waking from Sleep May Cause Unexpected Behavior**

Waking from Sleep may cause unexpected behavior.

Work around

Do not use the `SLEEP` instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

Affected Silicon Revisions

B0	B2						
X							

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002343D):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
B	8/2022	Added new silicon revision B2; updated datasheet revision letter; added silicon issue 1.3.1.
A	3/2022	Initial release of this document.

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