LAN8804

LAN8804 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the LAN8804 family of devices, which includes the following:

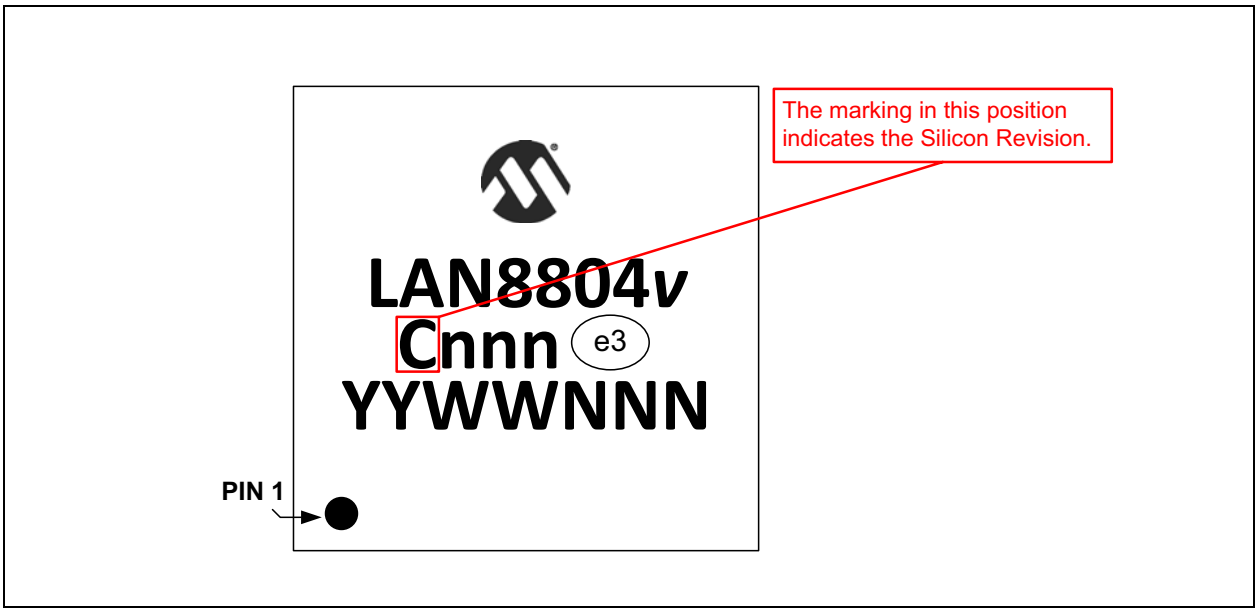
- LAN8804/ZMX
- LAN8804-V/ZMX

The silicon errata discussed in this document are for silicon revision(s) listed in Table 1. The silicon revision can be determined by the device's top marking as indicated in Figure 1. A summary of LAN8804 silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
LAN88x4/ZMX LAN88x4-V/ZMX	ALL

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of Figure 1 is to detail the top markings of an example part and highlight the location of the date code. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary
1.	1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification
2.	Link up time improvements for 1000BASE-T mode
3.	First frame received in 10BASE-T mode may be corrupted
4.	Analog front-end not optimized for PHY-side shorted center taps
5.	MODE[4:0] configuration strap override settings not reset to chip defaults
6.	1000BASE-T Slave Mode cable reach improvement > 100m
7.	IEEE Clause 40 PMA compliance tests may fail
8.	Near-end loopback errors in 10BASE-T mode
9.	1000BASE-T PMA EEE TX wake timer is non-compliant
10.	QSGMII interface may exceed T_TJ specification
11.	Late Collisions in half-duplex modes
12.	MII Isolate mode (mr0 Basic Control Register bit 10) not functioning
13.	IEEE Clause 14 MAU compliance tests may fail
14.	tx_config_reg bit 15 sent from the PHY is always 0
15.	LDO feature does not function correctly

Silicon Errata Issues

Module 1: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

DESCRIPTION

The device’s 1000BASE-T Transmitter Distortion exceeds the <10mV limit indicated in the IEEE specification.

END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following Application Note has more details regarding the Gigabit Transmit Distortion test:

https://www.microchip.com/en-us/application-notes/an3455

Work Around

None

PLAN

This erratum will not be corrected in a future revision.

Module 2: Link up time improvements for 1000BASE-T mode

DESCRIPTION

When establishing a 1000BASE-T link, the PHY link-up time may exceed 10 seconds.

END USER IMPLICATIONS

In order to reduce the link-up time, an initialization script should be applied to each port of the quad-PHY.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 3: First frame received in 10BASE-T mode may be corrupted

DESCRIPTION

When operating the PHY in a 10BASE-T link, the first frame received may contain data errors due to a receiver initialization error. All frames subsequent to the first frame are received normally.

END USER IMPLICATIONS

This error only occurs in 10BASE-T links and only affects the first frame received after link establishment. It has no other impact. The error is random in occurrence and cannot be predicted upon 10BASE-T link establishment. When the error occurs, the received frame will output on the QSGMII interface of the PHY but will result in a frame error at the host MAC.

Work Around

None

PLAN

This erratum will not be corrected in a future revision.

Module 4: Analog front-end not optimized for PHY-side shorted center taps

DESCRIPTION

When connecting the PHY to magnetics which short center-tap connections on the PHY-facing winding, the default register settings of the device need to be optimized for better electrical performance.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. Its side effect is a negligible power penalty when applying these settings to the PHY, therefore it is recommended to apply these settings irrespective of the magnetic's internal topology. As such, power consumption values for the device reflect this initialization sequence applied to all four ports of the PHY.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 5: MODE[4:0] configuration strap override settings not reset to chip defaults

DESCRIPTION

The Strap override registers EP2.2 and EP2.81 should be reset to hardware defaults, upon assertion of register 0 bit 15 (PHY Hard Reset [[RESET]) but are not. As a result, an overwrite-defaults operation needs to be performed anytime that register 0 bit 15 is used.

END USER IMPLICATIONS

A software workaround sequence to return the EP2.2 and EP2.81 registers to their hardware defaults should be applied, just prior to asserting register 0 bit 15.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 6: 1000BASE-T Slave Mode cable reach improvement > 100m

DESCRIPTION

The default register settings of the device need to be optimized for better 1000BASE-T Slave linking performance, if connected to cable lengths > 100m.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. There is no negative side effects and therefore it is recommended to apply these settings irrespective of the PHY's actual environmental conditions.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 7: IEEE Clause 40 PMA compliance tests may fail

DESCRIPTION

The default register settings of the PHY's 1000BASE-T PMA are sub-optimal, and may result in UNH compliance failures for Clause 40 PMA Transmitter tests. The default register settings of the device need optimization.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. It is recommended to apply the settings unconditionally, for better PHY interoperability performance.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 8: Near-end loopback errors in 10BASE-T mode

DESCRIPTION

When the 10BASE-T datapath is configured for near-end loopback, clocking errors may result in traffic corruption. The default register settings of the device need updates.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. It is recommended to apply the settings unconditionally, for robust loopback performance in 10BASE-T mode.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 9: 1000BASE-T PMA EEE TX wake timer is non-compliant

DESCRIPTION

The hardware default of the PHY's 1000BASE-T PMA EEE TX wake timer exceeds the UNH IoL test maximum for the Waketx test.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. It is recommended to apply the settings unconditionally, to remain UNH compliant for the Clause 40 EEE Waketx test.

Work Around

This erratum has been addressed in MEPA v2021.12 and later.

This erratum will be addressed in Linux driver micrel.c, with patch uploads in March 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 10: QSGMII interface may exceed T_TJ specification

DESCRIPTION

The QSGMII transmitter total jitter Max is 0.35 UIpp for the device. The QSGMII revision 1.3 specification for T_TJ Max limit is 0.3 UIpp.

END USER IMPLICATIONS

A QSGMII receiver connected to this PHY needs to support an excess of 0.05 UIpp total jitter, above and beyond the QSGMII R_TJ Max limit, in order for the QSGMII link to comply with the BER.

Work Around

Use the 125MHz PHY reference clock for improved T_TJ performance.

For Rev. C silicon:
To meet the QSGMII T_TJ specification, the 125MHz reference clock source must be used in conjunction with TVDDAL_SERDES/VDDTXL_SERDES and VDDAH_SERDES voltage levels meeting or exceeding the mid-point of their voltage range listed in the Power Consumption tables of the datasheet.

For Rev. B silicon:
Performance is not guaranteed beyond the data sheet specifications even with a 125MHz reference clock source.

PLAN

This erratum will not be corrected in a future revision.

Module 11: Late Collisions in half-duplex modes

DESCRIPTION

The PHY may incur Late Collisions while operating on a half-duplex network. The PHY delays which cause the Late Collisions are not limited to a particular speed, and the frequency of Late Collisions increases with longer cable media. As a result, half-duplex operation is not recommended except where higher-layer networking protocols can guarantee re-transmission in the event of frame loss at the Ethernet Layer, due to Late Collisions.

END USER IMPLICATIONS

The PHY may not successfully retransmit frames if it detects a collision while operating on a half-duplex network.

Work Around

Layer 3 (and above) communications protocols must be relied upon to detect and retransmit any lost segments of a packet transmission.

PLAN

Future plans for this erratum are in development.

Module 12: MII Isolate mode (mr0 Basic Control Register bit 10) not functioning

DESCRIPTION

Basic Control register mr0 bit 10 does not work and has no effect on the PHY when the bit value is changed. The PHY will remain in Non-Isolated (Normal operational) mode regardless of the mr0 bit 10 value.

END USER IMPLICATIONS

the MII Isolate function cannot be used.

Work Around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 13: IEEE Clause 14 MAU compliance tests may fail

DESCRIPTION

The default register settings of the PHY's 10BASE-T/10BASE-Te transmitter are sub-optimal and may result in UNH compliance failures for Clause 14 MAU Transmitter tests. The default register settings of the device require optimization.

END USER IMPLICATIONS

An initialization script should be applied to each port of the quad-PHY. For better PHY interoperability performance, it is recommended to apply the settings unconditionally. The UNH compliance test case 14.1.7 - Transmitter Waveform for Start of TP_IDL may still marginally fail, with certain loads.

Work Around

This erratum has been addressed in MEPA v2022.09 and later. This erratum will be addressed in Linux driver micrel.c, with patch uploads in September 2022 to the net-next subsystem tree of the kernel.

PLAN

This erratum will not be corrected in a future revision.

Module 14: tx_config_reg bit 15 sent from the PHY is always 0

DESCRIPTION

The Q-USGMII transmitted link status bit [15] in the advertised tx_config_reg remains 0, regardless of actual media link state.

END USER IMPLICATIONS

A QSGMII/Q-USGMII receiver connected to this PHY cannot ascertain link status from the control information received from the PHY.

Work Around

None.

PLAN

Future plans for this erratum are in development.

Module 15: LDO feature does not function correctly

DESCRIPTION

The on-chip LDO controller output in conjunction with pin **LDO_O** is unsupported.

END USER IMPLICATIONS

The external system must power the **VDDAL_x**, **VDDTXL_SERDES**, and **VDDCORE** rails of the PHY. The LDO output controller pin **LDO_O** is not guaranteed to function correctly, and therefore should be left unconnected.

Work Around

None.

PLAN

Future plans for this erratum are in development.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80001001B (07-06-22)	All	Updated document to reflect latest Revision C silicon.
	Modules 11. through 15.	Added new modules 11. through 15.
DS80001001A (02-02-22)	All	Initial release

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ISBN: 9781668308257

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