



PIC18F26/46/56Q83

PIC18F26/46/56Q83 Silicon Errata and Data Sheet Clarifications

The PIC18F26/46/56Q83 devices that you have received conform functionally to the current device data sheet (DS40002253C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/46/56Q83 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A1	A2
PIC18F26Q83	0xA306	0xA001	0xA002
PIC18F46Q83	0xA307	0xA001	0xA002
PIC18F56Q83	0xA308	0xA001	0xA002



Important: Refer to the **Device/Revision ID** section in the current “**PIC18FXXQ84 Family Programming Specification**” (DS40002137C) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A1	A2
UTMR	Level-triggered ERS Start/Reset condition	1.1.1.	Dead zone exists in level-triggered Start/Reset condition when ERS signal is generated due to an SFR access	X	X
	Hardware Reset condition	1.1.2.	Reset does not happen at period match when the prescaler > 0 and the Timer Stops at Period Match (includes One Shot mode)	X	X
	Output Pulse	1.1.3	Pulse output does not occur at period match when the prescaler>0	X	X
Note: Only those issues indicated in the last column apply to the current silicon revision.					

1. Silicon Errata Issues

CAUTION

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = 'b11 or RESET = 'b01) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

A1	A2
X	X

1.1.2 Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the timer is configured to reset at a hardware-based event (RESET = 'b01 or 'b10 or 'b11) and stop at period match (STOP = 'b11), the timer stops at period match but does not reset (no pulse output occurs and ZIF interrupt is not generated).

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

A1	A2
X	X

1.1.3 Pulse Output Does Not Occur at Period Match When the Prescaler = 1

The timer output pulse will not occur at period match when prescaler = 1.

Work around

1. Use prescaler = 0 or prescaler > 1 when a pulse output is desired.

Affected Silicon Revisions

A1	A2
X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002253C):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Memory Programming Specifications

The flash memory cell endurance specification is reduced to **1k** minimum. The corresponding parameter (E_P) will be updated in the next revision of datasheet (DS40002253).

Table 2-1. Memory Programming

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	1M	4M	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	—	11	ms	
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	1k	—	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (Note 1)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Page Write	—	—	10	ms	
MEM36	T_{SE}	Self-Timed Page Erase	—	—	11	ms	
MEM37	T_{P_WRD}	Self-Timed Word Write	—	—	75	μs	
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.							
Note:							
1. Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.							

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
B	08/2022	Added Datasheet Clarification 2.1.
A	02/2021	Initial document release.

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