SAMHAXGXXA

SAMHAXGXXA-B Errata

ATSAM HAXGXXA

The ATSAM HAXGXXA family of devices that you have received conform functionally to the current Device Data Sheet (DS20005841E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1.

The errata described in this document will be addressed in future revisions of the ATSAM HAXGXXA family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM HAX Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision (DID.REVISION[3:0])		
		E	F	G
ATSAMHA1G16A	0x10011432	0x4	N/A	N/A
ATSAMHA1G15A	0x10011433			
ATSAMHA1G14A	0x10011434			
ATSAMHA1G16A-B	0x10011583	N/A	0x5	N/A
ATSAMHA1G15A-B	0x10011584			
ATSAMHA1G14A-B	0x10011585			
ATSAMHA0G16A-B	0x10011586			
ATSAMHA0G15A-B	0x10011587			
ATSAMHA0G14A-B	0x10011588			
ATSAMHA1G17A-B	0x10012698	N/A	N/A	0x6
ATSAMHA0G17A-B	0x1001269C			

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS20005841E) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Errata Summary

Table 2. Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				E	F	G
XOSC32K	Automatic Gain Control	1.1.1	The automatic amplitude control of the XOSC32K does not work.	X	X	X
XOSC32K	External Reset	1.1.2	If the external XOSC32K fails, the external reset will not reset the GCLKs sourced by the XOSC32K.	X	X	X

.....continued

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				E	F	G
DFLL48M	Write Access to DFLL Register	1.2.1	The DFLL clock must be requested before being configured.	X	X	X
DFLL48M	False Out of Bound Interrupt	1.2.2	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X	X
DFLL48M	DFLL Status Bits (PCLKSR Register)	1.2.3	The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode may be incorrect after a USB suspend state.	X	X	X
FDPLL	DPLLRATIO Register FDPLL Ratio Value	1.3.1	When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.	X	X	X
ADC	Offset correction	1.4.1	Offset correction is not supported in the 8-bit and 10-bit conversion resolution.	X	X	X
DEVICE	APB Clock	1.5.1	If APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system.	X	X	X
DEVICE	SYSTICK Calibration Value	1.5.2	The SYSTICK calibration value specified in the data sheet is incorrect.	X	X	
DEVICE	High Leakage Current on VDDIO	1.5.3	When external reset is active it causes a high leakage current on VDDIO.	X		
DEVICE	Supply Rise Rates	1.5.4	If NRES and RESETN are not connected to each other, there must be a minimum rise rate on the VDDANA pin to ensure correct start-up.	X		
DEVICE	Standby Entry	1.5.5	Potential device lockup upon standby entry when Systick interrupt is enabled.	X	X	X
DEVICE	Standby Wake-up	1.5.6	Potential lockup on standby wakeup with interrupts disabled.	X	X	X
DAC	EMPTY Flag is Set When Leaving Standby Mode	1.6.1	DAC.INTFLAG.EMPTY will be set after exiting Sleep mode.	X	X	X
DMAC	Consecutive Write Instructions to CRCDATAIN	1.7.1	If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.	X	X	
DMAC	Linked Descriptors	1.7.2	When at least one channel using linked descriptors is already active, enabling another DMA channel may result in a channel Fetch Error or an incorrect descriptor fetch.	X	X	
DSU	Pause-on-Error is Not Functional	1.8.1	The MBIST Pause-on-Error feature is not functional.	X	X	
EIC	Interrupts	1.9.1	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges with the filter enabled, a spurious flag may appear.	X	X	
NVMCTRL	Spurious Writes	1.10.1	The default value of MANW in NVM.CTRLB is '0', which may lead to spurious writes to the NVM.	X	X	X
NVMCTRL	NVMCTRL.INTFLAG.READY	1.10.2	The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a '1' value.	X		
NVMCTRL	RWW NVM Command	1.10.3	Incorrect data fetch after RWW NVM command	X	X	X
PORT - I/O Pin Controller	Write Protect	1.11.1	Non-debugger IOBUS writes to PAC Write-Protected registers are not prevented when the PORT is PAC Write-protected.	X	X	X
SERCOM	SPI with Client Select Low Detection	1.12.1	If the SERCOM is enabled in SPI mode with SSL detection enabled and CTRLB.RXEN = '1', an erroneous client select low interrupt may be generated.	X		
SERCOM	USART in Auto-Baud Mode	1.12.2	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X	
SERCOM	NACK and Repeated Start in I^2C Host Mode	1.12.3	For High-Speed Host Read operations, sending a NACK forces a STOP to be issued making repeated start not possible in that mode.	X	X	X
SERCOM	SERCOM-USART: Collision Detection	1.12.4	In USART operating mode with Collision Detection enabled, the SERCOM will not abort the current transfer as expected if a collision is detected.	X	X	X
SERCOM	SERCOM-USART: USART in Debug Mode	1.12.5	In USART operating mode, if DBGCTRL.DBGSTOP = '1', data transmission is not halted after entering Debug mode.	X	X	X
SERCOM	SERCOM-I^2C: Client Mode with DMA	1.12.6	In I^2C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push data to the DATA register.	X	X	X
SERCOM	SERCOM-I^2C: I^2C Mode in 10-bit Address	1.12.7	10-bit addressing in I^2C Client mode is not functional.	X	X	X

.....continued

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				E	F	G
SERCOM	SERCOM-SPI: Data Preload	1.12.8	In SPI Client mode and with Client Data Preload Enabled, the first data sent from the client will be a dummy byte.	X	X	X
SERCOM	CLKHOLD Bit Status in I^2C	1.12.9	STATUS.CLKHOLD bit may be written whereas it is a read-only status bit in both Host and Client modes.	X	X	X
SERCOM	Quick Command I^2C	1.12.10	When Quick command is enabled (CTRLB.QCEN = '1'), the software may issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bitfields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = '1', a bus error will be generated.	X	X	X
SERCOM	Repeated Start I^2C	1.12.11	For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.	X	X	X
SERCOM	Client Mode I^2C	1.12.12	In Client mode, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.	X	X	X
SERCOM	Software Reset	1.12.13	Software Reset (CTRLA.SWRST=1) is not functional when the SERCOM is not enabled (CTRAL.ENABLE=0).	X	X	X
SERCOM	SERCOM Wakeup	1.12.14	The SERCOM USART does not wake up the device on Error Interrupt (INTFLAG.ERROR = 1).	X	X	X
SERCOM	SERCOM I^2C RXNACK	1.12.15	RXNACK invalid during I2CS_DRDY handler	X	X	X
SERCOM	SERCOM I^2C AACKEN	1.12.16	I^2C Slave AACKEN not usable with repeated start.	X	X	X
TCC	RAMP 2 Mode	1.13.1	In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp may have two restarts.	X		
TCC	CAPTMARK is Not Functional	1.13.2	FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet.	X	X	
TCC	Capture Using PWP/PPW Mode	1.13.3	When a capture is done using PWP or PPW mode, CC0 and CC1 are always filled with the period. It is not possible to get the pulse width.	X		
TCC	Advance Capture Mode	1.13.4	Advance capture mode does not work.	X	X	
TCC	MAX Capture Mode	1.13.5	In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurred within two cycles before TOP, the value captured is '0' instead of TOP.	X	X	
TCC	Dithering Mode	1.13.6	Using TCC in Dithering mode with external retrigger events may lead to an unexpected stretch of right-aligned pulses or a shrink of left-aligned pulses.	X	X	
TCC	Interrupt Flags	1.13.7	The TCC interrupt flags are not always properly set when using asynchronous TCC features.	X		
TCC	PATTB	1.13.8	The PATTB register write will not update the PATT register on an update condition.	X	X	X
TCC	PERBUF	1.13.9	In downcounting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.	X	X	X
TCC	TCC with EVSYS in SYNC/RESYNC Mode	1.13.10	TCC Peripheral is not compatible with an EVSYS channel in SYNC or RESYNC Mode.	X	X	X
TCC	Prescale	1.13.11	A DMA transfer to the TCC CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC) and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024.	X	X	X
TC	TC with EVSYS in SYNC/RESYNC Mode	1.14.1	TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.	X	X	X
TC	DMA Trigger	1.14.2	When using TC MC0 as a trigger source for the DMA, it will not work.	X	X	
SYSCTRL	XOSC	1.15.1	The XOSC may prevent entry into Standby mode regardless of XOSC.RUNSTDBY value.	X	X	X
SYSCTRL	BOD33 interrupts	1.15.2	The BOD33 interrupt may not be generated second time if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) while in Active mode.	X	X	X
SYSCTRL	BOD33 hysteresis	1.15.3	The BOD33 hysteresis may not work if other reset sources are active.	X	X	X

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1. ATSAM HAXGXXA

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): the device variant denotes functional differences, whereas the die revision marks evolution of the die.

1.1 32.768 kHz Crystal Oscillator (XOSC32K)

1.1.1 Automatic Gain Control

The automatic amplitude control of the XOSC32K does not work.

Work Around
Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0).

Affected Silicon Revisions

E	F	G
X	X	X

1.1.2 External Reset

If the external XOSC32K fails, neither the external pin RST, nor the GCLK software reset may reset the GCLK generators using XOSC32K as the source clock.

Work Around
Do a power cycle to reset the GCLK generators after an external XOSC32K failure.

Affected Silicon Revisions

E	F	G
X	X	X

1.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.2.1 Write Access to DFLL Register

The DFLL clock must be requested before being configured; otherwise, a write access to a DFLL register may freeze the device.

Work Around
Write a ‘0’ to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

E	F	G
X	X	X

1.2.2 False Out of Bound Interrupt

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and therefore, may be false out of bounds interrupts.

Work Around
Enable the DFLL out of bounds (DFLLOOB) interrupt when configuring the DFLL in closed loop mode. In the DFLLOOB ISR verify the COARSE and FINE calibration bits and process as needed.

Affected Silicon Revisions

E	F	G
X	X	X

1.2.3 DFLL Status Bits (PCLKSR Register)

The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode may be incorrect after a USB suspend state.

Workaround
Do not monitor the DFLL status bits in the PCLKSR register during the USB Clock Recovery mode.

Affected Silicon Revisions

E	F	G
X	X	X

1.3 96 MHz Fractional Digital Phase-Locked Loop (FDPLL)

1.3.1 DPLLRATIO Register FDPLL Ratio Value

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround
Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

Affected Silicon Revisions

E	F	G
X	X	X

1.4 ADC

1.4.1 Offset Correction

Offset correction using the OFFSETCORR register is not supported in the 8-bit and 10-bit conversion resolution.

Workaround
None

Affected Silicon Revisions

E	F	G
X	X	X

1.5 Device

1.5.1 APB Clock

If the APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, and as a consequence, debug operation is impossible.

Work Around

Do not make read access to read-synchronized registers when the APB clock is stopped and GCLK is running. To recover from this condition, power cycle the device or reset the device using the $\overline{\text{RESET}}$ pin.

Affected Silicon Revisions

E	F	G
X	X	X

1.5.2 SYSTICK Calibration Value

The SYSTICK calibration value is incorrect.

Work Around

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM® Cortex®-M0+ documentation.

Affected Silicon Revisions

E	F	G
X	X	

1.5.3 High Leakage Current on VDDIO

When external reset is active it causes a high leakage current on VDDIO.

Work Around

Minimize the time external reset is active.

Affected Silicon Revisions

E	F	G
X		

1.5.4 Supply Rise Rates

If NRES and RESETN are not connected to each other, there must be a minimum rise-rate on the VDDANA pin to ensure correct startup

Work Around

When the reset output of the SBC is not connected to the reset input of the MCU, the rise-rate on the VDDANA pin between 1.25V and 1.75V must be > 0.0004 V/µs.

Affected Silicon Revisions

E	F	G

X	X	X

1.5.5 Potential Lockup on Standby Entry

If the Systick interrupt is enabled, a device lockup may occur when the Systick interrupt coincides with the standby entry.

Work Around

Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

E	F	G
X	X	X

1.5.6 Potential Lockup on Standby Wakeup with Arm Core PRIMASK=1

Upon wake up from standby with Arm Core register PRIMASK = 1, the first instruction fetched by the CPU in Flash memory will be the first instruction following the WFI. This instruction may be returned corrupted and lead to unpredictable behavior.

If PRIMASK = 0, the first instruction fetched by the CPU will be the first instruction of the interrupt handler. This one will be correctly returned to the CPU.

Work Around

Two possible workarounds may be used independently:

1. Disable Flash sleep in Standby Sleep mode (SLEEPPRM = DISABLED).
2. Place the standby sleep function in SRAM and make sure that at least one dummy Flash fetch is completed before exiting the function. This may be achieved by reading from two different locations in Flash memory with addresses separated by at least the cache size. Because the first read could be a cache hit, the second one will be a cache miss and will force an actual read from Flash memory.

The following code may be used:

```
__attribute__((noinline, section(".ramfunc")))
                    void ram_sleep(void)
                    {
                    __DSB();
                    __WFI();

                    // The following sequence ensures that the flash is ready before
returning from the RAM code
                    #define CACHE_SIZE_IN_BYTES 64
                    ((volatile unsigned int *)FLASH_ADDR)[CACHE_SIZE_IN_BYTES/sizeof(unsigned
int)];     //will read a word at FLASH_ADDR + 0x40 in this case
                    ((volatile unsigned int *)FLASH_ADDR)[(CACHE_SIZE_IN_BYTES*2)/
sizeof(unsigned int)]; //will read a word at FLASH_ADDR + 0x80 in this case
                    }
```

Affected Silicon Revisions

E	F	G
X	X	X

1.6 Digital-to-Analog Controller (DAC)

1.6.1 EMPTY Flag is Set When Leaving Standby Mode

When DAC.CTRLA.RUNSTDBY = ‘0’ and DATABUF is written (not empty), and if the device goes to Standby Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exiting Sleep mode.

Work Around

After waking from Standby mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

Affected Silicon Revisions

E	F	G
X	X	X

1.7 Direct Memory Access Controller (DMAC)

1.7.1 Consecutive Write Instructions to CRCDATAIN

If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.

Work Around

Add a `NOP` instruction between each write to the CRCDATAIN register.

Affected Silicon Revisions

E	F	G
X	X	

1.7.2 Linked Descriptors

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) may result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This occurs if the channel number of the channel being enabled is lower than the channel already active.

Work Around

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the newly-enabled DMA channel must be greater than the other channel numbers.

Affected Silicon Revisions

E	F	G
X	X	

1.8 Device Service Unit (DSU)

1.8.1 Pause-on-Error is Not Functional

The MBIST Pause-on-Error feature is not functional.

Workaround

None.

Affected Silicon Revisions

E	F	G
X	X	

1.9 External Interrupt Controller (EIC)

1.9.1 Interrupts

When the EIC is configured to generate an interrupt on a low level, rising edge, or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag may appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

Work Around

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

E	F	G
X	X	

1.10 Non-Volatile Memory Controller (NVMCTRL)

1.10.1 Spurious Writes

The default value of MANW in NVM.CTRLB is ‘0’, which may lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to the NVM area.

Work Around

Set MANW in the NVM.CTRLB register to ‘1’ at start-up

Affected Silicon Revisions

E	F	G
X	X	X

1.10.2 NVMCTRL.INTFLAG.READY Bit

The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a ‘1’ value. If a new `RWWEEER` command is issued, it may be accepted even if the previous `RWWEEER` command is ongoing. The ongoing NVM `RWWEER` command will be aborted and the content of the row under erase will be unpredictable.

Work Around

Perform a dummy write to the page buffer right before issuing a `RWWEEER` command. This will cause the INTFLAG.READY bit to behave as expected.

Affected Silicon Revisions

E	F	G
X		

1.10.3 RWW NVM Command

Incorrect Data Fetch after RWW NVM Command

Issuing an NVM command on RWWEE region while the NVM Controller cache is enabled may result in incorrect data fetch afterward.

Work Around
Disable the NVM Controller cache before issuing any RWW NVM command. Enable the cache only after the internal RWW operation is complete.

Pseudo Code

```
NVMCTRL->CTRLB.CACHEDIS |= NVMCTRL_CTRLB_CACHEDIS_Msk;
                        NVMRWW_ErasePage();
                        while(NVMCTRL_IsBusy());
                        NVMCTRL->CTRLB.CACHEDIS &= ~NVMCTRL_CTRLB_CACHEDIS_Msk;
```

Affected Silicon Revisions

E	F	G
X	X	X

1.11 PORT - I/O Pin Controller

1.11.1 Write-Protect

The non-debugger IOBUS writes to the PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.12 Serial Communication Interface (SERCOM)

1.12.1 SPI with Client Select Low Detection

If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN = ‘1’, an erroneous client select low interrupt (INTFLAG.SSL) may be generated.

Work Around
Enable the SERCOM first with CTRLB.RXEN = ‘0’. In a subsequent write, set CTRLB.RXEN = ‘1’.

Affected Silicon Revisions

E	F	G
X		

1.12.2 USART in Auto-baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	

1.12.3 NACK and Repeated Start in I²C Host Mode

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in this mode.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.4 SERCOM-USART: Collision Detection

In USART Operating mode with Collision Detection enabled (CTRLB.COLDEN = '1'), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Work Around
The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.5 SERCOM-USART: USART in Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = '1', data transmission is not halted after entering Debug mode.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.6 SERCOM-I²C: Client Mode with DMA

In I²C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push data to the DATA register. Because a NACK was received, the transfer on the I²C bus will not occur causing the loss of this data.

Work Around
Configure the DMA transfer size to the number of data to be received by the I²C host. DMA may not be used if the number of data to be received by the host is unknown.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.7 SERCOM-I²C: I²C Mode in 10-bit Address

10-bit addressing in I²C Client mode is not functional.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.8 SERCOM-SPI: Data Preload

In SPI Client mode and with Client Data Preload Enabled (CTRLB.PLOADEN = ‘1’), the first data sent from the client will be a dummy byte if the host may not keep the Client Select (SS) line low until the end of transmission.

Work Arounds
In SPI Client mode, the Client Select pin (SS) must be kept low by the host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = ‘1’).

Affected Silicon Revisions

E	F	G
X	X	X

1.12.9 CLKHOLD Bit Status in I²C

STATUS.CLKHOLD bit may be written whereas it is a read-only status bit in both Host and Client modes.

Work Arounds
Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.10 Quick Command I²C

When Quick command is enabled (CTRLB.QCEN = ‘1’), the software may issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch Mode is CTRLA.SCLSM = ‘1’, a bus error will be generated.

Work Arounds
Use Quick Command mode (CTRLB.QCEN = ‘1’) only if SCL Stretch Mode is CTRLA.SCLSM = ‘0’.

Affected Silicon Revisions

E	F	G

X	X	X

1.12.11 Repeated Start I²C

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.

Work Arounds

None.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.12 Client Mode I²C

In Client mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Work Arounds

PERBUFlear the STATUS register bits, such as BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR by writing these STATUS bits to '1', when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

E	F	G
X	X	X

1.12.13 Software Reset in SERCOM module

Software Reset (CTRLA.SWRST=1) is not functional when the SERCOM is not enabled (CTRAL.ENABLE=0).

Work Arounds

None

Affected Silicon Revisions

E	F	G
X	X	X

1.12.14 SERCOM Wakeup

The SERCOM USART does not wake up the device on Error Interrupt (INTFLAG.ERROR = 1).

Workaround

Configure the USART to wake up the device on the RX Complete Interrupt (INTENSET.RXC = 1) in order to check the PERR/FERR/BUFOVF status (STATUS.PERR = 1, STATUS.FERR = 1 or STATUS.BUFOVF = 1).

Affected Silicon Revisions

E	F	G
X	X	X

1.12.15 RXNACK invalid during I2CS_DRDY handler

The RXNACK status bit is invalid during the first I2CS_DRDY interruption handler.

Workaround
Use a software flag to track when to ignore RXNACK (equivalent to have it true) and resets this flag in the I2CS_AMATCH interruption handler (workaround inapplicable with AACKEN=1).

Affected Silicon Revisions

E	F	G
X	X	X

1.12.16 I2C Slave AACKEN not usable with repeated start.

The I2C slave AACKEN feature is not usable when doing a repeated start.

Workaround
Do not use the AACKEN feature, implement an AMATCH handler instead.

Affected Silicon Revisions

E	F	G
X	X	X

1.13 Timer/Counter for Control Applications (TCC)

1.13.1 RAMP 2 Mode

In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp may have two restarts.

Work Around
Avoid faults few cycles before the end or the beginning of a ramp.

Affected Silicon Revisions

E	F	G
X		

1.13.2 CAPTMARK is Not Functional

FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet. CAPTMARK may not be used to identify captured values triggered by fault inputs source A or B on the same channel.

Workaround
Use two different channels to timestamp FaultA and FaultB.

Affected Silicon Revisions

E	F	G
X	X	

1.13.3 Capture Using PWP/PPW Mode

When a capture is done using PWP or PPW mode, CC0 and CC1 are always filled with the period. It is not possible to get the pulse width.

Work Around
Use the PWP feature on TC instead of TCC.

Affected Silicon Revisions

E	F	G
X		

1.13.4 Advance Capture Mode

Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these mode. For example, when CC[0] = CAPTMIN, CC[1] = CAPTMAX, CC[2] = CAPTEN, and CC[3] = CAPTEN, CAPTMIN and CAPTMAX will not work.

Work Around
Basic capture mode must be set in lower channel and advance capture mode in upper channel.

For example, CC[0] = CAPTEN , CC[1] = CAPTEN , CC[2] = CAPTMIN, CC[3] = CAPTMAX

All capture will be done as expected.

Affected Silicon Revisions

E	F	G
X	X	

1.13.5 MAX Capture Mode

In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurs within two cycles before TOP, the value captured is '0' instead of TOP.

Work Arounds

1. If the event is controllable, the capture event must not occur when the counter is within two cycles before the TOP value.
2. Use the Timer in Down Counter mode and capture the MIN value instead of the MAX value.

Affected Silicon Revisions

E	F	G
X	X	X

1.13.6 Dithering Mode

Using TCC in Dithering mode with external retrigger events may lead to an unexpected stretch of right-aligned pulses, or a shrink of left-aligned pulses.

Work Around
Do not use retrigger events/actions when the TCC is configured in Dithering mode.

Affected Silicon Revisions

E	F	G
X	X	

1.13.7 Interrupt Flags

The TCC interrupt flags INTFLAG.ERR, INTFLAG.DFS, INTFLAG.UFS, INTFLAG.CNT, INTFLAG.FAULTA,INTFLAG.FAULTB, INTFLAG.FAULT0, INTFLAG.FAULT1 are not always properly set when using asynchronous TCC features.

Work Around
Do not use these flags when using asynchronous TCC features.

Affected Silicon Revisions

E	F	G
X		

1.13.8 PATTB

The PATTB register write will not update the PATT register on an update condition.

Work Around
Write directly to the PATT register when an update is required.

Affected Silicon Revisions

E	F	G
X	X	X

1.13.9 PERBUF

In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.13.10 TCC with EVSYS in SYNC/RESYNC Mode

TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Work Around
Use TCC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

E	F	G
X	X	X

1.13.11 Prescale

A DMA transfer to the TCC.CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC), and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024.

Work Around
Use the TCC.CCB for DMA transfers, or the GCLK division register (GENDIV.DIV) to divide the TCC input clock to a range that allows a TCC prescaler value that is not 64, 256 or 1024. To ensure this does not have an impact on other modules in the system, the divided GCLK used to supply the TCC peripheral with its input clock should not source other peripheral modules.

Affected Silicon Revisions

E	F	G
X	X	X

1.14 Timer/Counter (TC)

1.14.1 TC with EVSYS in SYNC/RESYNC Mode

TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Work Around
Use TC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

E	F	G
X	X	X

1.14.2 DMA Trigger

When using TC MC0 as a trigger source for the DMA, only the first transfer is performed and after that DMA is blocked and does not do any more transfers.

Workaround
Changing the trigger source to TC Overflow makes things work as expected.

Affected Silicon Revisions

E	F	G
X	X	

1.15 SYSCTRL

1.15.1 XOSC

The XOSC may prevent entry into Standby mode regardless of XOSC.RUNSTDBY value.

Work Around
Change the clock source for gclk0 to the internal RC OSC, and then disable the XOSC before entering Standby mode.

Affected Silicon Revisions

E	F	G
X	X	X

1.15.2 BOD33 interrupts

The BOD33 interrupt may only generate once if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) when in Active mode. If in Standby mode, when the BOD33 interrupt is generated, the device will have to be in Active mode while VDDANA increases above BOD.LEVEL to re-enable the BOD33 interrupt.

Work Around
None.

Affected Silicon Revisions

E	F	G
X	X	X

1.15.3 BOD33 hysteresis

The BOD33 Hysteresis does not work if either an external reset or a watchdog reset occurs during the time that the Supply voltage is between VBOD- and VBOD+. If one of those resets occurs the device will continue operation if the supply voltage is above VBOD- and the reset condition is lifted.

Work Around
Instead of using the built-in hysteresis it is possible to use the BOD33 Level in the NVM User Row as an upper BOD threshold and configure the SYSCTRL->BOD33 Level bitfield to be the lower treshold and hence generating a hysteresis.

Affected Silicon Revisions

E	F	G
X	X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device Data Sheet (DS20005841E). The corrected information is shown in **BOLD** type.

- None to report at this time

3. Appendix A: Revision History

Rev C Document (02/2023)

- Fixed wording for Systick Erratum - removed reference to the Datasheet value
- Added erratum SERCOM: 1.12.14 SERCOM Wakeup
- Added erratum SERCOM: 1.12.15 SERCOM RXNACK
- Added erratum SERCOM: 1.12.16 SERCOM AACKEN
- Added erratum TC: 1.14.2 DMA Trigger

Rev B Document (08/2021)

- Adding 128 kB version of the device.
- The SPI and I^2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.
- The following Silicon errata were added in this revision:
  - ADC: 1.4.1 Offset Correction
  - DEVICE: 1.5.5 Standby Entry
  - DEVICE: 1.5.6 Standby Wake-up
  - SYSCTRL: 1.15.3 BOD33 hysteresis

Rev A Document (11/2020)

Initial release of this document.

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