PIC16F15213/14/23/24/43/44

PIC16F15213/14/23/24/43/44 Silicon Errata and Data Sheet Clarifications

The PIC16F15213/14/23/24/43/44 devices that you have received conform functionally to the current device data sheet (DS40002195**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F15213/14/23/24/43/44 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID			
		A3	A5	A6	A7
PIC16F15213	0x30E3	0x2003	0x2005	0x2006	0x2007
PIC16F15214	0x30E6	0x2003	0x2005	0x2006	0x2007
PIC16F15223	0x30E4	0x2003	0x2005	0x2006	0x2007
PIC16F15224	0x30E7	0x2003	0x2005	0x2006	0x2007
PIC16F15243	0x30E5	0x2003	0x2005	0x2006	0x2007
PIC16F15244	0x30E8	0x2003	0x2005	0x2006	0x2007

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions			
				A3	A5	A6	A7
Nonvolatile Memory (NVM)	Self-write operation	1.1.1	Self-write operation may not work above 85°C with V_{DD} above 5.3V	X			
Capture/ Compare/PWM (CCP)	PWM mode	1.2.1	Duty cycle values are incorrect	X	X	X	X
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Transmit mode	1.3.1	Possible duplicate byte transmitted	X	X	X	X
Host Synchronous Serial Port (MSSP)	Start and Stop interrupt function	1.4.1	A race condition can cause the Start and/or Stop flags to be set when I^2C is enabled	X	X	X	X
In-Circuit Serial Programming™	Low-Voltage Programming	1.5.1	Low-Voltage Programming is not possible when V_{DD} is below BORV while BOR is enabled	X	X	X	X
Watchdog Timer (WDT)	Watchdog Timer Reset	1.6.1	WDT reset may not work properly while device is not in Sleep	X	X	X	
Configuration Words (CONFIG)	Sleep	1.7.1	Waking from Sleep may cause unexpected behavior.	X	X	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Nonvolatile Memory (NVM)

1.1.1 Self-Write Operation

When performing self-write operations at 85°C or above, the writes may not occur at V_{DD} voltages above 5.3V.

Work around

Perform self-write operations at a temperature below 85°C while operating at V_{DD} voltages above 5.3V.

Affected Silicon Revisions

A3	A5	A6	A7				
X							

1.2 Module: Capture/Compare/PWM Module (CCP)

1.2.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1, while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around

None.

Affected Silicon Revisions

A3	A5	A6	A7				
X	**X**	**X**	**X**				

1.3 Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

1.3.1 Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

Method 1: Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2: Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

Affected Silicon Revisions

A3	A5	A6	A7				
X	X	X	X				

1.4 Module: Host Synchronous Serial Port (MSSP)

1.4.1 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instructions cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
SSPxCON3bits.SCIE = 0;          // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;          // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;         // Enable I2C
Delay();                        // Wait for 250 ns + 6 instruction cycles (FOSC/4)
PIRxbits.SSPxIF = 0;            // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;          // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;          // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A3	A5	A6	A7				

X	X	X	X				

1.5 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.5.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level, while BOR is enabled.

Work around

Method 1: Disable BOR to use Low-Voltage Programming.

Method 2: Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A3	A5	A6	A7				
X	X	X	X				

1.6 Module: Watchdog Timer (WDT)

1.6.1 Watchdog Timer Reset

The Watchdog Timer (WDT) Reset feature may not work properly outside of Sleep mode. Reliance on WDT Reset while executing a program is not recommended. Operation in Sleep is not impacted by this errata.

Work around

Use an independent timer to emulate a watchdog feature, outside of Sleep mode, using the following steps:

1. Configure the chosen timer for the desired timeout period
2. Enable the timer interrupt
3. Enable Peripheral and Global interrupts
4. Enable the timer, which starts the count
5. At the end of the Main loop, restore the timer values
6. If the timer interrupt occurs, issue a `RESET` command

A code example using Timer1 is shown below.

```
void __interrupt() isr(void)
{
    if( TMR1IF && TMR1IE )
    {
        asm("RESET");
    }
}

void main(void)
{
    configure_TMR1();
    GIE = 1;
    PEIE = 1;

    T1CONbits.ON = 1;

    while(1)
    {
        // user code here
```

```
            restore_TMR1();
        }
}
```

Affected Silicon Revisions

A3	A5	A6	A7				
X	X	X					

1.7 Module: Configuration Words (CONFIG)

1.7.1 Waking from Sleep May Cause Unexpected Behavior

Waking from Sleep may cause unexpected behavior.

Work around

Do not use the `SLEEP` instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

Affected Silicon Revisions

A3	A5	A6	A7				
X	X	X	X				

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002195**E**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
H	09/2022	Added silicon errata item 1.7.1.
G	07/2022	Added silicon revision A7.
F	6/2022	Updated DS revision letter to ‘E’ to match DS revision.
E	5/2022	Added silicon errata item 1.6.1.
D	10/2021	Updated Table 2. Added silicon errata items 1.2.1, 1.3.1, 1.4.1 and 1.5.1.
C	2/2021	Added silicon revision A6
B	10/2020	Adding silicon revision A5
A	9/2020	Initial document release

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