

**PIC24FJ512GU410 Family
Silicon Errata and Data Sheet Clarification**

The PIC24FJ512GU410 family devices conform functionally to the current Device Data Sheet (DS30010203D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC24FJ512GU410 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ512GU410 family silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
PIC24FJ512GL405	0x2320	A1	PIC24FJ512GU405	0x2321	A1
PIC24FJ256GL405	0x2310		PIC24FJ256GU405	0x2311	
PIC24FJ128GL405	0x2300		PIC24FJ128GU405	0x2301	
PIC24FJ512GL406	0x2324		PIC24FJ512GU406	0x2325	
PIC24FJ256GL406	0x2314		PIC24FJ256GU406	0x2315	
PIC24FJ128GL406	0x2304		PIC24FJ128GU406	0x2305	
PIC24FJ512GL408	0x2328		PIC24FJ512GU408	0x2329	
PIC24FJ256GL408	0x2318		PIC24FJ256GU408	0x2319	
PIC24FJ128GL408	0x2308		PIC24FJ128GU408	0x2309	
PIC24FJ512GL410	0x232C		PIC24FJ512GU410	0x232D	
PIC24FJ256GL410	0x231C		PIC24FJ256GU410	0x231D	
PIC24FJ128GL410	0x230C		PIC24FJ128GU410	0x230D	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the “*PIC24FJ512GU410 Family Flash Programming Specification*” (DS30010194) for detailed information on Device and Revision IDs for your specific device.

PIC24FJ512GU410 FAMILY

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A1
CCP	32-Bit ICAP mode	1.	MCCP timer in 32-Bit ICAP mode cannot be cleared by writing a zero to the Timer register.	X
I ² C	Multiple Slave mode	2.	Unexpected behavior if payload matches general call address (00h) in a multiple Slave environment.	X
I ² C	Slave Transmit	3.	Slave transmits 0xFF if ACKDT bit is set prior to transmission.	X
Oscillator	Clock Switch	4.	Clock switch to FRC+PLL does not occur after MCLR.	X
UART	Break Character Transmission	5.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.	X
Oscillator	Oscillator Trap	6.	RESET instruction in oscillator trap locks up device.	X
LCD	Frame Counter	7.	Frame counter can be written at any time.	X
Flash Security	Flash	8.	Software breakpoints in the last page of program memory can lead to an ECC double error trap generation.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

PIC24FJ512GU410 FAMILY

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A1).

1. Module: CCP

The MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.

Work around

Switch to 16-bit mode, clear both low and high words, and then go back to 32-bit mode.

Affected Silicon Revisions

A1							
X							

2. Module: I²C

In applications with multiple I²C Slaves and General Call (GCEN (I2CxCONL[7] = 1) is enabled, unexpected behavior is observed in the unaddressed Slave when the data payload of the addressed Slave matches the general call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed Slave. If Address Hold (AHEN (I2CxCONH[1] = 1) is enabled, then I²C will erroneously ACK the byte.

Work around

If Address Hold (AHEN (I2CxCONH[1] = 1) is enabled, Acknowledge Data (ACKDT (I2CxCONL[5] = 1) should be set during initialization. Instead of a Slave interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

Affected Silicon Revisions

A1							
X							

3. Module: I²C

When the Slave is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5] = 1) is set before the Slave starts transmission, the second data transmitted will be 0xFF irrespective of the actual data in I2CxTRN.

Work around

Clear the ACKDT bit before Slave transmission.

Affected Silicon Revisions

A1							
X							

4. Module: Oscillator

A clock switch to FRC+PLL after POR will cause the device to hang up if the POSC is disabled/not present and PLLSS = PRI is selected.

Work around

If POSC is disabled/not present, then PLLSS should be set to FRC. PLLSS = PRI is an invalid configuration when POSC is not present.

Affected Silicon Revisions

A1							
X							

5. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (UxSTA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A1							
X							

PIC24FJ512GU410 FAMILY

6. Module: Oscillator

When a clock failure is detected and a `RESET` instruction is executed in the oscillator trap, the device locks up if the Configuration bits set the initial clock settings to EC+PLL. WDT, POR or TMOD Resets recover the locked up device.

Work around

The device should be started from FRC (defined in the Configuration bits) and then switch to the PRI+PLL clock in application code.

Affected Silicon Revisions

A1								
X								

7. Module: LCD

The LCD Frame Counter register (LCDFC_x) can be written while the LCD Enhanced mode is active, which can impact blink and blank frame timings configured before Enhance mode was enabled.

Work around

Software should only write the FC_x register bits when LCD Frame Counter x is disabled or `ELCDEN = 0`.

Affected Silicon Revisions

A1								
X								

8. Module: Flash Security

Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.

Work around

Avoid using software breakpoints in the last page; use hardware breakpoints instead.

PIC24FJ512GU410 FAMILY

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010203D):

<p>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</p>

1. Module: Product Identification System

The package code has changed for the following package styles:

M4 = 48 lead UQFN

PT = 48 lead TQFP

MR = 64 lead VQFN

2. Module: Serial Peripheral Interface (SPI)

In SPI1CON1H bits 9:8 - AUDMOD[1:0] Audio Protocol Mode Selection bits, a "00" value selects the I²S mode.

3. Module: Timer1

In the T1CON register, TGATE is bit 6 and not bit 7.

4. Module: Electrical Characteristics

In **Table 32-11. Internal Voltage Regulator Specifications**, Parameter DVR30 Max has increased from 1.2V to 1.5V.

PIC24FJ512GU410 FAMILY

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2020)

Initial release of this document; issued for Silicon Revision A1.

Rev B Document (10/2022)

Updated data sheet revision to current DS30010203D.

Added data sheet clarifications 1 ([Product Identification System](#)), 2 ([Serial Peripheral Interface \(SPI\)](#)), 3 ([Timer1](#)) and 4 ([Electrical Characteristics](#)).

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGL00, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020-2022, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-1429-6



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Novi, MI
Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC

Tel: 919-844-7510

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto

Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820