PIC24FJ512GU410 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ512GU410 family devices conform functionally to the current Device Data Sheet (DS30010203**D**),except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ512GU410 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ512GU410 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
PIC24FJ512GL405	0x2320	A1	PIC24FJ512GU405	0x2321	A1
PIC24FJ256GL405	0x2310		PIC24FJ256GU405	0x2311	
PIC24FJ128GL405	0x2300		PIC24FJ128GU405	0x2301	
PIC24FJ512GL406	0x2324		PIC24FJ512GU406	0x2325	
PIC24FJ256GL406	0x2314		PIC24FJ256GU406	0x2315	
PIC24FJ128GL406	0x2304		PIC24FJ128GU406	0x2305	
PIC24FJ512GL408	0x2328		PIC24FJ512GU408	0x2329	
PIC24FJ256GL408	0x2318		PIC24FJ256GU408	0x2319	
PIC24FJ128GL408	0x2308		PIC24FJ128GU408	0x2309	
PIC24FJ512GL410	0x232C		PIC24FJ512GU410	0x232D	
PIC24FJ256GL410	0x231C		PIC24FJ256GU410	0x231D	
PIC24FJ128GL410	0x230C		PIC24FJ128GU410	0x230D	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ512GU410 Family Flash Programming Specification"* (DS30010194) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
CCP	32-Bit ICAP mode	1.	MCCP timer in 32-Bit ICAP mode cannot be cleared by writing a zero to the Timer register.	X
I^2C	Multiple Slave mode	2.	Unexpected behavior if payload matches general call address (00h) in a multiple Slave environment.	X
I^2C	Slave Transmit	3.	Slave transmits 0xFF if ACKDT bit is set prior to transmission.	X
Oscillator	Clock Switch	4.	Clock switch to FRC+PLL does not occur after MCLR.	X
UART	Break Character Transmission	5.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.	X
Oscillator	Oscillator Trap	6.	`RESET` instruction in oscillator trap locks up device.	X
LCD	Frame Counter	7.	Frame counter can be written at any time.	X
Flash Security	Flash	8.	Software breakpoints in the last page of program memory can lead to an ECC double error trap generation.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: CCP

The MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.

Work around

Switch to 16-bit mode, clear both low and high words, and then go back to 32-bit mode.

Affected Silicon Revisions

A1							
X							

2. Module: I^2C

In applications with multiple I^2C Slaves and General Call (GCEN (I2CxCONL[7] = 1) is enabled, unexpected behavior is observed in the unaddressed Slave when the data payload of the addressed Slave matches the general call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed Slave. If Address Hold (AHEN (I2CxCONH[1] = 1) is enabled, then I^2C will erroneously ACK the byte.

Work around

If Address Hold (AHEN (I2CxCONH[1] = 1) is enabled, Acknowledge Data (ACKDT (I2CxCONL[5] = 1) should be set during initialization. Instead of a Slave interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

Affected Silicon Revisions

A1							
X							

3. Module: I^2C

When the Slave is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5] = 1) is set before the Slave starts transmission, the second data transmitted will be 0xFF irrespective of the actual data in I2CxTRN.

Work around

Clear the ACKDT bit before Slave transmission.

Affected Silicon Revisions

A1							
X							

4. Module: Oscillator

A clock switch to FRC+PLL after POR will cause the device to hang up if the POSC is disabled/not present and PLLSS = PRI is selected.

Work around

If POSC is disabled/not present, then PLLSS should be set to FRC. PLLSS = PRI is an invalid configuration when POSC is not present.

Affected Silicon Revisions

A1							
X							

5. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (UxSTA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A1							
X							

6. Module: Oscillator

When a clock failure is detected and a RESET instruction is executed in the oscillator trap, the device locks up if the Configuration bits set the initial clock settings to EC+PLL. WDT, POR or TMOD Resets recover the locked up device.

Work around

The device should be started from FRC (defined in the Configuration bits) and then switch to the PRI+PLL clock in application code.

Affected Silicon Revisions

A1							
X							

7. Module: LCD

The LCD Frame Counter register (LCDFCx) can be written while the LCD Enhanced mode is active, which can impact blink and blank frame timings configured before Enhance mode was enabled.

Work around

Software should only write the FCx register bits when LCD Frame Counter x is disabled or ELCDEN = 0.

Affected Silicon Revisions

A1							
X							

8. Module: Flash Security

Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.

Work around

Avoid using software breakpoints in the last page; use hardware breakpoints instead.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010203**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Product Identification System

The package code has changed for the following package styles:

M4 = 48 lead UQFN

PT = 48 lead TQFP

MR = 64 lead VQFN

2. Module: Serial Peripheral Interface (SPI)

In SPI1CON1H bits 9:8 - AUDMOD[1:0] Audio Protocol Mode Selection bits, a "00" value selects the I^2S mode.

3. Module: Timer1

In the T1CON register, TGATE is bit 6 and not bit 7.

4. Module: Electrical Characteristics

In **Table 32-11. Internal Voltage Regulator Specifications**, Parameter DVR30 Max has increased from 1.2V to 1.5V.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2020)

Initial release of this document; issued for Silicon Revision A1.

Rev B Document (10/2022)

Updated data sheet revision to current DS30010203**D**.

Added data sheet clarifications 1 (Product Identification System), 2 (Serial Peripheral Interface (SPI)), 3 (Timer1) and 4 (Electrical Characteristics).

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