PIC18F26/45/46Q10

PIC18F26/45/46Q10 Silicon Errata and Data Sheet Clarifications

The PIC18F26/45/46Q10 devices you have received conform functionally to the current device data sheet (DS40001996D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/45/46Q10 silicon.

Note: This document summarizes all silicon errata issues from all silicon revisions, previous and current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID		
		A5	B0	B2
PIC18F26Q10	0x7180	0xA045	0xA0C0	0xA0C2
PIC18F45Q10	0x7140	0xA045	0xA0C0	0xA0C2
PIC18F46Q10	0x7120	0xA045	0xA0C0	0xA0C2

Important: Refer to the **Device/Revision ID** section in the current **"PIC18F2X/4XQ10 Memory Programming Specification"** (DS40001874) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				A5	B0	B2
Electrical Specifications	Sleep current	1.1.1.	Higher current after DFM write	X		
Resets	$\overline{\text{RMCLR}}$ flag	1.2.1.	POR may clear the $\overline{\text{RMCLR}}$ bit by mistake	X	X	X
Resets	LPBOR	1.2.2.	Trip point rises with temperature		X	
CWG	Auto-shutdown sources	1.3.1.	CLC2 and CLC6 not available	X		
ADCC	FVR reference	1.4.1.	Missing codes when using FVR as reference	X	X	X
ADCC	Burst average	1.4.2.	ADCNT may not increment	X		
ADCC	ADCRC (FRC) oscillator	1.4.3.	Oscillator continues to run in Sleep mode after conversion	X		
ADCC	Input slew rate	1.4.4.	Unreliable conversion results with fast falling slew rate	X	X	X
WWDT	Window operation	1.5.1.	The window feature of WWDT does not operate correctly in Doze mode	X		
NVM	NVMERR	1.6.1.	The NVMERR bit is set by device Reset after being cleared by the software	X		
NVM	Self-writes	1.6.2.	Do not write above 85°C	X		
MSSP	SPI	1.7.1.	SSPBUF may be corrupted by writes to other GPR/SFRs	X		
Oscillator	HFINTOSC	1.8.1.	5% variation over temperature range	X		
Oscillator	XT mode	1.8.2.	Maximum clock frequency limited to 2 MHz for XT mode	X	X	
In-Circuit Debug	Software breakpoints	1.9.1.	Software breakpoints are not available	X	X	X
PFM-Program Flash Memory	Self-Write	1.10.1	The first instruction following a self-write instruction may not execute.	X	X	X

Note: Only issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Electrical Specifications

1.1.1 Sleep Current - Higher Sleep Current After DFM Write Operation

The system clock will stay Active when performing a DFM write operation during Sleep mode once completing the write operation, meaning a higher Sleep current will be experienced when the device remains in this state.

Work around
Once completing the DFM write operation, wake the device up from Sleep mode and re-execute a new Sleep command.

Affected Silicon Revisions

A5	B0	B2
X		

1.2 Module: Resets

1.2.1 The $\overline{\text{RMCLR}}$ Flag in the PCON0 Register Cleared by Mistake

On an initial power-up of the device or when executing a software Reset, the $\overline{\text{RMCLR}}$ flag in the PCON0 register may be improperly cleared by a Power-on Reset (POR) or software Reset ($\overline{\text{RI}}$), thereby indicating a false $\overline{\text{MCLR}}$ event.

Work around
None.

Affected Silicon Revisions

A5	B0	B2
X	X	X

1.2.2 Low-Power Brown-out Reset (LPBOR) Mode

The Brown-out Reset trip level increases proportionally with temperature to a level where BOR is never released. LPBOR cannot be used reliably because the trip level relative to temperature is indeterminate.

Work around
Use the Normal-Power BOR mode.

Affected Silicon Revisions

A5	B0	B2

	X	

1.3 Module: Complementary Waveform Generator (CWG)

1.3.1 CWG Auto-Shutdown Sources

Shutdown sources AS6E (CLC2_out) and AS7E (CLC6_out) are unavailable.

Work around
Route the CLC output through PPS to an output pin, and use the AS0E source selection (the pin selected by CWGxPPS) and PPS controls to select the same pin as the shutdown source.

Affected Silicon Revisions

A5	B0	B2
X		

1.4 Module: Analog-to-Digital Converter with Computation (ADCC)

1.4.1 Missing Codes with FVR Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around
Method 1:

Increase the bit conversion time, known as T_{AD}, to 8 µs or higher.

Method 2:

Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A5	B0	B2
X	X	X

1.4.2 ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (ADMD = `0b011` in the ADCON2 register) while enabling noncontinuous operation and double-sampling (ADCONT = `0` in the ADCON0 register and ADDSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around
When operating the ADCC in Burst Average mode with double-sampling, enable continuous module operation (ADCONT = `1` in the ADCON0 register) and set the Stop-on-Interrupt bit (the ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in noncontinuous Burst Average mode can be operated with a single ADC conversion (ADDSEN = `0` in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A5	B0	B2
X		

1.4.3 ADCRC (FRC) Oscillator Operation in Sleep Mode

If the part is in Sleep mode and the ADCRC (FRC) oscillator is used as clock source to the ADC, the oscillator continues to run after the conversion is complete, increasing the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around
None.

Affected Silicon Revisions

A5	B0	B2
X		

1.4.4 Unreliable Conversion Results with Fast Falling Slew Rate

When the ADC input falls by greater than 3.2V, with a slew rate faster than -11 V/µs, the following ADC conversion will have the Most Significant bit (MSb) improperly set. This is likely to happen when the ADC input channel is switched from one with a high input level to another with a low input level.

Work around
When switching between input channels, discard the first conversion result after the switch. Subsequent conversions will not be affected.

Affected Silicon Revisions

A4	B0	B2
X	X	X

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Operation in Doze Mode

When enabling the Windowed operation mode in Doze mode, a window violation error is issued even though the window is open and armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around
Method 1:

Use the Windowed operation mode in any mode other than Doze. If disabling the Doze mode is not an option, use the WWDT module without enabling the window.

Method 2:

If the device is in Doze mode, perform the arming process for the window in Normal mode and return to the Doze mode.

Method 3:

If there is an Interrupt Service Routine (ISR) in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A5	B0	B2
X		

1.6 Module: Nonvolatile Memory (NVM)

1.6.1 NVMERR

When a Reset is issued while an NVM high-voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

Work around
None.

Affected Silicon Revisions

A5	B0	B2
X		

1.6.2 PFM Writes Above 85° Celsius

Do not perform write operations on the Program Flash Memory (PFM) when the temperature exceeds 85°C.

Work around
Perform PFM writes below 85°C.

Affected Silicon Revisions

A5	B0	B2
X		

1.7 Module: Host Synchronous Serial Port (MSSP)

1.7.1 MSSP SPI Client Mode

When operating in SPI Client mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF Transmit Shift Register (TSR) may become corrupted. The byte transmitted to the client cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM before an SFR read

Work around
Method 1 (Interrupt based using $\overline{SS}$):

1. Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise, check that $\overline{SS}$ == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.

4. Continue program execution.
5. When invoking the Interrupt Service Routine (ISR), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Method 2 (Bit polling based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.$\overline{SS}$ == 0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ == 0), do either of the following:
   a. Add a delay that ensures the first SCK clock will be complete, or
   b. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Once one of these two methods is complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A5	B0	B2
X		

1.8 Module: Oscillator

1.8.1 Internal HFINTOSC Oscillator Varies up to 5%

The internal HFINTOSC oscillator frequency varies up to 5% over the voltage and temperature range.

Work around

For systems requiring more precision, use an external crystal or ceramic resonator in one of the external oscillator modes.

Affected Silicon Revisions

A5	B0	B2
X		

1.8.2 Maximum Clock Frequency Limited to 2 MHz for XT Mode

The maximum clock frequency for the intermediate gain setting that supports quartz crystal and ceramic resonator operation (XT mode) is being reduced from 4 MHz to 2 MHz.

Work around

For crystal or resonator frequencies above 2 MHz, use HS mode.

Affected Silicon Revisions

A5	B0	B2
X	X	

1.9 Module: In-Circuit Debug

1.9.1 Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A5	B0	B2
X	X	X

1.10 Module: Program Flash Memory (PFM)

1.10.1 The First Instruction Following a Self-Write Instruction May Not Execute

When performing a self-write operation to Program Flash Memory, the first instruction following a self-write instruction may not execute.

Work around

Add two all-zero `NOP()` macros immediately after the self-write instruction. The all-zero `NOP()` macros are included automatically when the `#include <xc.h>` directive is used in user software.

Affected Silicon Revisions

A5	B0	B2
X	X	X

2. Data Sheet Clarifications

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
H	11/2022	Added silicon erratum item 1.10.1
G	07/2021	Removed silicon erratum item 1.4.5. Minor editorial corrections.
F	02/2021	Added silicon erratum items 1.4.5 and 1.9.1
E	11/2020	Updated the Revision ID for silicon Rev B0
D	09/2020	Added new silicon Rev B2
C	05/2020	Added new silicon Rev B0. Added issue 1.2.2 and 1.8.2.
B	05/2019	Added oscillator drift erratum. Removed data sheet clarifications.
A	03/2019	Initial document release

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