

dsPIC33CK64MP105 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK64MP105 family devices that you have received conform functionally to the current Device Data Sheet (DS70005363E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the dsPIC33CK64MP105 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on [page 7](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select Programmer > Reconnect.
 - b) For MPLAB X IDE, select Window > Dashboard and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK64MP105 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision		
		A0	A2	A4
dsPIC33CK32MP102	0x8E00			
dsPIC33CK32MP103	0x8E01			
dsPIC33CK32MP105	0x8E02			
dsPIC33CK64MP102	0x8E10			
dsPIC33CK64MP103	0x8E11			
dsPIC33CK64MP105	0x8E12	0x0000	0x0002	0x0004

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

dsPIC33CK64MP105

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A0	A2	A4
I ² C	Interrupt	1.	In Client mode, an incorrect interrupt is generated when DHEN = 1.	X	X	X
I ² C	Idle	2.	Module SFR registers are reset in Idle mode.	X	X	X
I ² C	SMBus 3.0	3.	When Configuration bit, SMB3EN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X		
Oscillator	XT, HS	4.	Removed.			
PWM	Dead Time	5.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X	X	X
UART	Frame Error	6.	FERR bit will not get set if a Stop bit is received.	X	X	X
UART	Sleep	7.	SLPEN needs to be set when waking from Sleep with a UART reception.	X	X	X
UART	Address Detect	8.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X	X	X
UART	IrDA [®]	9.	When the UART is operating in IrDA mode, the received data may be corrupted.	X	X	X
I/O	POR	10.	Spike on I/O at POR.	X		
ICSP™ Flash Write Inhibit	Flash Write Inhibit	11.	Flash memory cannot be protected against reprogramming.	X		
CPU	FLIM Instruction	12.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X	X	X
CPU	DIV.SD Instruction	13.	Overflow bit is not getting set when an overflow occurs.	X	X	X
CPU	MAXAB/MINAB/ MINZAB Instructions	14.	MAXAB, MINAB and MINZAB do not work for different sign operands.	X	X	X
CPU	Byte Mode Instructions	15.	Upper byte of the destination register may not be persistent.	X	X	X
DMA	ADC Triggers	16.	DMA is triggered continuously from ADC.	X		
I ² C	I ² C	17.	All instances of I ² C may exhibit errors and should not be used.	X	X	
Oscillator	VCO and AVCO Dividers	18.	Main and auxiliary PLL external VCO dividers can fail to output the clock.	X	X	
Reset	BOR	19.	BOR may stop functioning when VDD drops in the window between the BOR level and BOR-25 mV.	X	X	
Reset	BOR	20.	BOR may periodically cause device Resets when the VDD is in a window between the BOR level and BOR-25 mV.	X	X	X

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A4).

1. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Client interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

2. Module: I²C

In Client mode, the SFRs are reset when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

3. Module: I²C

When selecting SMBus 3.0 operation using Configuration bit, SMB3EN (FDEVOPT[10]), the Voltage Input High (VIH) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X							

4. Module: Oscillator

This errata is no longer applicable to any silicon revisions of this product. See **Section 2.5 External Oscillator Pins** in the current device data sheet for guidance on oscillator design to avoid start-up related issues.

5. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

6. Module: UART

When UART is operating with STSEL[1:0] = 2, (two Stop bits sent, two checked at receive) and STPMD = 0, the FERR bit will not get set if a Stop bit is received.

Work around

Use STPSEL = 3 instead of STSEL = 2. When operating with STSEL = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

7. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

dsPIC33CK64MP105

8. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

9. Module: UART

When the UART is operating in IrDA® mode, the received data may be corrupted.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

10. Module: I/O

At device power-up, the I/O pins may drive a pulse up to 0.8V for a duration of up to 100 μ Sec.

Work around

It is recommended to ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 μ Sec later than powering the dsPIC® DSC to avoid the issue.

Behavior is specific to each part and not affected by aging.

Affected Silicon Revisions

A0	A2	A4					
X							

11. Module: ICSP™ Flash Write Inhibit

The ICSP Write Inhibit feature does not prevent ICSP Flash erase and program operations, even if the lock values are written.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X							

12. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

13. Module: CPU

When using the Signed 32-by-16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the div.sd instruction.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

14. Module: CPU

When operating on signed operands of different sign values, the output for MAXAB, MINAB and MINZAB instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

15. Module: CPU

When using Byte mode instructions, the upper byte of the destination register may not be persistent.

Work around

None.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

16. Module: DMA

The DMA receives multiple continuous triggers from ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A0	A2	A4					
X							

17. Module: I²C

All instances of I²C/SMBus may exhibit errors and should not be used. When operating I²C/SMBus in a noisy environment, the I²C module may exhibit various errors. These errors may include, but are not limited to, corrupted data, unintended interrupts or the I²C bus getting hung up due to injected noise. Examples of system noise include, but are not limited to, PWM outputs or other pins toggled at high speed adjacent to the I²C pins. Both Host and Client I²C/SMBus modes may exhibit this issue.

Work around

If I²C is required, use a software I²C implementation. An example I²C software library is available from Microchip:

www.microchip.com/dsPIC33C_I2C_SoftwareLibrary

Affected Silicon Revisions

A0	A2	A4					
X	X						

18. Module: Oscillator

At PLL start-up, the main and auxiliary PLL VCO dividers may occasionally halt and not provide a clock output. The VCO and AVCO dividers can be selected as clock sources for different peripheral modules, including the ADC, PWM, DAC, UART, etc. VCO and AVCO dividers, Fvco/2, Fvco/3, Fvco/4, FVCODIV, AFvco/2, AFvco/3, AFvco/4 and AFVCODIV outputs, are affected.

Work around

1. Use another clock source, such as the Fosc, PLL or APLL output (FPLLO and AFPLLO) instead of the VCO or AVCO dividers.
2. If the application requires the VCO or AVCO divider, test this clock source. System resources, such as a timer, I/O pin state or interrupts can be used to detect and verify peripheral activity for presence of the VCO divider clock output. Any type of Reset may recover the VCO divider clock (Software Reset, WDT, MCLR or POR).

Affected Silicon Revisions

A0	A2	A4					
X	X						

19. Module: Reset

After start-up, if VDD decreases to a value between VBOR-25 mV and VBOR, the BOR may be unintentionally disabled. The device may incorrectly operate down to 2.0V. However, while operating at a VDD between 3-3.6V, the device will operate as expected. The VBOR specification is listed in the "Electrical Characteristics" section in the device data sheet.

Work around

An external voltage monitor IC may be used as a work around. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A0	A2	A4					
X	X						

dsPIC33CK64MP105

20. Module: Reset

If VDD is between VBOR-25 mV and VBOR, a BOR Reset may repeatedly occur. However, while operating at a VDD between 3-3.6V, the device will operate as expected. The VBOR specification is listed in the “**Electrical Characteristics**” section in the device data sheet.

Work around

An external voltage monitor IC may be used as a work around. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A0	A2	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005363E):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (1/2019)

Initial version of this document; issued for revision A0.

Rev B Document (2/2019)

Updated device data sheet revision from B to C.

Rev C Document (3/2019)

Added silicon issue 16 ([DMA](#)).

Rev D Document (1/2020)

Added silicon issue 17 ([I²C](#)).

Rev E Document (6/2020)

Added silicon issue 18 ([Oscillator](#)).

Removed silicon issue 4 ([Oscillator](#)) since it is no longer applicable.

Rev F Document (7/2020)

Added silicon revision A2.

Rev G Document (2/2020)

Added silicon issues 19 ([Reset](#)) and 20 ([Reset](#)).

Added A2 to affected silicon revisions in silicon issue 17 ([I²C](#)).

The I²C standard uses the terminology “*Master*” and “*Slave*.” The equivalent Microchip terminology used in this document is “*Host*” and “*Client*”, respectively.

Rev H Document (6/2022)

Added silicon revision A4.

Updated silicon issues 19 ([Reset](#)) and 20 ([Reset](#)).

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, Optolyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, QuietWire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019-2022, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-0553-9



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Novi, MI
Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC

Tel: 919-844-7510

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto

Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
China - Beijing
Tel: 86-10-8569-7000
China - Chengdu
Tel: 86-28-8665-5511
China - Chongqing
Tel: 86-23-8980-9588
China - Dongguan
Tel: 86-769-8702-9880
China - Guangzhou
Tel: 86-20-8755-8029
China - Hangzhou
Tel: 86-571-8792-8115
China - Hong Kong SAR
Tel: 852-2943-5100
China - Nanjing
Tel: 86-25-8473-2460
China - Qingdao
Tel: 86-532-8502-7355
China - Shanghai
Tel: 86-21-3326-8000
China - Shenyang
Tel: 86-24-2334-2829
China - Shenzhen
Tel: 86-755-8864-2200
China - Suzhou
Tel: 86-186-6233-1526
China - Wuhan
Tel: 86-27-5980-5300
China - Xian
Tel: 86-29-8833-7252
China - Xiamen
Tel: 86-592-2388138
China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
India - New Delhi
Tel: 91-11-4160-8631
India - Pune
Tel: 91-20-4121-0141
Japan - Osaka
Tel: 81-6-6152-7160
Japan - Tokyo
Tel: 81-3-6880- 3770
Korea - Daegu
Tel: 82-53-744-4301
Korea - Seoul
Tel: 82-2-554-7200
Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906
Malaysia - Penang
Tel: 60-4-227-8870
Philippines - Manila
Tel: 63-2-634-9065
Singapore
Tel: 65-6334-8870
Taiwan - Hsin Chu
Tel: 886-3-577-8366
Taiwan - Kaohsiung
Tel: 886-7-213-7830
Taiwan - Taipei
Tel: 886-2-2508-8600
Thailand - Bangkok
Tel: 66-2-694-1351
Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393
Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829
Finland - Espoo
Tel: 358-9-4520-820
France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79
Germany - Garching
Tel: 49-8931-9700
Germany - Haan
Tel: 49-2129-3766400
Germany - Heilbronn
Tel: 49-7131-72400
Germany - Karlsruhe
Tel: 49-721-625370
Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44
Germany - Rosenheim
Tel: 49-8031-354-560
Israel - Ra'anana
Tel: 972-9-744-7705
Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781
Italy - Padova
Tel: 39-049-7625286
Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340
Norway - Trondheim
Tel: 47-7288-4388
Poland - Warsaw
Tel: 48-22-3325737
Romania - Bucharest
Tel: 40-21-407-87-50
Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91
Sweden - Gothenberg
Tel: 46-31-704-60-40
Sweden - Stockholm
Tel: 46-8-5090-4654
UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820