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Consider the JFET When You Have a Priority Performance Objective

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Introduction

Though not as well known as the bipolar transistor or op amp, this long-established transistor still excels in where you need to optimize circuit behavior, such as for lowest noise.

Many engineers are somewhat familiar with discrete bipolar transistors, such as the venerable 2N2222. They are also comfortable with the MOSFET (metal-oxide semiconductor field-effect transistor) as a discrete device for amplifying analog signals and switching power signals, as well as its role as the key digital structural element in large-scale ICs.

But alongside these devices is the JFET (junction field-effect transistor), which was developed soon after the bipolar transistor. To many designers, the JFET is the nearly ideal three-terminal solid-state device, and its operation and parameters are analogous to the vacuum-tube triode. The difference is that the JFET is, of course, a low-voltage, much-more efficient device, although it can't deliver the power that a vacuum tube can. For applications which require extremely low noise, the JFET is often offers superior performance compared to any other discrete device, as well as op amps.

JFET Structure and Operation

Figure 1. Illustrates the cross section of an n-channel JFET.

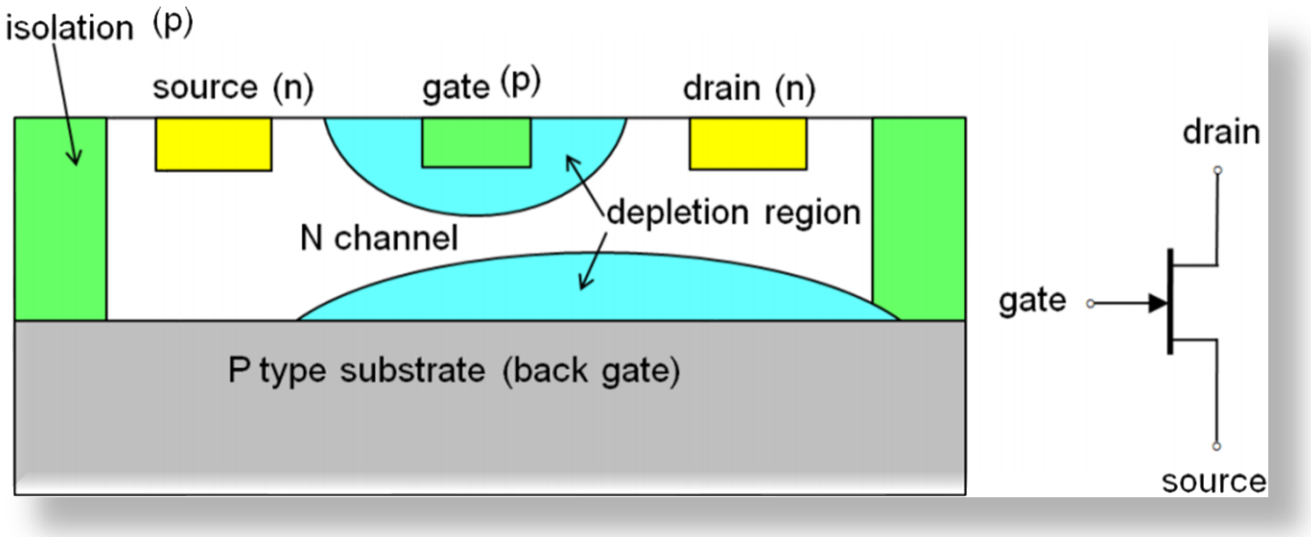


Figure 1 N-channel JFET Cross Section

In this device, there is a conducting, majority-carrier n channel between the source (where majority carriers enter the n-type material) and the drain (where majority carriers leave the material). By applying a negative voltage to the p+ gate, the depletion area widens with reverse bias. It then begins to restrict the flow of electrons between the source and the drain; it's as if a garden hose is being squeezed. When the gate voltage becomes sufficiently negative, the channel pinches off (symbolized by VP), and the current flow decreases to zero.

Note: Some current flows even with zero gate-source voltage VGS at larger values of drain-source voltage VDS. The basic input/output relationship for VGS = 0V, gate and source are connected to each other, as illustrated in **Figure 2**.

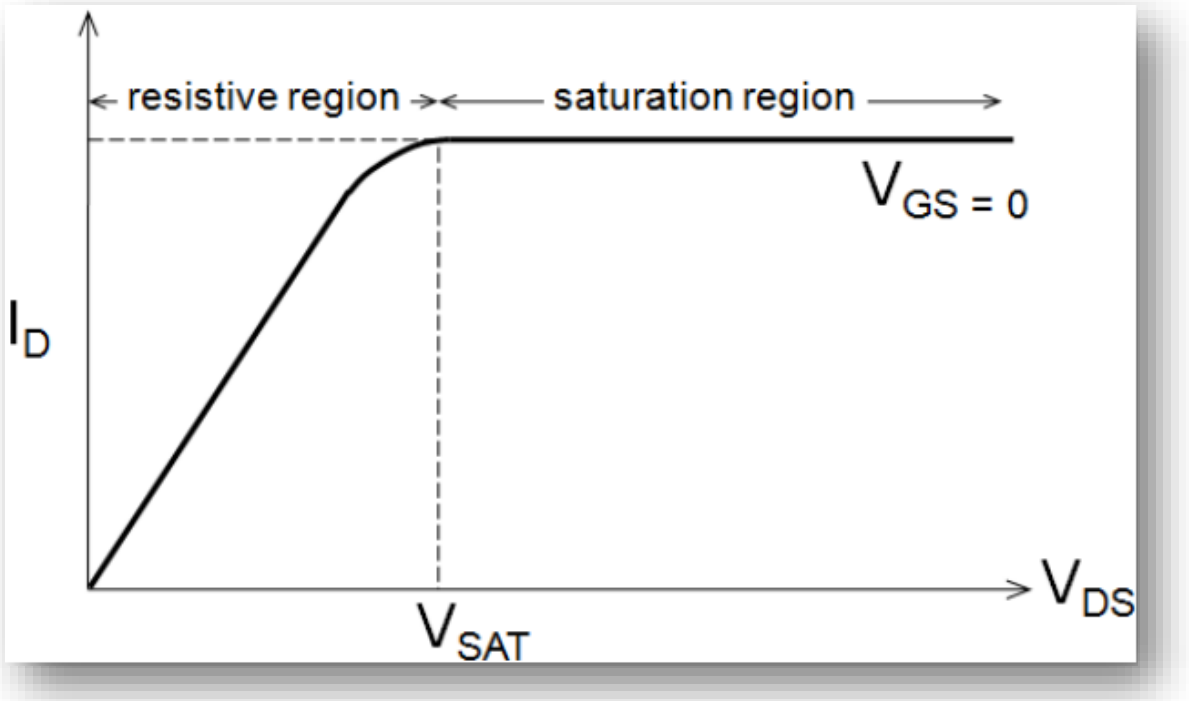


Figure 2 V VGS = 0V Basic Input/Output Relationship

There are two main operating regions:

1. Resistive region (left)
2. Saturation region (right)

In the resistive region on the left, the JFET is operating below its saturation voltage, and an increase in drain-source voltage VDS produces an increase in drain current ID which is very nearly linear. At VDS values above VSAT, there is no increase in ID.

The current flow through the JFET channel is determined by both VDS and VGS, but when VDS is greater than the saturation voltage VSAT—where an increase in VDS does not result in a further increase in drain current ID—then the channel current is determined solely by VGS.

While **Figure 2**. illustrates a single curve, what designers really use is a graph with a family of curves, **Figure 3**.

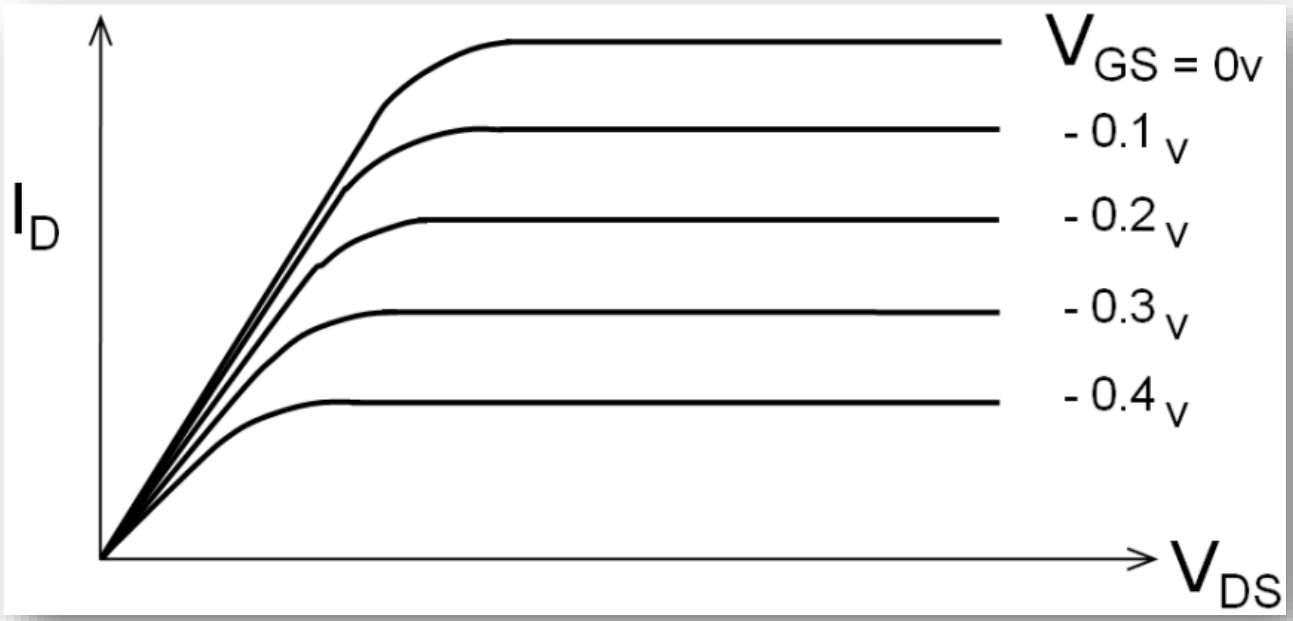


Figure 3 ID Versus VGS

This graph shows ID versus VGS for a set of values of VGS beginning at 0V, and then going increasingly negative in steps, usually with step size of 0.1V or 0.2V.

If you're familiar with the bipolar transistor, you know that its base is forward biased and conducts a base current. In contrast, the p-n junction of the JFET is reverse-biased and the gate current is zero. The result is that the bipolar transistor is a low-impedance device, while the JFET is inherently a high-impedance device.

JFETs and Noise

One area where JFETs can provide clear designer benefit is in audio-band noise, for both conventional audio as well as instrumentation amplifiers for low-frequency, highly sensitive sensors and transducers. The noise model of a JFET, Figure 4. shows the equivalent voltage and current noise sources. The current-noise effect depends on the source impedance RS, while the voltage noise (referred to input) is independent of that impedance.

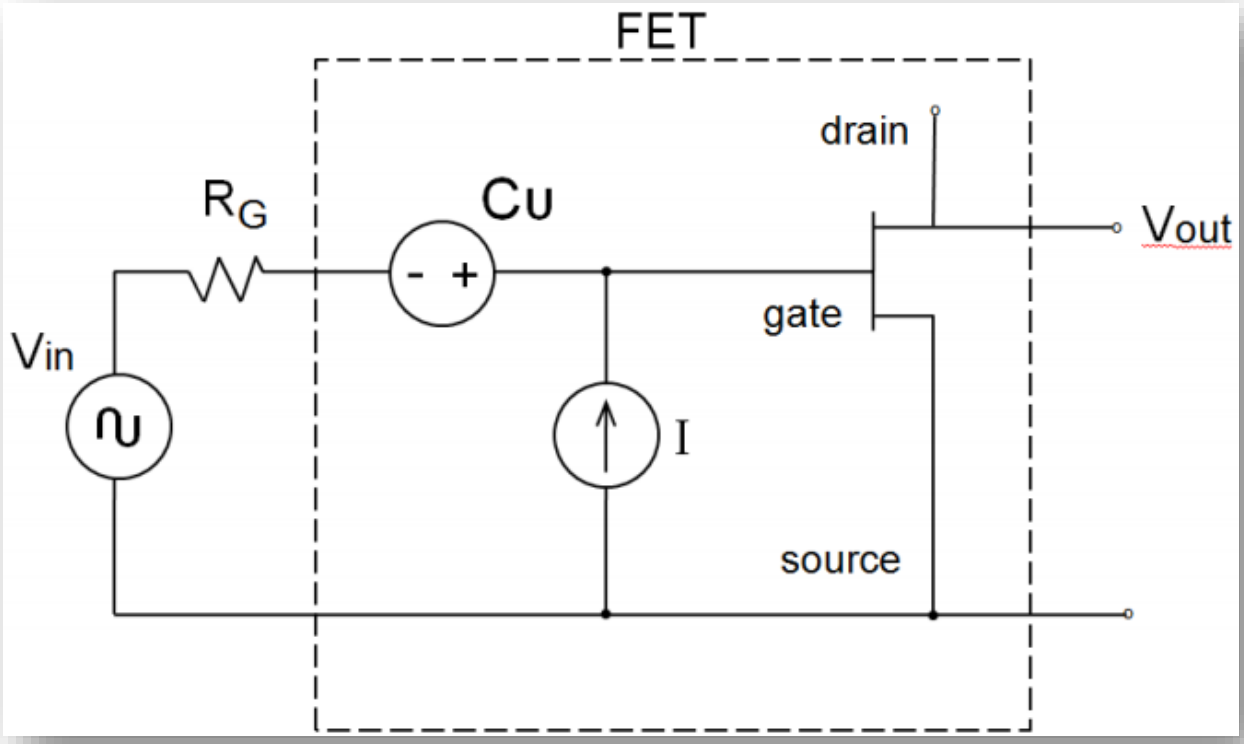


Figure 4 Equivalent Voltage and Current Noise Sources

The JFET has three overlapping noise types; their relative proportions change with frequency:

- Excess or flicker noise, properly called 1/fn , but more often referred to as 1/f noise, is the result of thermally generated reverse current in the gate channel junction; it is usually negligible in low-noise JFETs.
- Thermal noise, also called Johnson or Nyquist noise, is generated in the resistive channel of the JFET; the equivalent short-circuit noise voltage is characterized by the classic value √(4kTRNB) where K is Boltzmann's constant, T is temperature (Kelvin), RN is the equivalent resistance for noise, and B is bandwidth.
- Shot or generator recombination noise, which is related to the flow of current into the gate-source impedance.

What concerns most designers is the JFET noise figure (NF). NF is defined with respect to a reference standard, the generator resistance RG:

NF (in dB) = 10 log10 [1 + ((en2 + in2RG2)/4kTRGB)] where RG is a source resistor added to the circuit.

To determine the lowest noise figure for critical circuits, take the derivative of the NF equation and set it to zero. The result is that for minimum noise, source resistor RG should be set to be equal to en/in. While en will be at a minimum for JFETs when the device is operated at VGS = 0, both en and in vary only slightly as ID changes. In contrast, en and in vary directly with the collector current in bipolar transistors.

In general, JFETs can yield noise figures below 1 dB even in circuits with higher source impedances, reaching up to RG = 1 GΩ. Bipolar transistors will have NFs which are substantially higher, in the range of 5 dB or more.

Other JFET Considerations

Input capacitance of JFETs is relatively high, which will affect frequency response. This capacitance has two components: Ciss, the basic input capacitance, and Crss, the reverse transfer capacitance. While Crss is much lower than Ciss, it is magnified by the Miller effect and thus has a larger impact on overall input capacitance as seen by the source. To reduce this effective input capacitance, designers sometimes use the cascade configuration, which has been used since the days of vacuum tubes.

Temperature coefficient and temperature-induced drift are another related pair of concerns in low-noise, precision designs. It is possible to design the circuit to operate at the single point of zero tempco, which can be calculated by analysis based on the values of VGS and VP versus temperature. However, this approach is both technically difficult and often impractical, since the circuit's operating temperature is often not constant or controllable.

A better approach is based on using a different circuit topology. In place of the basic single-ended amplifier, designers can use a differential design, also called a balanced design. In this approach, two amplifiers are symmetrically configured as "half-circuits" and work both with and against each other. The consequence of this design is that any signals which are common to both half circuits are largely cancelled, characterized by common-mode rejection ratio (CMRR) or common-mode gain (CMG), both in dB; the higher the CMRR or lower the CMG, the better.

This approach works to counter tempco-related drift because changes in JFET parameters such as ID, VGS, and conductance are seen by the configuration as being common-mode signals and thus cancelled. But to make it work to the maximum extent, the two JFETs themselves must have characteristics which are as nearly identical as possible.

There are two ways to achieve this. The first approach is to take a large number of JFETs, test them, and then pair them up as closely as possible. While this is possible in theory and can work in low-volume or custom projects, it is often impractical in practice, especially in a manufacturing or field-repair environment.

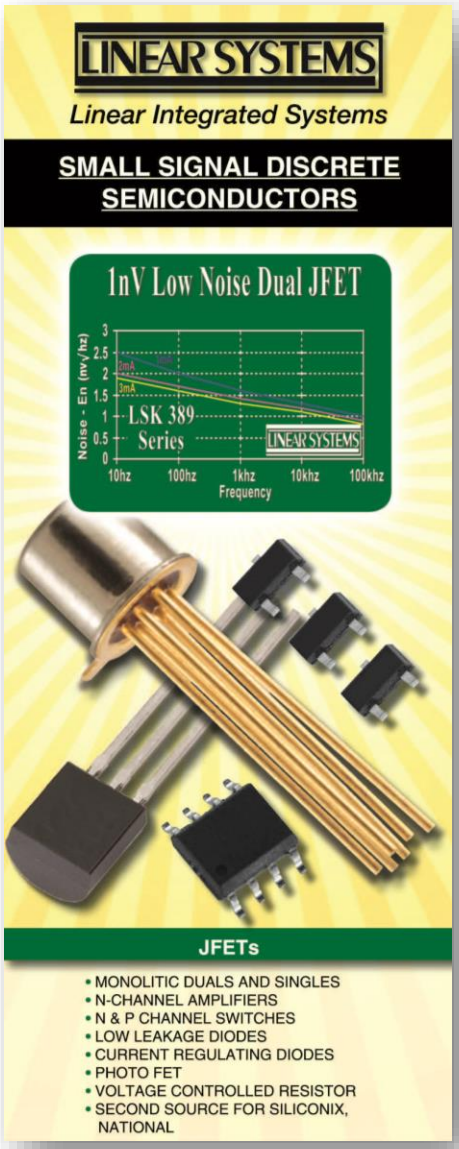
A better approach is to use dual monolithic JFETs, where the die contains two devices. Such dual devices inherently usually have nearly identical performance parameters, including their various drift coefficients. Examples of such dual devices include the LSK389 ultra-low noise, monolithic, n-channel JFET pair and LSK489 low-noise, low-capacitance, n-channel JFET pair, both available from Linear Integrated Systems (Fremont, CA).

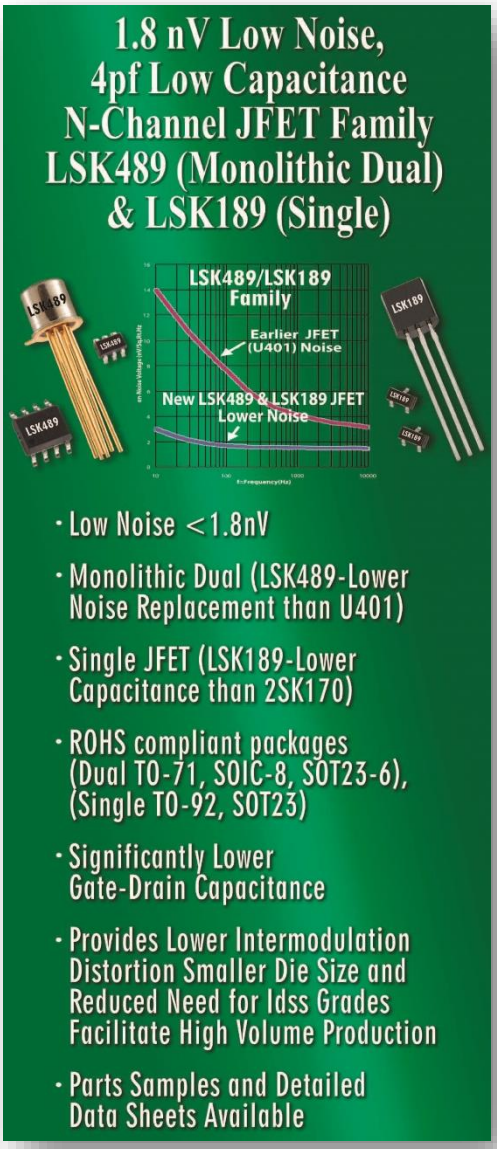
The LSK389 has lower noise than the LSK489, and while the LSK489's noise is almost as low, it also has much lower typical gate-to-drain capacitance of just 4 pF, compared with 25 pF for the LSK389. Although the noise difference between the two JFETs is not significant for most designs, the lower gate-to-drain capacitance is very important, as the higher capacitance can cause intermodulation distortion (IMD) in some designs.

This lower capacitance results in a much-wider-bandwidth front end for the audio op amp, while also reducing the IMD that the op amp will see.

Conclusion

There are many good, high-performance bipolar transistors, and even op amps, available on the market, no doubts about that. But for applications where the designer is really striving to achieve the highest level of performance in one or two parameters, the JFET can provide the flexibility in specifications, configuration, topology, and associated components needed to achieve these goals.





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