Product Bulletin

Document #:PB27296Z
Issue Date:15 Feb 2026

Title of Change:	Updated Parameter Definitions for LV8907UWR2G
Effective date:	15 Feb 2026
Contact information:	Contact your local onsemi Sales Office
Type of notification:	This Product Bulletin is for notification purposes only. onsemi will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

onsemi Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

This Product Bulletin is being issued to inform customers of corrections made to the datasheet of LV8907UWR2G. Several parameters within the document were previously described with unclear or incorrect definitions, particularly the voltage range notation, LIN communication parameter settings, and missing bit descriptions in the SPI register map. These updates are intended to improve clarity and ensure accurate interpretation of the device specifications.

Correction of Unclear Voltage Range Parameter Definitions

Before

Duty Cycle 1	D1	Threcmax = 0.744VS Thdommax = 0.581VS VS = 7.0 V &18 V, tbit = 50 µs D1 = tBusrecmin / (2×tbit)	0.396		0.5	
Duty Cycle 2	D2	Threcmin = 0.422VS Thdommin = 0.284VS VS = 7.6 V &18 V, tbit = 50 µs D1 = tBusrecmax / (2×tbit)	0.5		0.581	
Duty Cycle 3	D3	Threcmax = 0.778VS Thdommax = 0.616VS VS = 7.0 V &18 V, tbit = 96 µs D1 = tBusrecmin / (2×tbit)	0.417		0.5	
Duty Cycle 4	D4	Threcmin = 0.389VS Thdommin = 0.251VS VS = 7.6 V &18 V, tbit = 96 µs D1 = tBusrecmax / (2×tbit)	0.5		0.59	

Low Slope Rise Time	T_rise_low	VS = 12 V, LINSLP = 0, L3 (Note 6)			62	µs
Low Slope Fall Time	T_fall_low	VS = 12 V, LINSLP = 0, L3 (Note 6)			62	µs

GSDAT[7:0]

Bit7	6	5	4	3	2	1	Bit0	
ORBEN	STUPO	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]		
						0	0	Sleep mode (MRACK[7:0] = FFh)
						0	1	Device start up time
						1	0	Standby mode
						1	1	Normal mode (MRACK [7:0] = 55h)
0	×	×	0	0	0	×	×	Normal Operation
					1			OTP busy with read/write access
				1				Latched shutdown condition
			1					Failure Condition
		0						Last SPI access OK
		1						Last SPI access failed*
	1							Startup mode
1								OTP integrity test mode

After

Duty Cycle 1	D1	Threcmax = 0.744VS Thdommax = 0.581VS VS = 7.0 V...18 V, tbit = 50 µs D1 = tBusrecmin / (2×tbit)	0.396		0.5	
Duty Cycle 2	D2	Threcmin = 0.422VS Thdommin = 0.284VS VS = 7.6 V...18 V, tbit = 50 µs D1 = tBusrecmax / (2×tbit)	0.5		0.581	
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Low Slope Rise Time	T_rise_low	VS = 12 V, LINSLP = 1, L3 (Note 6)			62	µs
Low Slope Fall Time	T_fall_low	VS = 12 V, LINSLP = 1, L3 (Note 6)			62	µs

GSDAT[7:0]

Bit7	6	5	4	3	2	1	Bit0	
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						1	0	Standby mode
						1	1	Normal mode (MRACK [7:0] = 55h)
0	×	×	0	0	0	×	×	Normal Operation
					1			OTP busy with read/write access
				1				Latched shutdown condition
			1					Failure Condition
		0						Last SPI access OK
		1						Last SPI access failed*
	0							Motor in Startup mode
	1							Motor in Normal drive mode
1								OTP integrity test mode

Lin communication parameters

SPI register map

All these changes have no impact on the OPN functionality.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

LV8907UWR2G		