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PCN Number:	20260716001.1A	PCN Issued	July 27, 2026
Qualification of RFAB using qualified Process Technology, Datasheet and BOM options for select devices		Sample request deadline:	September 25, 2026
		Estimated 1st ship date:	October 25, 2026
Sample requests received after September 25, 2026 will not be supported.			

Change Type(s)	Datasheet Design Packing/Shipping/Labeling Wafer Fab Site Wafer Fab Material Wafer Fab Process Assembly Site Assembly Process Assembly Material
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PCN Details

Description of Change:

Texas Instruments is pleased to announce the addition of RFAB using the LBC9 qualified process technology, and assembly BOM options for the devices listed below.

Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter
DL-LIN-2	LBC3	200 mm	RFAB	LBC9	300 mm

The die was also changed as a result of the process change.

Construction differences are as follows:

Assembly Site	MLA	CDAT
Bond wire composition, diameter	Cu, 1.98 mil	Cu, 1 mil
Mount Compound	4205846	4207123
Mold Compound	4208625	4222198

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below:



TPS796
SLVS351R – SEPTEMBER 2002 – REVISED JANUARY 2026

Changes from Revision Q (June 2025) to Revision R (January 2026)

Page

- added DRB thermal information for "new chip"..... 5

Changes from Revision P (January 2015) to Revision Q (June 2025)

Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed device name to condensed *TPS796* to consolidate all voltage option devices under one device name..... 1
- Changed entire document to align with current family format..... 1
- Added new silicon (M3) devices to document..... 1
- Added nomenclature distinguishing between new chip and legacy chip information throughout document..... 1
- Changed *Features, Applications, and Description* sections..... 1
- Changed *Pin Configuration and Functions* section..... 3
- Added new silicon curves to *Typical Characteristics* section 8
- Added new chip block diagrams to *Functional Block Diagrams* section..... 14
- Added *Active Discharge (New Chip)* section..... 16
- Changed *Shutdown* section..... 16
- Changed *Undervoltage Lockout (UVLO)* section..... 16
- Changed *Regulator Protection* section and added subsections..... 17
- Added steady dropout state discussion in second paragraph to *Dropout Operation* section..... 19
- Added subsections to *Application Information* 20
- Changed *Design Parameters* table..... 25
- Changed *Detailed Design Procedure* section..... 25
- Changed *Application Curves* section..... 26
- Changed title from *Do's and Don'ts* to *Best Design Practices* 26
- Added *Estimating Junction Temperature* section..... 26
- Added M3 information to *Available Options* table..... 31

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
TPS796	SLVS351R	SLVS351Q	http://www.ti.com/product/TPS796

The datasheet also provides more information on the performance differences between the LBC9 chip (new chip) and the LBC3 chip (legacy chip). See below example for TPS796:

5.5 Electrical Characteristics

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{V}^{(1)}$, $I_{OUT} = 1\text{mA}$, and $C_{OUT} = 10\mu\text{F}$ and $C_{NR} = 0.01\mu\text{F}$ (Legacy Chip only), unless otherwise noted. All typical values at $T_J = 25^{\circ}\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	Legacy chip		5.5	V
		New chip		6.0	
V_{FB}	Internal reference (TPS79601)	1.2	1.225	1.25	V
I_{OUT}	Continuous output current	0		1	A
V_{OUT}	Output voltage range (TPS79601)	1.225		5.5V _{DO}	V
V_{OUT}	Output accuracy	TPS79601 (legacy chip)	$0\mu\text{A} \leq I_{OUT} \leq 1\text{A}$, $V_{OUT(nom)} + 1\text{V} \leq V_{IN} \leq 5.5\text{V}^{(1)}$	$0.98V_{OUT(nom)}$	%
		TPS79601 (new chip)	$0\mu\text{A} \leq I_{OUT} \leq 1\text{A}$, $V_{OUT(nom)} + 1\text{V} \leq V_{IN} \leq 5.5\text{V}^{(1)}$	$1.02V_{OUT(nom)}$	

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT ⁽¹⁾	DESCRIPTION
TPS796xx(x)yyy z M3	xx(x) is the nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). yyy is the package designator. z is the package quantity. M3 is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are part of our multiyear plan to transition products from our 200-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

Anticipated impact on Form, Fit, Function, Quality or Reliability:

- These devices include new die with schematic or behavior changes.
- There are changes in the electrical tables.
- Device quality has been impacted.
- Review updated datasheets and/or the Standard Data Packet for more details on the changes. Evaluating samples is encouraged.

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Fab Site Information

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DL-LIN	DLN	USA	Dallas
RFAB	RFB	USA	Richardson

Die Rev:

Current **New**

Die Rev [2P]	Die Rev [2P]
A	A

Assembly Site Information

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
MLA	MLA	MYS	KUALA LUMPUR
CDAT	CDA	CHN	Chengdu

Sample product shipping label (not actual product label):



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Products Affected:

TPS79650DRBR	TPS79650DRBT	TPS79650DRBTG4	
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Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: TPS79650DRBR	QBS Package Reference: CAXC8T245QRHLRQ1	QBS Process Reference: BQ79600PWRQ1	QBS Package Reference: TPS7B8550QWDRCRQ1	QBS Product Reference: TPS79501QDRBRM3Q1	QBS Product Reference: TPS79601DRBRM3
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-	1/77/0	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	3/231/0	-	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	3/231/0	-	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	3/231/0	-	3/231/0	-	-
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	3/135/0	-	1/77/0	-	-
HTSL	A6	High Temperature Storage Life	Per QSS-009-018	1 Step	-	-	-	1/77/0	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	3/231/0	-	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	1/15/0	-	-

Type	#	Test Name	Condition	Duration	Qual Device: TPS79650DRBR	QBS Package Reference: CAXC8T245QRHLRQ1	QBS Process Reference: BQ79600PWRQ1	QBS Package Reference: TPS7B8550QWDRCRQ1	QBS Product Reference: TPS79501QDRBRM3Q1	QBS Product Reference: TPS79601DRBRM3
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	1/15/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	3/30/0	-	3/30/0	1/10/0	-
ESD	E2	ESD CDM	-	250 Volts	1/3/0	-	-	-	1/3/0	-
ESD	E2	ESD HBM	-	1000 Volts	1/3/0	-	-	-	1/3/0	-
LU	E4	Latch-Up	Per JESD78	-	1/3/0	-	-	-	1/3/0	-
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	-	-	-	1/30/0	-
FTY	E6	Final Test Yield	-	-	1/All/0	-	-	-	1/All/0	1/All/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device TPS79650DRBR is qualified at MSL2 260C
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2503-071

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification

by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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