12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN#20241112000.1
Qualification of new fab (RFAB), Die shrink &/or BOM options for select devices
Change Notification / Sample Request

Date: November 13, 2024
To: MOUSER PCN

Dear Customer:

This is an announcement of a change to a device that is currently offered by Texas Instruments. The details of this change are on the following pages.

Texas Instruments requires acknowledgement of receipt of this notification within **30** days of the date of this notice. Lack of acknowledgement of this notice within 30 days constitutes acceptance and approval of this change. If samples or additional data are required, requests must be received within **30 days** of this notification.

The changes discussed within this PCN will not take effect any earlier than the proposed first ship date on Page 3 of this notification, unless customer agreement has been reached on an earlier implementation of the change.

This notice does not change the end-of-life status of any product. Should product affected be on a previously issued product withdrawal/discontinuance notice, this notification does not extend the life of that product or change the life time buy offering/discontinuance plan.

For questions regarding this notice or to provide acknowledgement of this PCN, you may contact your local Field Sales Representative or the change management team.

For sample requests or sample related questions, contact your local Field Sales Representative.

Sincerely,

Change Management Team
SC Business Services

20241112000.1
Attachment: 1

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records, you have recently purchased these devices. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
UCC21540DWR	595-UCC21540DWR
UCC21540DWKR	NULL
UCC21220ADR	UCC21220ADR
UCC21530DWKR	UCC21530DWKR
UCC21540ADWKR	UCC21540ADWKR
UCC21520DWR	UCC21520DWR
UCC21220DR	UCC21220DR
UCC21520ADWR	UCC21520ADWR
UCC21540ADWR	NULL
UCC21222DR	UCC21222DR

Technical details of this Product Change follow on the next page(s).

PCN Number:	20241112000.1	PCN Date:	November 13, 2024
Title:	Qualification of new fab (RFAB), Die shrink &/or BOM options for select devices		
Customer Contact:	Change Management Team	Dept:	Quality Services
Proposed 1st Ship Date:	February 11, 2025	Sample requests accepted until:	December 13, 2024*

***Sample requests received after December 13, 2024 will not be supported.**

Change Type:

☐	Assembly Site	☒	Design	☐	Wafer Bump Material
☒	Assembly Process	☐	Data Sheet	☐	Wafer Bump Process
☒	Assembly Materials	☐	Part number change	☒	Wafer Fab Site
☐	Mechanical Specification	☐	Test Site	☒	Wafer Fab Material
☒	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the change to a new design in RFAB using the LBC8LVISO.2 qualified process technology and additional BOM options for the list of devices below. This fab information comparision table is only for the Group 1 devices:

Current Fab Site			Additional Fab Site		
Current Fab Site	**Process**	**Wafer Diameter**	**Additional Fab Site**	**Process**	**Wafer Diameter**
MIHO8/DP1DM5	LBC8LVISO.1	200 mm	RFAB	LBC8LVISO.2	300 mm

The die were also changed as a result of this process change.

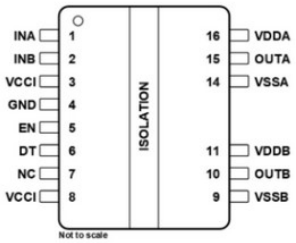
Construction differences are as follows (Group 1 & Group 2 devices):

	Current	New
Bond wire diam/type	0.96mil Au, 1.0mil Cu	0.8mil Cu

This particular PCN is related to TI's transition of dual-channel isolated gate drivers to a newly-designed circuit and to TI's most efficient manufacturing processes and technology. The newly-designed circuit includes improvements to robustness in common automotive and industrial applications. Changes in the datasheet are summarized in the table below. TI additionally offers a transition guide to ensure
complete understanding of system considerations which is available upon request in the SDP (supporting data package). The changes to the manufacturing processes and technology underscore our commitment to product longevity and supply continuity.

Design change considerations for new UCC21530 Si

- Critical gate driving parameters **don't change**:
  - Max drive current: +4A/-6A
  - Improved VDDx power up delay
  - Propagation delay can be addressed by application

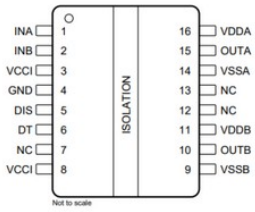


DWK Package 14-Pin SOIC

PARAMETER		UCC21530 (current Si)	UCC21530 (new Si)
Isolation	CMTI	100V/ns (min)	125V/ns (min)
Input Stage	VCCI rec. operating range	3.0V – 18V	3.0V – 18V
	ICC switching MAX	2.0mA (typ) (500 kHz)	3mA (typ) (500 kHz)
	EN pin structure	Internal pull up	Internal pull up
Output Driver	VDDx rec. operating range	8V UVLO version: 9.2V – 25V 12V UVLO version: 14.7V – 25V	8V UVLO version: 9.2V – 25V 12V UVLO version: 13.5V – 25V
	Max Drive Current TYP	+4A/-6A	+4A/-6A
	VDDx Power-up Delay MAX	100us	10us
	IDDx Quiescent Current TYP	1.8mA	2.5mA
Timing	Prop Delay MIN, MAX	14ns, 30ns	26ns, 45ns
	CHA-CHB Delay Matching MAX	<5ns	<5ns (Tj = -10C to +150C) <6.5ns (Tj = -40C to -10C)
	Dead Time range	5-5000ns	10-3000ns
	Deadtime Accuracy	20%	20%
Temperature	Tj Recommended Max	130°C	150°C

Design change considerations for new UCC21520 Si

- Critical gate driving parameters **don't change**:
  - Max drive current: +4A/-6A
  - Improved VDDx power up delay
  - Propagation delay can be addressed by application

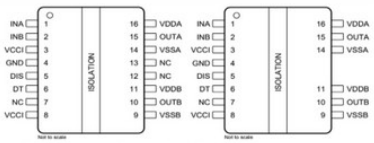


DW Package 16-Pin SOIC

PARAMETER		UCC2152x (current Si)	UCC2152x (new Si)
Isolation	CMTI	100V/ns (min)	125V/ns (min)
Input Stage	VCCI rec. operating range	3.0V – 18V	3.0V – 18V
	ICC switching MAX	2.0mA (typ) (500 kHz)	3mA (typ) (500 kHz)
	DIS pin structure	Internal pull down	Internal pull down
Output Driver	VDDx rec. operating range	5V UVLO version: 6.5V – 25V 8V UVLO version: 9.2V – 25V	5V UVLO version: 6.5V – 25V 8V UVLO version: 9.2V – 25V
	Max Drive Current TYP	+4A/-6A	+4A/-6A
	VDDx Power-up Delay MAX	100us	10us
	IDDx Quiescent Current TYP	1.8mA	2.5mA
Timing	Prop Delay MIN, MAX	14ns, 30ns	26ns, 45ns
	CHA-CHB Delay Matching MAX	<5ns	<5ns (Tj = -10C to +150C) <6.5ns (Tj = -40C to -10C)
	Dead Time range	5-5000ns	10-3000ns
	Deadtime Accuracy	20%	20%
Temperature	Tj Recommended Max	130°C	150°C

Design change considerations for new UCC21540 Si

- Critical gate driving parameters **don't change**:
  - Max drive current: +4A/-6A
  - Improved VDDx power up delay
  - Propagation delay can be addressed by application
- VDDx rec max **increases to 18V**

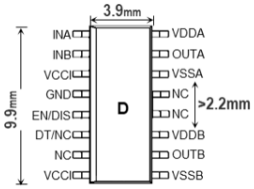


DW Package 16-Pin SOIC and DWK 14-pin package options

PARAMETER		UCC21540 (current Si)	UCC21540 (new Si)
Isolation	CMTI	100V/ns (min)	125V/ns (min)
Input Stage	VCCI rec. operating range	3.0V – 5.5V	3.0V – 18V
	ICC switching MAX	2.5mA (typ) (500 kHz)	3mA (typ) (500 kHz)
	DIS pin structure	Internal pull down	Internal pull down
Output Driver	VDDx rec. operating range	5V UVLO version: 6.0V – 18V 8V UVLO version: 9.2V – 18V	5V UVLO version: 6.5V – 25V 8V UVLO version: 9.2V – 25V
	Max Drive Current TYP	+4A/-6A	+4A/-6A
	VDDx Power-up Delay MAX	35us	10us
	IDDx Quiescent Current TYP	1.8mA	2.5mA
Timing	Prop Delay MIN, MAX	20ns, 40ns	26ns, 45ns
	CHA-CHB Delay Matching MAX	<5ns	<5ns (Tj = -10C to +150C) <6.5ns (Tj = -40C to -10C)
	Dead Time range	10-3000ns	10-3000ns
	Deadtime Accuracy	20%	20%
Temperature	Tj Recommended Max	150°C	150°C

Design change considerations for new UCC2122x Si

- Critical gate driving parameters **don't change**:
  - Max drive current: +4A/-6A
  - Improved VDDx power up delay
  - Propagation delay can be addressed by application
- **Design changes needed** for new UCC2122x Si
  - Dead time configuration resistor (*if applicable*) must be changed according to equation found Section 8.4 of the UCC21551 datasheet
  - Dead time can be disabled by leaving DT pin open or pulling DT pin to VCC



D Package 16-Pin SOIC

PARAMETER		UCC2122x (current Si)	UCC2122x (new Si)
Isolation	CMTI	100V/ns (min)	125V/ns (min)
Input Stage	VCCI rec. operating range	3.0V – 5.5V	3.0V – 5.5V
	ICC switching MAX	2.5mA (typ) (500 kHz)	2.7mA (typ) (500 kHz)
	DIS pin structure	Internal pull down	Internal pull up
Output Driver	VDDx rec. operating range	8V UVLO version: 9.2V – 18V	8V UVLO version: 9.2V – 25V
	Max Drive Current TYP	+4A/-6A	+4A/-6A
	VDDx Power-up Delay MAX	35us	10us
	IDDx Quiescent Current MAX	1.8mA	2.3mA
Timing	Prop Delay MIN, MAX	20ns, 40ns	26ns, 45ns
	CHA-CHB Delay Matching MAX	<5ns	<5ns (Tj = -10C to +150C) <6.5ns (Tj = -40C to -10C)
	Dead Time range	10-3000ns	27-870ns
	Deadtime Accuracy	20%	20%
Temperature	Tj Recommended Max	150°C	150°C

Changes from Revision E (December 2021) to Revision F (November 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document... 1
- Deleted 5ns maximum delay matching from Features section... 1
- Changed Typ propagation delay from 19ns to 33ns... 1
- Changed 10ns minmum pulse width to 20ns... 1
- Changed operating temperature range to junction temeperature range... 1
- Changed CMTI specification from 100V/ns to 125V/ns... 1
- Changed surge immunity value from 12.8kV to 10kV... 1
- Deleted bullet on isolation barrier life >40 years... 1
- Deleted "Rejects input pulses and noise transients shorter than 5ns"... 1
- Updated safety certifications to latest standards... 1
- Deleted CSA certification... 1
- Updated Description section to match new spec values... 1
- Updated DT pin description to recommend ≤1nF capacitor on DT pin... 4
- Changed DT pin Min resistor recommendations from 500Ω to 2kΩ... 4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards... 5
- Deleted ambient temperature spec... 5
- Changed Max junction temp to 150C... 5
- Updated values from RθJA = 67.3°C/W, RθJC(top) = 34.4°C/W, RθJB = 32.1°C/W, ψJT = 18°C/W, ψJB = 31.6°C/W to RθJA = 69.8°C/W, RθJC(top) = 33.1°C/W, RθJB = 36.9°C/W, ψJT = 22.2°C/W, ψJB = 36°C/W... 5
- Updated values from PD = 1.05W, PDI = 0.05W, PDA/PDB = 0.5W to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW... 6
- Updated values from DTI = 21mm, VIOSM = 8000VPK to DTI = 17mm, VIOSM = 10000VPK and added VIMP = 7692VPK... 7
- Deleted safety related certifications section... 7
- Updated values from IS = 75mA/36mA, PS = 50mW/900mW/900mW/1850mW to IS = 58mA/34mA, PS = 50mW/870mW/870mW/1790mW... 8
- Changed test condition from VDDA=VDDB=12V to VDDA=VDDB=15V... 8
- Updated IVCCI quiescent current spec 1.4mA typical value to 1.5mA typical... 8
- Updated IVDDA/IVDDB quiescent current spec Max value from 1.8mA to 2.5mA... 8
- Updated IVCCI operating current Typ value from 2.0mA to 3.0mA and added Max value 3.5mA... 8
- Added IVDDA/IVDDB operating current Max = 4.2mA... 8
- Updated values from Rising threshold Min = 8.3V, Typ = 8.7V, Max = 9.2V to Min = 7.7V, Typ = 8.5V, Max = 8.9V... 8
- Updated values from Falling threshold Min = 7.8V, Typ = 8.2V, Max = 8.7V to Min = 7.2V, Typ = 7.9V, Max = 8.4V... 8
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V... 8
- Updated Input high threshold Min value from 1.6V to 1.2V... 8
- Changed output voltage at high state spec from 11.95V Typ to 14.95V Typ. Changed test condition from VDDA=VDDB=15V to VDDA=VDDB=12V. ... 8
- Deleted Dead time parameter from Electrical Characteristics and added new Timing Requirements... 9
- Changed propagation delay TPDHL and TPDLH from Min=14ns, Typ = 19ns, Max = 30ns to Min=26ns. Typ = 33ns, Max = 45ns... 9
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C... 9
- Added VCCI power up delay... 9
- Updated VDDA/VDDB power-up delay from Max = 100us to 10us... 9
- Updated CMTI from Min = 100V/ns to 125V/ns... 9
- Updated insulation and thermal curves to match updated characteristics... 10
- Updated typical characteristics figures... 11
- Updated Power-up UVLO Delay to OUTPUT section to match device electrical characteristics ... 16
- Changed the Functional Block Diagram to add deglitch filter block... 18
- Changed DISABLE logic; DISABLE left open will pull outputs low... 21
- Added paragraph on minimum pulse width to Output Stage section... 22
- Updated ESD diode structure... 23
- Updated DT Pin Connected to a Programming Resistor Between DT and GND Pins section to recommend <=1nF capacitor on DT pin. ... 24
- Updated typical schematic DT pin capacitor recommendation ... 26
- Updated Dead Time Setting Guidelines section to recommend <=1nF capacitor on DT pin. ... 33

Changes from Revision C (November 2021) to Revision D (November 2024) **Page**

- Changed typical propagation delay from 19ns to 33ns.... 1
- Changed minimum pulse width from 10ns to 20ns.... 1
- Deleted bullet on 5-ns maximum delay matching.... 1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.... 1
- Deleted bullet on >40 years isolation barrier.... 1
- Deleted bullet on rejecting shorter than 5ns input pulses.... 1
- Changed operating temperature to new range of junction temperature.... 1
- Updated certifications to latest standards. Removed CSA certification.... 1
- Deleted sentence on best-in-class propagation delay and PWD.... 1
- Changed minimum 100V/ns CMTI to 125V/ns.... 1
- Changed recommended DT pin condition and capacitor size on DT pin.... 3
- Changing all -0.5V minimum to -0.3V to keep consistent with newly released datasheets.... 4
- Changing all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets.... 4
- Changed input signal voltage transient test condition to 50ns and absolute minimum to -5V.... 4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards.... 4
- Changed 12V-UVLO recommended minimum VDDA/B voltage from 14.7V to 13.5V.... 4
- Deleted ambient temperature spec.... 4
- Changed Max junction temp to 150C.... 4
- Updated values from RθJA = 68.3°C/W, RθJC(top) = 31.7°C/W, RθJB = 27.6°C/W, ψJT = 17.7°C/W, ψJB = 27°C/W to RθJA = 74.1°C/W, RθJC(top) = 34.1°C/W, RθJB = 32.8°C/W, ψJT = 23.7°C/W, ψJB = 32.1°C/W.. 4
- Updated values from PD = 1810mW, PDI = 0.05W, PDA/PDB = 880mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test condition.... 5
- Updated values from DTI = 21mm, VIOSM = 8000VPK to DTI = 17mm, VIOSM = 10000VPK and added VIMP = 7692VPK.... 6
- Deleted safety related certifications section.... 6
- Updated values from IS = 58mA/35mA, PS = 50mW/880mW/880mW/1810mW to IS = 53mA/32mA, PS = 50mW/800mW/800mW/1650mW.... 7
- Changed VCCI quiescent current typical from 1.4mA to 1.5mA.... 7
- Updated IVDDA/IVDDB quiescent current spec Max value from 1.8mA to 2.5mA.... 7
- Updated IVCCI operating current Typ value from 2.0mA to 3.0mA and added Max value 3.5mA.... 7
- Changed IVDDA/IVDDB operating current Typ from 3mA to 2.5mA and added Max = 4.2mA.... 7
- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V.... 7
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V.... 7
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V.... 7
- Updated values from Rising threshold Min = 12.5V, Typ = 13.5V, Max = 14.5V to Min = 11.7V, Typ = 12.5V, Max = 13.3V.... 7
- Updated values from Rising threshold Min = 11.5V, Typ = 12.5V, Max = 13.5V to Min = 10.7V, Typ = 11.5V, Max = 12.3V.... 7
- Updated Input high threshold Min value from 1.6V to 1.2V.... 7
- Deleted enable high and low threshold.... 7
- Updated Deadtime parameter by moving to new Timing Requirements table and added more parameters.... 8
- Changed propagation delay TPDHL and TPDLH from Min = 14ns, Typ = 19ns, Max = 30ns to Min = 26ns, Typ = 33ns, Max = 45ns.... 8
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C.... 8
- Deleted VCCI power up delay typical 40us and added max 50us.... 8
- Updated VDDA/VDDB power-up delay from Typ = 50us to Max=10us.... 8
- Updated CMTI from Min = 100V/ns to 125V/ns.... 8
- Updated insulation and thermal curves to match updated characteristics.... 9
- Updated typical characteristics figures.... 10
- Updated UVLO timing delays.... 15
- Added driver stage deglitch filter block in functional block diagram.... 17
- Changed ENABLE logic; ENABLE left open will pull outputs low.... 19
- Added paragraph on minimum pulse width to Output Stage section.... 20
- Updated ESD diode structure.... 21
- Changed recommended DT capacitor size from >2.2nF to ≤1nF.... 21
- Changed recommended DT capacitor size in schematic.... 23
- Changed DT capacitor size to ≤1nF.... 24
- Changed DT capacitor size recommendation from >=2.2nF to ≤1nF.... 33

Changes from Revision D (February 2021) to Revision E (November 2024) **Page**

- Changed CMTI from greater than 100V/ns to greater than 125V/ns....1
- Changed propagation delay from 40ns max to 33ns typical....1
- Deleted bullet on 5-ns maximum delay matching....1
- Changed maximum pulse width distortion from 5.5ns to 6ns....1
- Changed 35us maximum VDD power up delay to 10us maximum....1
- Updated certification to the latest standards....1
- Updated per the latest industry and Texas Instruments data sheet standards....1
- Changed minimum 100V/ns CMTI to 125V/ns....1
- Deleted sentence on rejecting input transients shorter than 5ns....1
- Changed negative voltage handling from -2V for 200ns to -5V for 50ns for input pins....1
- Changed schematic DT capacitor size from >=2.2nF to <=1nF....1
- Changed recommended DT pin condition and capacitor size on DT pin....3
- Changed VCCI absmax from 6V to 20V....6
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V....6
- Changing all -0.5V minimum to -0.3V to keep consistent with newly released datasheets....6
- Changing all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets....6
- Changed input signal voltage transient test condition to 50ns and absolute minimum to -5V....6
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards....6
- Changed VCCI recommended max from 5.5V to 18V....6
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V....6
- Changed 5V-UVLO recommended minimum VDDA/B voltage from 6V to 6.5V....6
- Deleted ambient temperature spec....6
- Changed junction temperature max from 130°C to 150°C....6
- Updated DWK values from RθJA = 69.7°C/W, RθJC(top) = 33.1°C/W, RθJB = 29.0°C/W, ψJT = 20.0°C/W, ψJB = 28.3°C/W to RθJA = 74.1°C/W, RθJC(top) = 34.1°C/W, RθJB = 32.8°C/W, ψJT = 23.7°C/W, ψJB = 32.1°C/W....7
- Added DW package thermal information....7
- Updated values from PD = 1775mW, PDI = 15mW, PDA/PDB = 880mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions. 7
- Added VIMP = 7692Vpk and changed Viosm from 8000V to 10000V per latest insulation standard....7
- Deleted safety related certifications section....7
- Updated DWK values from IS = 73mA, PS = 15mW/880mW/880mW/1775mW to IS = 66mA, PS = 50mW/800mW/800mW/1650mW 8
- Added DW safety limiting values....8
- Changed test condition from VDDA=VDDB=12V to VDDA=VDDB=15V....10
- Updated IVDDA/IVDDB quiescent current spec Max value from 1.8mA to 2.5mA....10
- Updated IVCCI operating current Typ value from 2.5mA to 3.0mA and added Max value 3.5mA....10
- Added IVDDA/IVDDB operating current Max = 4.2mA....10
- Updated values from Rising threshold Min = 5.0V, Typ = 5.5V, Max = 5.9V to Min = 5.7V, Typ = 6.0V, Max = 6.3V 10
- Updated values from Falling threshold Min = 4.7V, Typ = 5.2V, Max = 5.6V to Min = 5.4V, Typ = 5.7V, Max = 6.0V 10
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V....10
- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V 10
- Updated values from Rising threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V 10
- Updated Input high threshold Min value from 1.6V to 1.2V....10
- Updated Input low threshold Max value from 1.25V to 1.2V....10
- Deleted peak current minimum values for UCC21540/2....10
- Deleted output resistance maximum values for UCC21540/2....10
- Deleted output voltage at high state minimum. Changed typical value from 11.95V to 14.95V. Changed test condition from VDD=12V to VDD=15V for UCC21540/2....10
- Deleted output voltage at low state maximum. Changed test condition from VDD=12V to VDD=15V for UCC21540/2....10
- Changed driver active pull down typical value from 1.75V to 1.6V and max value from 2.1V to 2V....10
- Deleted dead time matching rows....10
- Changed test condition from VDDA=VDDB=12V to VDDA=VDDB=15V....11
- Deleted minimum input pulse width typical value....11
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns....11
- Changed pulse width distortion max from 5.5ns to 6ns for UCC21540/2....11

- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C.....11
- Deleted VCCI power up delay typical 40us and changed max from 59us to 50us.....11
- Deleted VDD power up delay typical 23us and changed max from 35us to 10us.....11
- Updated CMTI from Min = 100V/ns to 125V/ns.....11
- Updated thermal curves to match updated characteristics.....12
- Updated typical char plots to show device characteristics 14
- Deleted language on deglitch filter. Changed minimum pulse width from 10ns typical to 20ns maximum. 17
- Changed recommended decoupling capacitor placement from 2.2nF or greater to ≤1nF.....18
- Changed UVLO delay timing.....19
- Updated functional block diagram.....21
- Changed clamping voltage typical value from 1.75V to 1.6V.....22
- Changed DIS pull-down resistor size from 50kOhm to 200kOhm.....23
- Added paragraph on minimum pulse width to Output Stage section.....24
- Updated ESD diode structure.....24
- Deleted incomplete sentence due to datasheet draft error.....25
- Changed DT capacitor recommendation from >=2.2nF to <=1nF 25
- Deleted sentence on DT pin steady state voltage 25
- Changed DT capacitor size in application schematic 27
- Changed DT capacitor size from 2.2nF to <=1nF.....28
- Changed DT capacitor recommendation from >=2.2nF to <=1nF.....38

Changes from Revision B (February 2024) to Revision C (November 2024) **Page**

- Updated Features section to reflect device characteristics.....1
- Added junction temperature range.....1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.....1
- Changed maximum VDD output drive supply from 18V to 25V.....1
- Changed typical propagation delay from 28ns to 33ns.....1
- Deleted bullet on maximum delay matching.....1
- Changed maximum pulse-width distortion from 5.5ns to 5ns.....1
- Deleted bullet on minimum pulse width.....1
- Added maximum VDD power-up delay of 10us.....1
- Deleted bullets on isolation barrier life and surge immunity.....1
- Updated certification to the latest standards.....1
- Updated applications section.....1
- Updated description section to reflect device characteristics.....1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.....1
- Deleted sentence on negative voltage handling.....1
- Changed Functional Block Diagram to Typical Application Schematic.....1
- Changed DIS pin description; leaving DIS pin open would disable the device, and the pin is internally pulled high instead of low.....3
- Deleted DT pin recommended capacitor size of 2.2nF or greater. Changed DT pin equation.....3
- Added INA and INB RC filter recommendation.....3
- Changed all -0.5V minimum to -0.3V to keep consistent with newly released datasheets.....4
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V.....4
- Changed all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets.....4
- Changed input signal trasient voltage from -2V to -5V and changed test condition from 200ns to 50ns.....4
- Added D package channel to channel isolation voltage.....4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards.....4
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V.....4
- Deleted ambient temperature spec.....4
- Changed junction temperature max from 130°C to 150°C.....4
- Updated thermal values from RθJA = 68.5°C/W, RθJC(top) = 30.5°C/W, RθJB = 22.8°C/W, ψJT = 17.1°C/W, ψJB = 22.5°C/W to RθJA = 80.2°C/W, RθJC(top) = 36.6°C/W, RθJB = 45°C/W, ψJT = 28°C/W, ψJB = 44.3°C/W.....4
- Updated values from PD = 1825mW, PDI = 15mW, PDA/PDB = 905mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions.....5
- Updated DIN EN IEC to the latest standard, updated insulation voltage values.....6
- Changed barrier capacitance from 0.5pF to ~1.2pF.....6
- Deleted safety-related certifications section, certification ongoing.....6
- Changed IS testing condition. Changed IS value from 75mA (with VDDA/B=12V) to 50mA (with VDDA/B=15V) and 30mA (with VDDA/B=25V).....7
- Updated safety-limiting values from PS = 15mW/905mW/905mW/1825mW to PS = 50mW/750mW/750mW/1550mW.....7
- Updated IVCCI quiescent current spec Typ value from 1.5mA to 1.4mA.....8
- Added more test conditions for IVCC and IVDD.....8
- Updated IVCCI operating current Typ value from 2.5mA to 2.7mA and added Max value 3.2mA.....8
- Updated IVDDA/IVDDB quiescent current spec Typ from 1.0mA to 1.2mA and Max value from 1.8mA to 2.0mA.....8
- Updated IVDDA/IVDDB operating current Typ value from 2.5mA to 2.7mA and added Max value 4.4mA. Deleted Cload from test condition.....8
- Changed VCCI power-up delay from Typ = 40us to Min = 18us, Max = 80us.....8
- Added VCC UVLO OFF delay and deglitch specs.....8

- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V..... 8
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V..... 8
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V..... 8
- Deleted VDD power up delay Typ 22us and added Max value of 10us..... 8
- Added VDD UVLO OFF delay and deglitch specs..... 8
- Updated Input high threshold Typ = 1.8V, Max = 2V to Typ = 2V, Max = 2.3V. Deleted Min spec..... 8
- Deleted Input low threshold voltage Max spec..... 8
- Updated Input threshold hysteresis Typ = 0.8V to Typ = 1V..... 8
- Added spec INx Pin Pull Down Resistance..... 8
- Updated peak current test condition to 0.22uF load capacitance. Changed peak output source current direction..... 8
- Updated output resistance test condition from ±10mA to ±0.05A..... 8
- Deleted output voltage at high/low state specs..... 8
- Updated active pull-down Typ = 1.75V, Max = 2.1V to Typ = 1.6V, Max = 2V..... 8
- Updated DT pin specs, deleted dead time matching..... 8
- Changed output rise time Typ from 5ns to 8ns. Deleted Max value..... 9
- Changed output fall time Typ from 6ns to 8ns. Deleted Max value..... 9
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns..... 9
- Changed minimum pulse width from Typ = 10ns, Max = 20ns to Min = 4ns, Typ = 12ns, Max = 30ns..... 9
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C..... 9
- Changed pulse width distortion max from 5.5ns to 5ns..... 9
- Updated CMTI from Min = 100V/ns to 125V/ns..... 9
- Updated thermal curves to match updated characteristics..... 10
- Updated typical char plots to show device characteristics..... 11
- Deleted mininum pulses in parameter measurement information..... 15
- Changed DT formula. Deleted recommended DT decoupling capacitor size of 2.2nF or greater..... 16
- Updated UVLO delay to match new specs..... 16
- Updated functional block diagram to reflect device characteristics..... 18
- Changed logic table; leaving DIS pin open disables the driver..... 20
- Updated input stage section to match new specs..... 20
- Added paragraph on minimum pulse width to Output Stage section..... 21
- Updated ESD structure diagram to reflect device characteristics..... 22
- Changed dead time equation, deleted recommendation on 2.2nF or greater DT capacitor..... 22
- Changed typical application schematic to remove DT capacitor..... 24
- Updated applications sections to match the latest specs..... 26
- Added Dead Time Setting Guidelines section..... 30
- Changed maximum VDDA/VDDB from 18V to 25V..... 35
- Deleted DT capacitor size recommendation of ≥ 2.2 nF..... 36
- Updated layout guidelines..... 36

Changes from Revision F (February 2024) to Revision G (November 2024) **Page**

- Updated Features section to reflect device characteristics.....1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.....1
- Changed maximum propagation delay from 40ns to typical 33ns.....1
- Deleted bullet on maximum delay matching.....1
- Changed maximum pulse-width distortion from 5.5ns to 5ns.....1
- Changed maximum VDD power-up delay from 35us to 10us.....1
- Changed maximum VDD output drive supply from 18V to 25V.....1
- Changed operating temperature range to junction temperature range.....1
- Deleted bullet on rejecting input pulse shorter than 5ns.....1
- Updated certification to the latest standards.....1

- Changed CMTI from greater than 100V/ns to greater than 125V/ns.....1
- Deleted sentences on input rejecting short transients and input/output withstanding voltage spikes.....1
- Changed active pull-down from 2.1V max to 2V max.....1
- Changed 5V UVLO recommended VDD supply minimum from 6V to 6.5V.....3
- Changed DIS pin description; leaving DIS pin open would disable the device.....3
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V.....4
- Changed all -0.5V minimum to -0.3V to keep consistent with newly released datasheets.....4
- Changed all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets.....4
- Deleted input signal voltage transient spec.....4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards.....4
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V.....4
- Changed 5V-UVLO recommended minimum VDDA/B voltage from 6V to 6.5V.....4
- Deleted ambient temperature spec.....4
- Changed junction temperature max from 130°C to 150°C.....4
- Updated thermal values from RθJA = 68.5°C/W, RθJC(top) = 30.5°C/W, RθJB = 22.8°C/W, ψJT = 17.1°C/W, ψJB = 22.5°C/W to RθJA = 80.2°C/W, RθJC(top) = 36.6°C/W, RθJB = 45°C/W, ψJT = 28°C/W, ψJB = 44.3°C/W.....5
- Updated values from PD = 1825mW, PDI = 15mW, PDA/PDB = 905mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions.....5
- Updated DIN EN IEC to the latest standard, updated insulation voltage values.....6
- Updated barrier capacitance value.....6
- Deleted safety-related certifications section, certification ongoing.....6
- Changed IS testing condition. Changed IS value from 75mA (with VDDA/B=12V) to 50mA (with VDDA/B=15V) and 30mA (with VDDA/B=25V).....7
- Updated safety-limiting values from PS = 15mW/905mW/905mW/1825mW to PS = 50mW/750mW/750mW/1550mW.....7
- Updated IVCCI quiescent current spec Typ value from 1.5mA to 1.4mA.....8
- Updated IVDDA/IVDDB quiescent current spec Typ from 1.0mA to 1.2mA and Max value from 1.8mA to 2.0mA.....8
- Updated IVCCI operating current Typ value from 2.5mA to 2.7mA and added Max value 3.2mA.....8
- Updated IVDDA/IVDDB operating current Typ value from 2.5mA to 2.7mA and added Max value 4.4mA. Deleted Cload from test condition.....8
- Updated values from Rising threshold Min = 5.0V, Typ = 5.5V, Max = 5.9V to Min = 5.7V, Typ = 6.0V, Max = 6.3V.....8
- Updated values from Falling threshold Min = 4.7V, Typ = 5.2V, Max = 5.6V to Min = 5.4V, Typ = 5.7V, Max = 6.0V.....8
- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V.....8
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V.....8
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V.....8
- Updated Input high threshold Typ = 1.8V, Max = 2V to Typ = 2V, Max = 2.3V. Deleted Min spec.....8
- Deleted Input low threshold voltage Max spec.....8
- Updated Input threshold hysteresis Typ = 0.8V to Typ = 1V.....8
- Updated peak current test condition to 0.22uF load capacitance. Changed peak output source current direction.....8
- Updated output resistance test condition from ±10mA to ±5mA.....8
- Deleted output voltage at high/low state specs.....8
- Updated active pull-down Typ = 1.75V, Max = 2.1V to Typ = 1.6V, Max = 2V.....8
- Changed output rise time Typ from 5ns to 8ns. Deleted Max value.....9
- Changed output fall time Typ from 6ns to 8ns. Deleted Max value.....9

- Changed minimum pulse width from Typ = 10ns, Max = 20ns to Min = 4ns, Typ = 12ns, Max = 30ns..... 9
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns..... 9
- Changed pulse width distortion max from 5.5ns to 5ns..... 9
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C..... 9
- Changed VCCI power-up delay from Typ = 40us, Max = 59us to Min = 18us, Typ = 42us, Max = 80us..... 9
- Deleted VDD power up delay Typ 22us and changed Max from 35us to 10us..... 9
- Updated CMTI from Min = 100V/ns to 125V/ns..... 9
- Updated thermal curves to match updated characteristics..... 10
- Updated typical char plots to show device characteristics 11
- Deleted language on deglitch filter. Changed minimum pulse width from typical 10ns to 12ns..... 14
- Updated UVLO delay to match new specs..... 15
- Updated functional block diagram to reflect device characteristics..... 17
- Changed logic table; leaving DIS pin open disables the driver..... 19
- Updated input stage section to match new specs..... 19
- Added paragraph on minimum pulse width to Output Stage section..... 20
- Updated ESD structure diagram to reflect device characteristics..... 20
- Updated device operation mode when DIS is floating. Added recommendation of bypass capacitor..... 21
- Changed maximum VDDA/VDDB from 18V to 25V..... 32

Changes from Revision A (January 2020) to Revision B (March 2024) **Page**

- Changed from Advance Information to Production Data..... 1
- Updated Features section to reflect device characteristics..... 1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns..... 1
- Changed maximum propagation delay from 40ns to typical 33ns..... 1
- Changed maximum pulse-width distortion from 5.5ns to 5ns..... 1
- Changed maximum VDD power-up delay from 35us to 10us..... 1
- Changed maximum VDD output drive supply from 18V to 25V..... 1
- Changed operating temperature range to junction temperature range..... 1
- Deleted bullet on rejecting input pulse shorter than 5ns..... 1

- Updated certification to the latest standards... 1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns... 1
- Deleted sentences on input rejecting short transients and input/output withstanding voltage spikes... 1
- Changed active pull-down from 2.1V max to 2V max... 1
- Changed 5V UVLO recommended VDD supply minimum from 6V to 6.5V... 3
- Changed DIS pin description; leaving DIS pin open would disable the device... 4
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V... 5
- Changed all -0.5V minimum to -0.3V to keep consistent with newly released datasheets... 5
- Changed all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets... 5
- Deleted input signal voltage transient spec... 5
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards... 5
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V... 5
- Changed 5V-UVLO recommended minimum VDDA/B voltage from 6V to 6.5V... 5
- Deleted ambient temperature spec... 5
- Changed junction temperature max from 130°C to 150°C... 5
- Updated thermal values from RθJA = 68.5°C/W, RθJC(top) = 30.5°C/W, RθJB = 22.8°C/W, ψJT = 17.1°C/W, ψJB = 22.5°C/W to RθJA = 80.2°C/W, RθJC(top) = 36.6°C/W, RθJB = 45°C/W, ψJT = 28°C/W, ψJB = 44.3°C/W... 5
- Updated values from PD = 1825mW, PDI = 15mW, PDA/PDB = 905mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions. ... 6
- Changed Material Group from I to II and CTI from >600V to >400V... 6
- Updated DIN EN IEC to the latest standard, updated insulation voltage values... 6
- Updated barrier capacitance value... 6
- Deleted safety-related certifications section, certification ongoing... 6
- Changed IS testing condition. Changed IS value from 75mA (with VDDA/B=12V) to 50mA (with VDDA/B=15V) and 30mA (with VDDA/B=25V). ... 7
- Updated safety-limiting values from PS = 15mW/905mW/905mW/1825mW to PS = 50mW/750mW/750mW/1550mW ... 7
- Updated IVCCI quiescent current spec Typ value from 1.5mA to 1.4mA... 7
- Updated IVDDA/IVDDB quiescent current spec Typ from 1.0mA to 1.2mA and Max value from 1.8mA to 2.0mA... 7
- Updated IVCCI operating current Typ value from 2.5mA to 2.7mA and added Max value 3.2mA... 7
- Updated IVDDA/IVDDB operating current Typ value from 2.5mA to 2.7mA and added Max value 4.4mA. Deleted Cload from test condition. ... 7
- Updated values from Rising threshold Min = 5.0V, Typ = 5.5V, Max = 5.9V to Min = 5.7V, Typ = 6.0V, Max = 6.3V ... 7
- Updated values from Falling threshold Min = 4.7V, Typ = 5.2V, Max = 5.6V to Min = 5.4V, Typ = 5.7V, Max = 6.0V ... 7
- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V ... 7
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V ... 7
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V... 7
- Updated Input high threshold Typ = 1.8V, Max = 2V to Typ = 2V, Max = 2.3V. Deleted Min spec... 7
- Deleted Input low threshold voltage Max spec... 7
- Updated Input threshold hysteresis Typ = 0.8V to Typ = 1V... 7
- Updated peak current test condition to 0.22uF load capacitance. Changed peak output source current direction... 7
- Updated output resistance test condition from ±10mA to ±5mA... 7
- Deleted output voltage at high/low state specs... 7
- Updated active pull-down Typ = 1.75V, Max = 2.1V to Typ = 1.6V, Max = 2V... 7

- Changed output rise time Typ from 5ns to 8ns. Deleted Max value... 8
- Changed output fall time Typ from 6ns to 8ns. Deleted Max value... 8
- Changed minimum pulse width from Typ = 10ns, Max = 20ns to Min = 4ns, Typ = 12ns, Max = 30ns... 8
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns... 8
- Changed pulse width distortion max from 5.5ns to 5ns... 8
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C... 8
- Changed VCCI power-up delay from Typ = 40us, Max = 59us to Min = 18us, Typ = 42us, Max = 80us... 8
- Deleted VDD power up delay Typ 22us and changed Max from 35us to 10us... 8
- Updated CMTI from Min = 100V/ns to 125V/ns... 8
- Updated thermal curves to match updated characteristics... 9
- Updated typical char plots to show device characteristics ... 10
- Deleted language on deglitch filter. Changed minimum pulse width from typical 10ns to 12ns... 13
- Updated UVLO delay to match new specs... 14
- Updated functional block diagram to reflect device characteristics... 16
- Changed logic table; leaving DIS pin open disables the driver... 18
- Updated input stage section to match new specs... 18
- Added paragraph on minimum pulse width to Output Stage section... 19
- Updated ESD structure diagram to reflect device characteristics... 20
- Updated device operation mode when DIS is floating. Added recommendation of bypass capacitor... 20
- Changed maximum VDDA/VDDB from 18V to 25V... 31

The datasheet number will be changing.

Device Family	Change From:	Change To:
UCC21520	**SLUSCJ9E**	**SLUSCJ9F**
UCC21530	**SLUSDC0C**	**SLUSDC0D**
UCC21540	**SLUSDE1D**	**SLUSDE1E**
UCC21222	**SLUSCX6B**	**SLUSCX6C**
UCC21220	**SLUSCK0F**	**SLUSCK0G**
SN21220	**SLUSDX5A**	**SLUSDX5B**

https://www.ti.com/product/UCC21520
https://www.ti.com/product/UCC21530
https://www.ti.com/product/UCC21540
https://www.ti.com/product/UCC21222
https://www.ti.com/product/UCC21220

The document (SN21220) is not available on the TI website. Please contact the document owner at e-preiss@ti.com or visit the MySecure site for a copy of the full datasheet.

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are to transition TI's dual-channel isolated gate drivers to TI's most efficient manufacturing processes and technology,underscoring our commitment to product longevity and supply continuity. Additionally, the newly-designed circuit includes improvements to robustness in common automotive and industrial applications, underscoring our commitment to continuous improvements in both product quality and end system robustness.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

See change summary table and datasheet revision history

Impact on Environmental Ratings:

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
MIHO8	MH8	JPN	Ibaraki
DP1DM5	DM5	USA	Dallas
RFAB	**RFB**	**USA**	**Richardson**

Die Rev:

Current	**New**
Die Rev [2P]	**Die Rev [2P]**
A,B,C	**A**

Sample product shipping label (not actual product label):

Product Affected:

Group 1 Device list (RFAB Process migration, die change plus BOM update):

UCC21520ADWR	UCC21520DWR	UCC21530DWKR

Group 2 Device list (BOM & Die change update only):

SN21220ADR	UCC21220DR	UCC21540ADWKR	UCC21540DWKR
UCC21220ADR	UCC21222DR	UCC21540ADWR	UCC21540DWR

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SNA21530DQDWKRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1	QBS Reference: ISO6763QDWRQ1	QBS Reference: UCC21520QDWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	1/77/0	3/231/0	1/77/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	1/77/0	3/231/0	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	1/77/0	3/231/0	1/77/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	3/135/0	-
HTOL	B1	Life Test	125C	1000 Hours	-	3/231/0	1/77/0	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-

Type	#	Test Name	Condition	Duration	Qual Device: SNA21530DQDWKRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1	QBS Reference: ISO6763QDWRQ1	QBS Reference: UCC21520QDWRQ1
PD	C4	Physical Dimensions	Cpk>1.67	-	-	3/30/0	1/10/0	-	1/10/0
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	-	1/3/0
LU	E4	Latch-Up	Per JESD78	-	1/3/0	1/6/0	1/6/0	-	1/3/0
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	1/30/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SNA21530DQDWKRQ1 is qualified at MSL3 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-NPD-2404-122

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: UCC21520QDWRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1	QBS Reference: ISO6763QDWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	1/77/0	-	1/77/0	3/231/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	1/77/0	3/231/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	-	1/77/0	3/231/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	3/135/0
HTOL	B1	Life Test	125C	1000 Hours	1/77/0	3/231/0	1/77/0	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	1/10/0	3/30/0	1/10/0	-
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	-
LU	E4	Latch-Up	Per JESD78	-	1/3/0	1/6/0	1/6/0	-
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device UCC21520QDWRQ1 is qualified at MSL3 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2404-046

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: UCC21550AQDWRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1	QBS Reference: ISO6763QDWRQ1	QBS Reference: UCC21550BQDWRQ1	QBS Reference: UCC21551CQDWKRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	1/77/0	3/231/0	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	1/77/0	3/231/0	-	3/231/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	1/77/0	3/231/0	-	3/231/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	3/135/0	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	3/231/0	1/77/0	-	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	3/30/0	1/10/0	-	-	3/30/0
ESD	E2	ESD CDM	-	500 Volts	-	1/3/0	1/3/0	-	1/3/0	-
ESD	E2	ESD HBM	-	2000 Volts	-	1/3/0	1/3/0	-	1/3/0	-
LU	E4	Latch-Up	Per JESD78	-	-	1/6/0	1/6/0	-	1/6/0	-
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	3/90/0	3/90/0	3/90/0	1/30/0	-

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device UCC21550AQDWRQ1 is qualified at MSL3 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-NPD-2305-069

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: UCC21330BQDRQ1	QBS Reference: ISO6721BQDRQ1	QBS Reference: TLV9022QDRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	3/231/0	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	3/231/0	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0	3/231/0	-	-
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	-	-
HTSL	A6	High Temperature Storage Life	175C	500 Hours	-	3/135/0	-	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	-	3/231/0	1/77/0
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0	-

Type	#	Test Name	Condition	Duration	Qual Device: UCC21330BQDRQ1	QBS Reference: ISO6721BQDRQ1	QBS Reference: TLV9022QDRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	3/30/0	3/30/0	3/30/0	3/30/0	1/10/0
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	1/6/0	1/6/0	1/6/0	1/6/0	1/6/0
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	3/90/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device UCC21330BQDRQ1 is qualified at MSL2 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-NPD-2211-087

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: UCC21551CQDWKRQ1	QBS Reference: UCC23513QDWYQ1	QBS Reference: UCC21551CQDWKRQ1	QBS Reference: ISO6763QDWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	1/77/0	3/231/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	3/231/0	-	1/77/0	3/231/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	1/77/0	3/231/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	3/135/0
HTOL	B1	Life Test	125C	1000 Hours	-	3/231/0	1/77/0	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	1/15/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	3/30/0	3/30/0	1/10/0	-
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	-
LU	E4	Latch-Up	Per JESD78	-	1/6/0	1/6/0	1/6/0	-
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device UCC21551CQDWKRQ1 is qualified at MSL2 260C
- Qual Device UCC21551CQDWKRQ1 is qualified at MSL3 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-NPD-2306-079

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: UCC21222QDRQ1	QBS Reference: UCC21330BQDRQ1	QBS Reference: UCC21330BQDRQ1
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	3/231/0	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	3/30/0	-
ESD	E2	ESD CDM	-	500 Volts	-	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	-	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	1/6/0	1/6/0
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	1/30/0	1/30/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device UCC21222QDRQ1 is qualified at MSL2 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2312-013

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.