

PCN Number:	20260915000.1	PCN Issued	September 18, 2026
Qualification of RFAB as an additional Fab site option, Die Revision, Datasheet and Marking update for select devices		Sample request deadline:	November 17, 2026
		Estimated 1st ship date:	December 17, 2026
Sample requests received after November 17, 2026 will not be supported.			

Change type(s)
Packing/Shipping/Labeling Design Data Sheet/Electrical Specification Wafer Fab Site Wafer Fab Material Wafer Fab Process

PCN Details

Description of Change:					
Texas Instruments is pleased to announce the qualification of RFAB as an additional Fab site option, Die revision, Data sheet and Marking update for the devices listed below.					
Current Fab Site			Additional Fab site		
Current Fab Site	Process	Wafer Diameter	Additional Fab site	Process	Wafer Diameter
FFAB	ASLNONC10	200mm	RFAB	LBC9	300mm
The die was also changed as a result of the process change.					
Device Marking					
Device name	Current		Additional		
SN74LVC1G00DCKR	CA5, CAS, CAR, CAH, CAP, CAJ		27C		
SN74LVC1G02DCKR	CB5, CBS, CBR, CBJ, CBR, CBH, CBF, CBP		27D		
SN74LVC1G08DCKR	CE5, CES, CEJ, CER, CEH, CEF, CEP		1MI		
SN74LVC1G125DCKR	CM5, CMJ, CMR, CMF		1BC		
SN74LVC1G126DCKR	CN5, CNR, CNJ, CNF		1BD		
SN74LVC1G132DCKR	D55, D5J, D5R		27E		
SN74LVC1G240DCKR	CK5, CKJ, CKR, CKF		27F		
SN74LVC1G32DCKR	CG5, CGS, CGJ, CGR, CGH, CGF, CGP		1BB		
SN74LVC1G80DCKR	CX5, CXR, CXJ, CXR, CXF		27G		
SN74LVC1G86DCKR	CH5, CHR, CHJ, CHR, CHF		27H		
SN74LVC1G79DCKR	CR5, CRJ, CRR, CRF		27J		
SN74LVC1G38DCKR	D75, D7J, D7R, D7H, D7F, D7P		27K		

Data sheet update

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.



SN74LVC1G00
SCES212AC – APRIL 1999 – REVISED AUGUST 2026

Changes from April 1, 2014 to August 12, 2026 (from Revision AB (April 2014) to Revision AC (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Changed <i>Handling Ratings</i> to <i>ESD Ratings</i>	4
• Moved <i>Storage temperature range</i> from <i>Handling Ratings</i> to <i>Absolute Maximum Ratings</i>	4
• Updated format for <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W.....	5
• Removed redundant t_{pd} specification from <i>Switching Characteristics</i> , –40°C to 125°C	7
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	14
• Updated <i>Overview</i> , <i>Application and Implementation</i> , <i>Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	16



SN74LVC1G02
SCES213Y – APRIL 1999 – REVISED AUGUST 2026

Changes from April 1, 2014 to August 12, 2026 (from Revision X (April 2014) to Revision Y (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved T_{stg} to <i>Absolute Maximum Ratings</i> table.....	4
• Changed <i>Handling Ratings</i> to <i>ESD Ratings</i>	4
• Updated format for <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W.....	5

• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W.....	5
• Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W.....	5
• Changed tpd maximum value at $V_{CC} = 1.8V \pm 0.15V$ from: 7.2ns to: 7.7ns.....	6
• Changed tpd maximum value at $V_{CC} = 2.5V \pm 0.2V$ from: 4.4ns to: 4.5ns.....	6
• Changed tpd maximum value at $V_{CC} = 1.8V \pm 0.15V$ from: 8ns to: 8.4ns.....	6
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	14
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	16



SN74LVC1G240

SCES305M – JANUARY 2001 – REVISED AUGUST 2026

Changes from December 1, 2013 to August 12, 2026 (from Revision L (December 2013) to Revision M (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Added <i>Applications, Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Added <i>Device Information</i> table.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved T_{stg} to <i>Absolute Maximum Ratings</i> table.....	4
• Added <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	9
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	14



SN74LVC1G80

SCES221T – APRIL 1999 – REVISED AUGUST 2026

Changes from November 1, 2016 to August 12, 2026 (from Revision S (November 2016) to Revision T (August 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 243.4°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 179°C/W to: 263.7°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 77.6°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 58.4°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 77°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278.9°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 121.3°C/W to: 297.5°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 65.6°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 7.5°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 64.9°C/W to: 256.2°C/W.....	5

Changes from August 1, 2015 to August 12, 2026 (from Revision V (August 2015) to Revision W (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Added <i>Applications, Device Information table, Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Thermal Information</i> table.....	6
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W.....	6
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W.....	6
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W.....	6
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W.....	6
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W.....	6
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W.....	6
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W.....	6
• Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W.....	6
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W.....	6
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W.....	6
• Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W.....	6
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W.....	6
• Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W.....	6
• Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W.....	6
• Changed Junction-to-board characterization value for DRL package from: 77°C/W to: 259.2°C/W.....	6
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	15
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	17

Changes from February 1, 2014 to June 1, 2026 (from Revision R (February 2014) to Revision S (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated format for <i>Thermal Information</i> table.....	5
• Extended <i>Thermal Information</i> table to include $R_{BJC(top)}$, R_{BJB} , Ψ_{JT} , Ψ_{JB} , $R_{BJC(bot)}$	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 142°C/W to: 364.1°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	9
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	15

Changes from May 1, 2019 to August 12, 2026 (from Revision Z (May 2019) to Revision AA (August 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated format for <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 207.6°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 145.2°C/W to: 263.7°C/W..	5
• Changed Junction-to-board characterization value for DBV package from: 53.5°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 37.5°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 53.1°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 283.1°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 92.3°C/W to: 297.5°C/W....	5
• Changed Junction-to-board characterization value for DCK package from: 60.9°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 1.7°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 60.1°C/W to: 256.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 242.9°C/W to: 364.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 77.5°C/W to: 280.6°C/W....	5
• Changed Junction-to-board characterization value for DRL package from: 77.5°C/W to: 261.5°C/W.....	5
• Changed Junction-to-top characterization value for DRL package from: 9.6°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 77.3°C/W to: 259.2°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	9
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	14



SN74LVC1G132

SCES546E – FEBRUARY 2004 – REVISED AUGUST 2026

Changes from April 1, 2014 to August 12, 2026 (from Revision D (June 2017) to Revision E (August 2026))

	Page
• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated format for <i>Thermal Information</i> table.....	5
• Extended <i>Thermal Information</i> table to include $R_{\theta JC(top)}$, $R_{\theta JB}$, Ψ_{JT} , Ψ_{JB} , $R_{\theta JC(bot)}$	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	9
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	14



SN74LVC1G38

SCES538H – JANUARY 2004 – REVISED AUGUST 2026

Changes from February 1, 2020 to August 12, 2026 (from Revision G (February 2020) to Revision H (August 2026))

Page

• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..	5
• Changed Junction-to-board characterization value for DBV package from: 86.8°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 58°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 70.9°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 47°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W.....	5



SN74LVC1G79

SCES220V – APRIL 1999 – REVISED AUGUST 2026

Changes from April 1, 2017 to August 12, 2026 (from Revision U (April 2017) to Revision V (August 2026))

Page

• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..	5
• Changed Junction-to-board characterization value for DBV package from: 86.8°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 58°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 277.6°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 179.5°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 75.9°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 49.7°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 75.1°C/W to: 256.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 294.3°C/W to: 364.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 129.9°C/W to: 280.6°C/W..	5
• Changed Junction-to-board characterization value for DRL package from: 143.4°C/W to: 261.5°C/W.....	5
• Changed Junction-to-top characterization value for DRL package from: 14.3°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 144°C/W to: 259.2°C/W.....	5
• Added <i>Thermal Information</i> table.....	5



SN74LVC1G125

SCES223U – APRIL 1999 – REVISED AUGUST 2026

Changes from October 1, 2014 to August 13, 2026 (from Revision T (October 2014) to Revision U (August 2026))

Page

• Updated <i>Device Information</i> table to include body and package dimensions.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Handling Ratings</i> to <i>ESD Ratings</i> .	4
• Moved <i>Storage temperature range</i> from <i>Handling Ratings</i> to <i>Absolute Maximum Ratings</i> .	4
• Updated format for <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W.....	5

• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 243°C/W to: 364.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 78°C/W to: 280.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 78°C/W to: 261.5°C/W.....	5
• Changed Junction-to-top characterization value for DRL package from: 10°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 77°C/W to: 259.2°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	9
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	14



SN74LVC1G86

SCES222R – APRIL 1999 – REVISED AUGUST 2026

Changes from June 1, 2017 to August 12, 2026 (from Revision Q (June 2017) to Revision R (August 2026))

	Page
• Added <i>Thermal Information</i> table.....	5
• Changed Junction-to-ambient thermal resistance value for DBV package from: 206°C/W to: 357.1°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 252°C/W to: 371°C/W.....	5
• Changed tpd maximum value for $V_{CC} = 2.5V \pm 0.2V$ from: 4.5ns to: 4.9ns.....	6

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
SN74LVC1G00	SCES212AB	SCES212AC	http://www.ti.com/product/SN74LVC1G00
SN74LVC1G02	SCES213X	SCES213Y	http://www.ti.com/product/SN74LVC1G02
SN74LVC1G240	SCES305L	SCES305M	http://www.ti.com/product/SN74LVC1G240
SN74LVC1G80	SCES221S	SCES221T	http://www.ti.com/product/SN74LVC1G80
SN74LVC1G32	SCES219V	SCES219W	http://www.ti.com/product/SN74LVC1G32
SN74LVC1G126	SCES224R	SCES224S	http://www.ti.com/product/SN74LVC1G126
SN74LVC1G08	SCES217Z	SCES217AA	http://www.ti.com/product/SN74LVC1G08
SN74LVC1G132	SCES546D	SCES546E	http://www.ti.com/product/SN74LVC1G132
SN74LVC1G38	SCES538G	SCES538H	http://www.ti.com/product/SN74LVC1G38
SN74LVC1G79	SCES220U	SCES220V	http://www.ti.com/product/SN74LVC1G79
SN74LVC1G125	SCES223T	SCES223U	http://www.ti.com/product/

			SN74LVC1G125
SN74LVC1G86	SCES222Q	SCES222R	http://www.ti.com/product/SN74LVC1G86

Qual details are provided in the Qual Data Section.

Reason for Change:	Supply Continuity
---------------------------	-------------------

Anticipated impact on Form, Fit, Function, Quality or Reliability:	These devices include new die based on existing schematics in a larger diameter wafer fab with a die shrink. There are changes in the electrical tables. Physical aspects of the device have changed. Request the Supporting Data Packet (SDP) for more details on the changes. Evaluating samples is encouraged.																		
Impact on Environmental Ratings	Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings. <table><tr><th>RoHS</th><th>REACH</th><th>Green Status</th><th>IEC 62474</th></tr><tr><td>☒ No Change</td><td>☒ No Change</td><td>☒ No Change</td><td>☒ No Change</td></tr></table>	RoHS	REACH	Green Status	IEC 62474	☒ No Change	☒ No Change	☒ No Change	☒ No Change										
RoHS	REACH	Green Status	IEC 62474																
☒ No Change	☒ No Change	☒ No Change	☒ No Change																
Changes to product identification resulting from this PCN:	Fab Site Information <table><tr><th>Chip Site</th><th>Chip Site Origin Code (20L)</th><th>Chip Site Country Code (21L)</th><th>Chip Site City</th></tr><tr><td>FFAB</td><td>TID</td><td>DEU</td><td>Freising</td></tr><tr><td>RFAB</td><td>RFB</td><td>USA</td><td>Richardson</td></tr></table> Die Rev: <table><tr><th>Current</th><th>New</th></tr><tr><td>Die Rev [2P]</td><td>Die Rev [2P]</td></tr><tr><td>D, E</td><td>A</td></tr></table> Sample product shipping label (not actual product label): TEXAS INSTRUMENTS MADE IN: China 2DC: 20: MSL 1 / 260C / UNLIM OPT: ITEM: 73 LBL: 1A (L) TO: 1168  (1P) PTAS2560YFFR (Q) 3000 (D) 1710 (31T) LOT: 7133710JCP (4W) SWR (1T) 2855550Z9A (P) (2P) REV: AO (V) 0033317 (20L) CSO: DM6 (21L) CCO: USA (22L) ASO: JCP (23L) ACO: CHN	Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City	FFAB	TID	DEU	Freising	RFAB	RFB	USA	Richardson	Current	New	Die Rev [2P]	Die Rev [2P]	D, E	A
Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City																
FFAB	TID	DEU	Freising																
RFAB	RFB	USA	Richardson																
Current	New																		
Die Rev [2P]	Die Rev [2P]																		
D, E	A																		

Products Affected: (Fab, Design, Marking)			
SN74LVC1G00DCKR	SN74LVC1G126DCKR	SN74LVC1G79DCKR	
SN74LVC1G02DCKR	SN74LVC1G132DCKR	SN74LVC1G80DCKR	
SN74LVC1G08DCKR	SN74LVC1G240DCKR	SN74LVC1G86DCKR	
SN74LVC1G08DCKR.A	SN74LVC1G32DCKR	SN74LVC1G86DCKR.B	

SN74LVC1G125DCKR	SN74LVC1G32DCKR.B	
SN74LVC1G125DCKR. B	SN74LVC1G38DCKR	

Qualification Report

Approve Date 07-April-2026

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC1G08DCKR	Qual Device: SN74LVC1G125DCKR	Qual Device: SN74LVC1G132DCKR	Qual Device: SN74LVC1G138DCKR	QBS Process Reference: SN74LVC1G08DCKR	QBS Package Reference: T2S0801DCKRQ1	QBS Package Reference: LMV723DCKR	QBS Package Reference: LMV723ADCKR	QBS Package Reference: SN74LVC1G125DCKRQ1	QBS Product Reference: SN74LVC1G08DCKRQ1	QBS Product Reference: SN74LVC1G125DCKRQ1	QBS Product Reference: SN74LVC1G132DCKRQ1	QBS Product Reference: SN74LVC1G138DCKRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	-	-	-	30310	-	-	1770	-	-	-	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	-	-	-	-	-	-	-	-	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	-	30310	30310	30310	1770	-	-	-	1770
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	-	-	-	30310	30310	30310	1770	-	-	-	1770
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	-	31350	-	-	1450	-	-	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	-	-	30310	-	-	-	-	-	-	-	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	-	-	-	-	-	-	-	-	-	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	-	-	-	304000	-	-	-	-	-	-	-
SD	C3	IPB Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	-	1150	-	-	-	-	-	-	-	-
SD	C3	IPB-free Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	-	-	1150	1150	1220	-	-	-	-	-	-
PD	C4	Physical Dimensions	Cpk=1.67	-	-	-	-	-	3000	3000	-	-	1000	1000	-	-	1000
ESD	E2	ESD CDM	-	500 Volts	-	-	-	-	-	-	-	-	-	100	100	100	100
ESD	E2	ESD HBM	-	2000 Volts	-	-	-	-	-	-	-	-	-	100	100	100	100
LU	E4	Latch-Up	Per JESD78	-	-	-	-	-	-	-	-	-	-	100	100	100	100
CHAR	E5	Electrical Distributions	Cpk=1.67 Floor, hot, and cold	-	-	-	-	-	-	-	-	-	-	1000	1000	1000	-
FTY	E6	Final Test Yield	-	-	1000	-	-	-	-	-	-	-	-	-	-	-	-

QBS: Qual By Similarity, also known as Generic Data

Qual Device SN74LVC1G08DCKR is qualified at MSL1 260C

Qual Device SN74LVC1G125DCKR is qualified at MSL1 260C

Qual Device SN74LVC1G38DCKR is qualified at MSL1 260C

Qual Device SN74LVC1G132DCKR is qualified at MSL1 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2603-026

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.