12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN Number:	20260713003.2	PCN Issued	July 14, 2026
Qualifying a Design change, Data sheet update, Clark-PR as an additional wafer Probe Test site, BOM update and TIEM as an additional Assembly/Test site option for select devices		Sample request deadline:	September 12, 2026
		Estimated 1st ship date:	January 10, 2027
Sample requests received after** September 12, 2026 will not be supported.**			

Change type(s)	ZVEI ID(s)
Assembly Site Assembly Material Packing/Shipping/Labeling Design Data Sheet/Electrical Specification Test Site	SEM-PA-18, SEM-DS-01, SEM-DE-02, SEM-PS-02, SEM-PA-03, SEM-PA-05, SEM-PA-07, SEM-PA-11, SEM-TF-01

PCN Details

Description of Change:

Texas Instruments is pleased to announce a die design, Clark-PR as an additional wafer Probe Test site, BOM update and TIEM as additional Assembly/Test site options for the select devices listed below.

	Current Site	Additional Site
Wafer probe Test site	CD-PR	CLARK-PR

Construction differences as follows:

Group 1 device

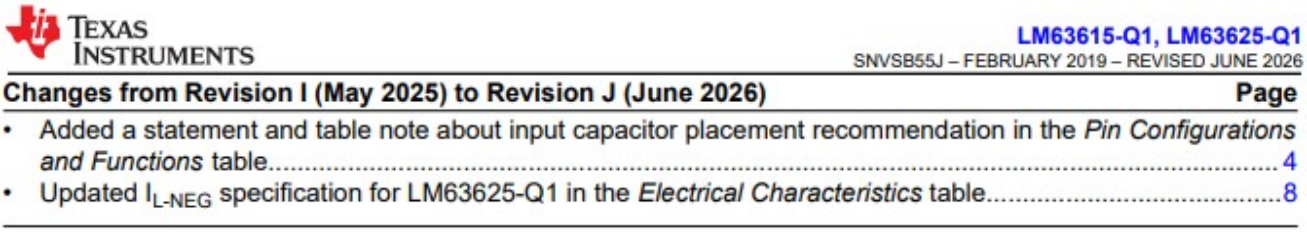
	Current site	BOM update	Additional Site
Assembly/Test site	MLA	MLA	TIEM
Mount compound	4208458	4211470	4211470
Mold compound	4211649	4211649	4228573
Lead finish	NiPdAu	NiPdAu	Matte Sn
MSL level	3	3	1

Group 2 device

	Current site	Additional Site
Assembly/Test site	TAI	TIEM
Mold compound	4211649	4228573
Lead finish	NiPdAu	Matte Sn
MSL level	3	1

The datasheets will be changing as a result of the above mentioned changes.

The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.



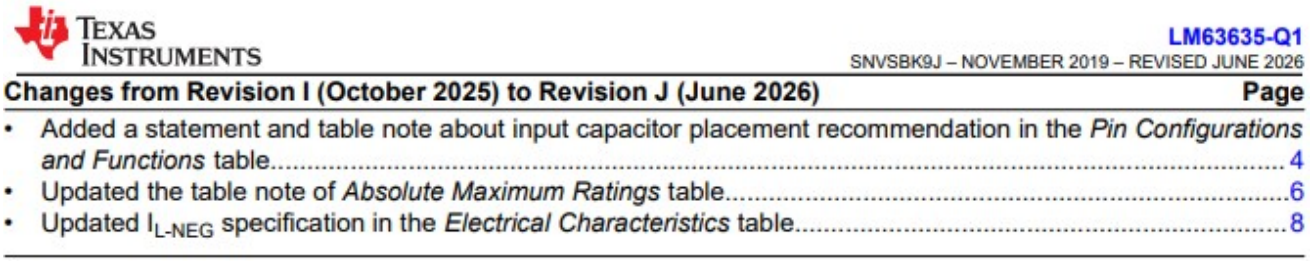
TEXAS INSTRUMENTS

LM63615-Q1, LM63625-Q1

SNVSB55J – FEBRUARY 2019 – REVISED JUNE 2026

Changes from Revision I (May 2025) to Revision J (June 2026) **Page**

- Added a statement and table note about input capacitor placement recommendation in the *Pin Configurations and Functions* table.....4
- Updated I_{L-NEG} specification for LM63625-Q1 in the *Electrical Characteristics* table.....8



TEXAS INSTRUMENTS

LM63635-Q1

SNVSBK9J – NOVEMBER 2019 – REVISED JUNE 2026

Changes from Revision I (October 2025) to Revision J (June 2026) **Page**

- Added a statement and table note about input capacitor placement recommendation in the *Pin Configurations and Functions* table.....4
- Updated the table note of *Absolute Maximum Ratings* table.....6
- Updated I_{L-NEG} specification in the *Electrical Characteristics* table.....8

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
LM636x5-Q1	SNVSB55I	SNVSB55J	http://www.ti.com/product/LM63615-Q1
LM63635-Q1	SNVSBK9I	SNVSBK9J	http://www.ti.com/product/LM63635-Q1

Qual details are provided in the Qual Data Section.
Test coverage, insertions, conditions will remain consistent with current testing.

Reason for Change:	Improve robustness under corner-case application conditions. Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability:	Review the updated datasheets and/or Standard Data Packet for more details on the changes
Impact on Environmental Ratings	Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:	**Assembly Site Information**

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City

MLA	MLA	MYS	Kuala Lumpur
TAI	TAI	TWN	Chung Ho, New Taipei City
TIEM	**CU6**	**MYS**	**Melaka**

Sample product shipping label (not actual product label):

Group 1 Products Affected: (Design, Probe site, Data sheet, Assembly/Test site)

LM63610DQPWPRQ1	LM63625DQPWPRQ1*
LM63615DQPWPRQ1*	LM63635DQPWPRQ1*

*With Data Sheet change

Group 2 Products Affected: (Assembly/Test site only)

DRV8876QPWPRQ1	DRV8876QPWPRQ1.A

Automotive Qualification Summary
(As per AEC-Q100 and JEDEC Guidelines)

Approve Date 26-February-2026

Note: Minor silicon die revision for all assembly sites – TI Qualification R-NPD-2512-048 *
*Die revision was localized routing change to internal logic circuits to address bug fix. Change does not impact reliability or alter device specific data.

Product Attributes

Attributes	Qual Device LM636xxxxQDRRQ1 CLARK-AT / CDAT assembly	Qual Device LM636xxxDQPWPQ1 TIEMA assembly	Qual Device LM636xxxDQPWPQ1 MLA assembly	Original Q100 qualification: LM636xxDQDRRQ1 CDAT assembly	Original Qualification: LM636xxQPWPQ1 MLA assembly	QBS for ELFR LMR33620CQRNXTQ1
Automotive Grade Level	Grade 1					Grade 1
Operating Temp Range	-40 to +125 C					-40 to +125 C
Product Function	Power Management					Power Management
Die Attributes	-	-		-	-	-
Wafer Fab Supplier	RFAB					RFAB
Wafer Process ID	LBC9					LBC9
Package Attributes	-	-		-	-	-
Assembly Site	CLARK	TIEMA	MLA	CDAT	MLA	UTL1
Package Type	QFN/SON	HTSSOP	HTSSOP	QFN/SON	HTSSOP	QFN/SON

Package Designator	DRR	PWP	PWP	DRR	PWP	RNX
Ball/Lead Count	12	16	16	12	16	12
Package Size (mils)	118.11 X 118.11	196.85 X 173.23	196.85 X 173.23	118.11 X 118.11	196.85 X 173.23	
Body Thickness (mils)	31.5	47.24	47.24	31.5	47.24	
Ball/Lead Pitch (mils)	19.7	25.59	25.59	19.7	25.59	
Leadframe Plating Composition	NiPdAu	Matte Sn	NiPdAu	NiPdAu	NiPdAu	

- QBS: Qual By Similarity

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

	Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device LM636xxxQDRRRQ1 / LM636xxxDQPWPRQ1	QBS Product Reference: LM63625DQDRRQ1	QBS Product Reference: LM63635DQPWPQ1	QBS Process ELFR Reference: LMR33620CQRNXTQ1
Test Group A – Accelerated Environment Stress Tests											
	PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 2 - 260	Refer to R-CHG-2410-069 for DRR in Clark-AT, R-CHG-2405-009 for PWP in TIEMA and R-CHG-2403-108 in MLA.	Pass Level 2-260C	Pass Level 3-260C	-
	HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours		3/231/0	3/231/0	-
	uHAST	A3	JEDEC JESD22-A102	3	77	Unbiased HAST 130C	96 Hours		3/231/0	3/231/0	-
	TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles		3/231/0	3/231/0	-
	TC-BP		MIL-STD883 Method 2011	1	30	Post 500 Temp. Cycle, Bond Pull	Wires		1/30/0	1/5/0	-
	PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle, -40/125C	1000 Cycles	N/A per Q100 rev J	N/A	1/45	-
	HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake, 175C or 150C	500 Hours 1000 hours	Refer to R-CHG-2410-069 for DRR in Clark-AT, R-CHG-2405-009 for PWP in TIEMA and R-CHG-2403-108 in MLA.	1/45/0	3/231/0	-
Test Group B – Accelerated Lifetime Simulation Tests											
	HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 150C	408 Hours	Device specific data	1/77/0	3/231/0	-
	ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	QBS to technology ELFR	QBS	QBS	3/2400/0
	EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A	N/A	N/A	N/A
Test Group C – Package Assembly Integrity Tests											
	WBS	C1	AEC Q100-001	1	30	Bond Shear (Cpk>1.67)	Wires	Refer to R-CHG-2410-069 for DRR in Clark-AT, R-CHG-2405-009 for PWP in TIEMA and R-CHG-2403-108 in MLA.	1/30/0	1/30/0 Pass	-
	WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires		1/30/0	1/30/0 Pass	-
	SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	-		1/15/0	1/15/0	-
	PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-		3/30/0	3/30/0	-
	SBS	C5	AEC Q100-010	3	50	Solder Ball Shear (Cpk>1.67)	Solder Balls	N/A	N/A	N/A	N/A
Test Group D – Die Fabrication Reliability Tests											
	EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements			
	TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	Completed Per Process Technology Requirements			
	HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology Requirements			
	NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements			
	SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements			
Test Group E – Electrical Verification Tests											
	HBM	E2	AEC Q100-002	1	3	ESD - HBM	2000V	Device specific data from original DRR and PWP Q100 qualifications	1/3/0	1/3/0	-
	CDM	E3	AEC Q100-011	1	3	ESD - CDM	750V	Device specific data from original DRR / PWP packages	1/3/0	1/3/0	-
	LU	E4	AEC Q100-004	1	6	Latch-up	(Per AED Q100-004)	Device specific data from original DRR / PWP packages	1/6/0	1/6/0	-
	ED	E5	AEC Q100-005	3	30	Electrical Distribution	Cpk>1.6 Room, Hot, & Cold	Device specific data from original DRR / PWP packages	3/30/0	3/30/0	-

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.
Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I) : -40°C to +85°C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Green/Pb-free Status:
Qualified Pb-Free(SMT) and Green
TI Qualification ID: 20201212-137488, R-NPD-2512-048

Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 02-December-2025

Product Attributes

Attributes	Qual Device: DRV8876QPWPRQ1	QBS Process Reference: DRV8873SPWPRQ1
Automotive Grade Level	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain
Wafer Fab Supplier	RFAB	RFAB
Assembly Site	TIEMA	TAI
Package Group	TSSOP	TSSOP
Package Designator	PWP	PWP
Pin Count	16	24

QBS: Qual By Similarity, also known as Generic Data
Qual Device DRV8876QPWPRQ1 is qualified at MSL1 260C
Per AEC-Q100J A1.3: The PCN devices are categorized as a qualification family and QBS to DRV8876QPWPRQ1 Group A data for the critical attributes in Die sizes,
Package Type, Assembly Process and Site
Note 1: Qual device and affected devices in PCN have justification to use Process QBS references for HTOL and ELFR based on AEC-100J A1.2 silicon wafer fab and
process attributes were qualified. Group B test purpose is for silicon defects, they do not get influenced by assembly site or BOM differences.
Note 2: One lot ED is allowed per AEC-Q100J A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one
wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: DRV8876QPWPRQ1	QBS Process Reference: DRV8873SPWPRQ1
Test Group A - Accelerated Environment Stress Tests									
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/231/0	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5//0	
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	3/36/0	-
PTC	A5	JEDEC JESD22-A105	1	45	PTC	-40/125C	1000 Cycles	N/A	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-
Test Group B - Accelerated Lifetime Simulation Tests									
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 1	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 1	3/2400/0
Test Group C - Package Assembly Integrity Tests									
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-
Test Group D - Die Fabrication Reliability Tests									
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests									
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 2	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site:
TI Qualification ID: R-CHG-2405-009

Automotive Qualification Summary (As per AEC and JEDEC Guidelines)

Q006 TSSOP at TIEMA

Approve Date 02-December-2025

Product Attributes

Attributes	Qual Device: DRV8876QPWPRQ1
Automotive Grade Level	Grade 1
Operating Temp Range (C)	-40 to 125
Product Function	Signal Chain
Wafer Fab Supplier	RFAB
Assembly Site	TIEMA
Package Group	TSSOP
Package Designator	PWP
Pin Count	16

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: DRV8876QPWPRQ1
Test Group A - Accelerated Environment Stress Tests								
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/231/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	-	-
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	-
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	-
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	-
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0

HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	Completed	3/9/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	Completed	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	Completed	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	-
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	-	-
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	-
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	-
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	-
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0
PTC	A5.1	JEDEC JESD22-A105	1	45	PTC	-40/125C	1000 Cycles	N/A
PTC	A5.2	JEDEC JESD22-A105	1	45	PTC	-40/125C	2000 Cycles	N/A
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	-	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0
Test Group C - Package Assembly Integrity Tests								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0

Qual Device DRV8876QPWPRQ1 is qualified at MSL1 260C
This report represents AEC-Q006 7.1 Family Data Usage using technology driver and lead products that are most representative of the technology family.
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site:
TI Qualification ID: R-CHG-2405-009

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.