



12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN Number:	20260709000.1	PCN Issued	July 09, 2026
Qualification of RFAB as an additional Fab site, Die Revision, Datasheet and BOM options for select devices		Sample request deadline:	September 07, 2026
		Estimated 1st ship date:	October 07, 2026
Sample requests received after September 07, 2026 will not be supported.			

Change type(s)

Assembly Material
Packing/Shipping/Labeling
Design
Data Sheet/Electrical Specification
Wafer Fab Site
Wafer Fab Material
Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of RFAB as an additional Fab site, Die Revision, Datasheet & BOM options for the devices listed below.

Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter
FFAB	ASLC10	200mm	RFAB	LBC9	300mm

The die was also changed as a result of the process change.

Construction Differences are as follows:

	Current	Additional
Wire diam/type	0.96mil Cu	0.8mil Cu

Data sheet update

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

Changes from July 1, 2014 to June 25, 2026 (from Revision L (July 2014) to Revision M (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Moved ESD ratings to <i>ESD Ratings</i> table.....	1
• Updated latch-up ratings to latest standards.....	1
• Updated <i>Device Information</i> format and included package size.....	1
• Updated <i>Simplified Schematic</i>	1
• Updated <i>Applications</i>	1
• Added DGS and RKS package information.....	1
• Added DGS and RKS package information.....	2
• Added <i>ESD Ratings</i> table.....	4
• Changed Junction-to-ambient thermal resistance value for PW package from: 102.5°C/W to: 120.3°C/W	5
• Changed Junction-to-case (top) thermal resistance value for PW package from: 35.9°C/W to: 62.5°C/W.....	5
• Changed Junction-to-board thermal resistance value for PW package from: 53.5°C/W to: 82.4°C/W.....	5
• Changed Junction-to-top characterization value for PW package from: 2.2°C/W to: 16.0°C/W.....	5
• Changed Junction-to-board characterization value for PW package from: 52.9°C/W to: 81.5°C/W.....	5
• Added DW, DB and NS package Thermal Information table.....	5
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	13
• Updated <i>Detailed Description, Application and Implementation</i> and <i>Device Documentation</i> sections.....	15

Changes from June 1, 2014 to June 17, 2026 (from Revision N (June 2014) to Revision O (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved ESD ratings to <i>ESD Ratings</i> table.....	1
• Updated latch-up ratings to latest standards.....	1
• Updated <i>Device Information</i> format and included package size.....	1
• Updated <i>Simplified Schematic</i>	1
• Updated <i>Applications</i>	1
• Added DGS and RKS package information.....	1
• Changed R0JA for DB package from: 112.1°C/W to: 121.7°C/W.....	6
• Changed R0JC(top) for DB package from: 73.6°C/W to: 86.8°C/W.....	6

• Changed Ψ_{JT} for DB package from: 67.3°C/W to: 87.8°C/W.....	6
• Changed Ψ_{JB} for DB package from: 33.3°C/W to: 44.7°C/W.....	6
• Changed R θ_{JC} (bot) for DB package from: 66.9°C/W to: 87°C/W.....	6
• Changed R θ_{JA} for DW package from: 99.4°C/W to: 114.8°C/W.....	6
• Changed R θ_{JC} (top) for DW package from: 66.9°C/W to: 84.1°C/W.....	6
• Changed Ψ_{JT} for DW package from: 66.9°C/W to: 88.8°C/W.....	6
• Changed Ψ_{JB} for DW package from: 33.8°C/W to: 55.8°C/W.....	6
• Changed R θ_{JC} (bot) for DW package from: 66.5°C/W to: 87.8°C/W.....	6
• Changed R θ_{JA} for NS package from: 90.3°C/W to: 116.3°C/W.....	6
• Changed R θ_{JC} (top) for NS package from: 56.6°C/W to: 82.4°C/W.....	6
• Changed Ψ_{JT} for NS package from: 57.8°C/W to: 86.2°C/W.....	6
• Changed Ψ_{JB} for NS package from: 28.7°C/W to: 43.9°C/W.....	6
• Changed R θ_{JC} (bot) for NS package from: 57.4°C/W to: 85.5°C/W.....	6
• Changed R θ_{JA} for PW package from: 100.8°C/W to: 120.3°C/W.....	6
• Changed R θ_{JC} (top) for PW package from: 35.2°C/W to: 62.5°C/W.....	6
• Changed Ψ_{JT} for PW package from: 51.8°C/W to: 82.4°C/W.....	6
• Changed Ψ_{JB} for PW package from: 2.2°C/W to: 16°C/W.....	6
• Changed R θ_{JC} (bot) for PW package from: 51.2°C/W to: 81.5°C/W.....	6
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	14



SN74LVC540A

SCAS2970 – JANUARY 1993 – REVISED JUNE 2026

Changes from May 1, 2014 to June 25, 2026 (from Revision N (May 2014) to Revision O (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved ESD ratings to <i>ESD Ratings</i> table.....	1
• Updated latch-up ratings to latest standards.....	1
• Deleted military disclaimers.....	1
• Updated <i>Device Information</i> format and included package size.....	1
• Updated <i>Simplified Schematic</i>	1
• Updated <i>Applications</i>	1
• Added DGS and RKS package information.....	1
• Added DGS and RKS packages to <i>Thermal Information</i> table.....	5
• Changed R θ_{JA} for DW package from: 88.3°C/W to: 114.8°C/W.....	5
• Changed R θ_{JC} (top) for DW package from: 51.1°C/W to: 84.1°C/W.....	5
• Changed Ψ_{JT} for DW package from: 50.9°C/W to: 88.8°C/W.....	5
• Changed Ψ_{JB} for DW package from: 20°C/W to: 55.8°C/W.....	5
• Changed R θ_{JC} (bot) for DW package from: 50.5°C/W to: 87.8°C/W.....	5
• Changed R θ_{JA} for PW package from: 102.5°C/W to: 120.3°C/W.....	5
• Changed R θ_{JC} (top) for PW package from: 35.9°C/W to: 62.5°C/W.....	5
• Changed Ψ_{JT} for PW package from: 53.5°C/W to: 82.4°C/W.....	5
• Changed Ψ_{JB} for PW package from: 2.2°C/W to: 16°C/W.....	5
• Changed R θ_{JC} (bot) for PW package from: 52.9°C/W to: 81.5°C/W.....	5
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	13



SN74LVC244A

SCAS414AG – NOVEMBER 1992 – REVISED JUNE 2026

Changes from February 2, 2026 to June 26, 2026 (from Revision AF (February 2026) to Revision AG (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed R θ JA for DB package from: 108.1°C/W to: 121.7°C/W.....	6
• Changed R θ JC(top) for DB package from: 70.2°C/W to: 86.8°C/W.....	6
• Changed Ψ JT for DB package from: 63.3°C/W to: 87.8°C/W.....	6
• Changed Ψ JB for DB package from: 30.6°C/W to: 44.7°C/W.....	6
• Changed R θ JA for DW package from: 90.9°C/W to: 114.8°C/W.....	6
• Changed R θ JC(top) for DW package from: 55.3°C/W to: 84.1°C/W.....	6
• Changed Ψ JT for DW package from: 58.8°C/W to: 88.8°C/W.....	6
• Changed Ψ JB for DW package from: 29.1°C/W to: 55.8°C/W.....	6
• Changed R θ JA for NS package from: 90.1°C/W to: 116.3°C/W.....	6
• Changed R θ JC(top) for NS package from: 56.4°C/W to: 82.4°C/W.....	6
• Changed Ψ JT for NS package from: 57.7°C/W to: 86.2°C/W.....	6
• Changed Ψ JB for NS package from: 28.4°C/W to: 43.9°C/W.....	6
• Changed R θ JA for PW package from: 114.7°C/W to: 120.3°C/W.....	6
• Changed R θ JC(top) for PW package from: 48.4°C/W to: 62.5°C/W.....	6
• Changed Ψ JT for PW package from: 65.6°C/W to: 82.4°C/W.....	6
• Changed Ψ JB for PW package from: 6.8°C/W to: 16°C/W.....	6
• Changed R θ JA for RGY package from: 50.3°C/W to: 82.84°C/W.....	6
• Changed R θ JC(top) for RGY package from: 58.4°C/W to: 88.73°C/W.....	6
• Changed Ψ JT for RGY package from: 28.3°C/W to: 56.81°C/W.....	6
• Changed Ψ JB for RGY package from: 4.9°C/W to: 32.37°C/W.....	6
• Changed R θ JC(bot) for RGY package from: 28.4°C/W to: 56.62°C/W.....	6



SN74LVCZ240A

SCES273I – JUNE 1999 – REVISED JUNE 2026

Changes from April 1, 2005 to June 24, 2026 (from Revision H (April 2005) to Revision I (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved ESD ratings to <i>ESD Ratings</i> table.....	1
• Updated latch-up ratings to latest standards.....	1
• Changed R θ JA for DW package from: 58°C/W to: 114.8°C/W.....	5
• Changed R θ JA for NS package from: 60°C/W to: 116.3°C/W.....	5
• Changed R θ JA for PW package from: 83°C/W to: 120.3°C/W.....	5
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	14



SN74LVCZ244A

SCES274J – MAY 1999 – REVISED JUNE 2026

Changes from October 1, 2014 to June 1, 2026 (from Revision I (October 2014) to Revision J (June 2026))

Page

• Add RKS package options.....	1
• Moved T_{stg} to <i>Absolute Maximum Ratings</i> table.....	4
• Change <i>Handling Ratings</i> to <i>ESD Ratings</i>	4
• Changed Junction-to-ambient thermal resistance value for PW package from: 103.5°C/W to: 120.3°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for PW package from: 37.9°C/W to: 62.5°C/W.....	5
• Changed Junction-to-board characterization value for PW package from: 54.5°C/W to: 82.4°C/W.....	5
• Changed Junction-to-top characterization value for PW package from: 3.3°C/W to: 16°C/W.....	5
• Changed Junction-to-board characterization value for PW package from: 53.9°C/W to: 81.5°C/W.....	5
• Updated <i>Overview, Application and Implementation, Device and Documentation Support</i> sections to extend detailed feature descriptions and more detailed information.	7
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately"	12

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
SN74LVC240A	SCAS293L	SCAS293M	http://www.ti.com/product/SN74LVC240A
SNx4LVC541A	SCAS298N	SCAS298O	http://www.ti.com/product/SN54LVC541A
SN74LVC540A	SCAS297N	SCAS297O	http://www.ti.com/product/SN74LVC540A
SN74LVC244A	SCAS414AF	SCAS414AG	http://www.ti.com/product/SN74LVC244A
SN74LVCZ240A	SCES273H	SCES273I	http://www.ti.com/product/SN74LVCZ240A
SN74LVCZ244A	SCES274I	SCES274J	http://www.ti.com/product/SN74LVCZ244A

Qual details are provided in the Qual Data Section.

Reason for Change:

Supply Continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability:

Physical aspects of the device have changed. Review updated datasheets and/or the Standard Data Packet for more details on the changes

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Fab Site Information

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
FFAB	TID	DEU	Freising
RFAB	RFB	USA	Richardson

Die Rev:

Current	New
Die Rev [2P]	Die Rev [2P]
A, E, P	A

Sample product shipping label (not actual product label):

Products Affected:			
SN74LVC240ADWR	SN74LVC244ADWRG4	SN74LVC541ADBR	
SN74LVC244ADBR	SN74LVC244ADWRE4	SN74LVC541ADBRG4	
SN74LVC244ADBRE4	SN74LVC244ANSR	SN74LVC541ADWR	
SN74LVC244ADBRG4	SN74LVC244ANSRG4	SN74LVC541ADWRE4	
SN74LVC244ADWR	SN74LVC540ADWR	SN74LVC541ANSR	

Qualification Report

FAB5 LD4 PCN 20 NS

Approve Date 03-November -2025

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC244ANSR	Qual Device: SN74LVC541ANSR	Process QBS Reference: SN74HCST4QEPWRQ1	Package QBS Reference: SN74LVC8T245NSR	Package QBS Reference: SN74LV244AQDGSRQ1	Package QBS Reference: SN74LV273AQDGSRQ1	Package QBS Reference: SN74LV541AQDGSRQ1	Product QBS Reference: SN74LVC9541APWRQ1	Process QBS Reference: SN74LVC240APWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	1/77/0	1/77/0	1/77/0	-	1/77/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	1/77/0	1/77/0	1/77/0	-	-
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	3/231/0	1/77/0	1/77/0	1/77/0	-	1/77/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	3/231/0	1/45/0	1/45/0	1/45/0	-	-
HTOL	B1	Life Test	125C	1000 Hours	-	-	3/231/0	-	1/77/0	-	-	-	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	-	-	-	-	-	1/77/0
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-	-	-	-
SD	C3	PB Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	-	1/15/0	-	-	-	-
SD	C3	PB-Free Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	-	1/15/0	-	-	-	1/15/0
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	-	1/10/0	1/10/0	1/10/0	-	1/10/0
ESD	E2	ESD CDM	-	250 Volts	1/3/0	-	1/3/0	-	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	-	-	1/3/0	-	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	-	1/6/0	-	1/6/0	1/6/0	1/6/0	1/3/0	1/3/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	1/30/0	3/90/0	-	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0

QBS: Qual By Similarity, also known as Generic Data

Qual Device SN74LVC244ANSR is qualified at MSL1 260C

Qual Device SN74LVC541ANSR is qualified at MSL1 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site:

<http://www.ti.com/>

TI Qualification ID: R-CHG-2409-092

Qualification Report

FAB5 LD4 PCN 20 DB

Approve Date 19-November-2025

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC244ADBR	Qual Device: SN74LVC541ADBR	Package QBS Reference: SN74HC574QPWQ1	Package QBS Reference: SN74LV244AODGSRQ1	Package QBS Reference: SN74LV273AODGSRQ1	Package QBS Reference: SN74LV541AODGSRQ1	Process QBS Reference: GD75232DBR	Process QBS Reference: SN74LVC9541APWRQ1	Product QBS Reference: SN74LVC240APWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	1/77/0	1/77/0	1/77/0	1/77/0	-	1/77/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	1/77/0	1/77/0	1/77/0	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	-	-	-	1/77/0	-	1/77/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	1/77/0	1/77/0	1/77/0	1/77/0	-	1/77/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	1/45/0	1/45/0	1/45/0	1/77/0	-	-
HTSL	A6	High Temperature Storage Life	175C	500 Hours	-	-	-	-	-	-	-	-	1/45/0
HTOL	B1	Life Test	125C	1000 Hours	-	-	3/231/0	1/77/0	-	-	-	-	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	-	-	-	-	-	1/77/0
SD	C3	PB Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	-	-	-	-	-
SD	C3	PB-Free Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	-	-	-	-	1/15/0
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	1/10/0	1/10/0	1/10/0	-	-	1/10/0
ESD	E2	ESD CDM	-	250 Volts	1/3/0	-	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	1000 Volts	-	-	1/3/0	1/3/0	1/3/0	1/3/0	-	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	-	1/6/0	1/6/0	1/6/0	1/6/0	-	1/3/0	1/3/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	1/30/0	3/90/0	1/30/0	1/30/0	1/30/0	-	1/30/0	1/30/0

QBS: Qual By Similarity, also known as Generic Data

Qual Device SN74LVC244ADBR is qualified at MSL1 260C

Qual Device SN74LVC541ADBR is qualified at MSL1 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2503-036

Qualification Report

FAB5 LD4 PCN 20 DW

Approve Date 19-November-2025

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC240ADWR	Qual Device: SN74LVC244ADWR	Package QBS Reference: SN74HCS74QPWRQ1	Package QBS Reference: SN74AHC244QDWRG4	Process/Product QBS Reference: SN74LS245DWR	Process QBS Reference: SN74LVC240APWRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	1/77/0	3/231/0	1/77/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	1/77/0	3/231/0	1/77/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	1/77/0	3/231/0	1/77/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	1/45/0	3/231/0	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	1/77/0	-	1/77/0
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-	-
SD	C3	PB Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	-	-	-
SD	C3	PB-Free Solderability	Precondition w.155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	-	1/15/0
PD	C4	Physical Dimensions	(per mechanical drawing)	-	-	-	-	2/10/0	-	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	1/10/0	-	1/10/0
ESD	E2	ESD CDM	-	250 Volts	-	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	1000 Volts	-	-	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	-	-	1/6/0	1/3/0	1/3/0	1/3/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	1/30/0	3/90/0	1/30/0	1/30/0	1/30/0

QBS: Qual By Similarity, also known as Generic Data

Qual Device SN74LVC240ADWR is qualified at MSL1 260C

Qual Device SN74LVC244ADWR is qualified at MSL1 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2503-035

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also

known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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