

PCN Number:	20251104000.1C	PCN Date:	August 06, 2026			
Title:	Qualification of RFAB using qualified Process Technology, Die Revision, Datasheet, and additional Assembly Site (CDAT & TIEMA) & BOM options for select devices					
Customer Contact:	Change Management Team	Dept:	Quality Services			
Proposed 1st Ship Date:	November 04, 2026	Sample requests accepted until:	October 05, 2026*			
*Sample requests received after October 05, 2026 will not be supported.						
Change Type:						
☒	Assembly Site	☒	Design			
☒	Assembly Process	☒	Data Sheet			
☒	Assembly Materials	☐	Part number change			
☐	Mechanical Specification	☐	Test Site			
☐	Packing/Shipping/Labeling	☐	Test Process			
☐		☐	Wafer Bump Material			
☐		☐	Wafer Bump Process			
☐		☒	Wafer Fab Site			
☐		☒	Wafer Fab Material			
☐		☒	Wafer Fab Process			
PCN Details						
Description of Change:						
Texas Instruments is pleased to announce the qualification of its RFAB fabrication facility using the LBC9PLV qualified process technology as an additional Wafer Fab option in addition to an Assembly Site/BOM options for the devices listed below.						
The Revision C is being issued to correct typo of LBC3 to LBC9PLV in description of Change and Probe Site from FFAB Probe to No Probe as the PCN Notification Revision A stated.						
Current Fab Site			Additional Fab Site			
Current Fab Site	Process	Wafer Diameter	Additional Fab Site			
FFAB	ASLC10 & ASLnonC10	200 mm	RFAB			
			LBC9PLV			
			300 mm			
	Current	New				
Probe Site	FFAB	None				
The die was also changed as a result of the process change.						
Die Rev [2P]	Die Rev [2P]					
D,G	A					
Construction differences are as follows:						
	Current Site	Current Site	Current Site	Current Site	Additional Site	Additional Site
Assembly Site	ASEWH	HFTF	HNA	TFME	CDAT	TIEMA
Wire diam/type	Au 1.0 mil Cu 0.8 mil	Cu 1.0 mil	Au 0.6 mil	Au 0.8 mil	Cu 0.8 mil	Cu 0.8 mil
Mold Compound	SID#402 0039A1	SID#R-27	SID#450 179	SID#R-07	4222198	4222198
Mount Compound	SID#112 0999A2	SID# A-03	SID#400 180	SID# A-03	4207123	4207123
Symbolization	Same	Same	Same	Same	Additional	Additional
Final Wafer Thickness	7.5 mils	7.5 mils	7.5 mils	7.5 mils	6.0 mils	7.5 mils
The datasheets will be changing as a result of the above mentioned changes. The datasheet						

change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

Changes from Revision AE (June 2025) to Revision AF (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 229°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W	5

Changes from Revision AA (June 2025) to Revision AB (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371.10°C/W ...	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W ..	5
• Changed Junction-to-board thermal resistance value for DCK package from: 70.9°C/W to: 258.2°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 47°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W	5

Changes from Revision AF (June 2025) to Revision AG (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W	5

Changes from Revision Z (June 2025) to Revision AA (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371.0°C/W	6
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W ..	6
• Changed Junction-to-board thermal resistance value for DCK package from: 70.9°C/W to: 258.6°C/W	6
• Changed Junction-to-top characterization value for DCK package from: 47.0°C/W to: 195.6°C/W	6
• Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W	6

Changes from Revision X (June 2025) to Revision Y (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 280°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 66°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 67°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 66°C/W to: 256.2°C/W	5

Changes from Revision N (June 2025) to Revision O (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W	5

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
SN74LVC1G04	SCES214AE	SCES214AF	http://www.ti.com/product/SN74LVC1G04
SN74LVC1G06	SCES295AA	SCES295AB	http://www.ti.com/product/SN74LVC1G06
SN74LVC1G07	SCES296AF	SCES296AG	http://www.ti.com/product/SN74LVC1G07
SN74LVC1G14	SCES218Z	SCES218AA	http://www.ti.com/product/SN74LVC1G14
SN74LVC1G17	SCES351X	SCES351Y	http://www.ti.com/product/SN74LVC1G17
SN74LVC1G34	SCES519N	SCES519O	http://www.ti.com/product/SN74LVC1G34

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are part of our multiyear plan to transition products from our 200-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

Any differences/changes between the ASLC10 & ASLnonC10 die and LBC9PLV die have been made in the data sheet using "Legacy silicon" ASLC10 & ASLnonC10 and "New silicon" (LBC9PLV).

Impact on Environmental Ratings:

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS

REACH

Green Status

IEC 62474

☒ No Change	☒ No Change	☒ No Change	☒ No Change
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Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
FFAB	TID	DEU	Freising
RFAB	RFB	USA	Richardson

Assembly/Test Site Information:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
HFTF	HFT	CN	Heifei
TFME	NFM	CHN	Economic Development Zone
UTL2	NS2	THA	Bangpakong, Chachoengsao
CDAT	CDA	CHN	Chengdu
TIEMA	CU6	MYS	Melaka

Sample product shipping label (not actual product label):

TEXAS
INSTRUMENTS
MADE IN: Malaysia
2DC: 2Q:



MSL 2 /260C/1 YEAR SEAL DT
MSL 1 /235C/UNLIM 03/29/04

OPT:
ITEM: 39
LBL: 5A (L)T0:1750

(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T) LOT: 3959047MLA
(4W) TKY (1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CS0: SHE (21L) CC0:USA
(22L) AS0: MLA (23L) AC0: MYS

Product Affected:

SN74LVC1G04DCKR	SN74LVC1G06DCKR	SN74LVC1G07DCKR	SN74LVC1G14DCKR
SN74LVC1G17DCKR	SN74LVC1G34DCKR		

Qualification Report

Approve Date 22-SEPTEMBER-2025

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC1G04DCKR	Qual Device: SN74LVC1G07DCKR	QBS Reference: SN74HCS74QPWRQ1	QBS Reference: TXS0101QDCKRQ1	QBS Reference: SN74LVC1G16DCKRQ1
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	3/231/0	1/77/0
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-
UHAST	A3	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	3/231/0	1/77/0
TC	A4	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	3/231/0	1/77/0
HTSL	A6	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	3/135/0	1/45/0
HTOL	B1	Life Test	125C	1000 Hours	-	-	3/231/0	3/231/0	-
HTOL	B1	Life Test	150C	300 Hours	-	-	-	-	1/77/0
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-
SD	C3	PB Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	-	-

Type	#	Test Name	Condition	Duration	Qual Device: SN74LVC1G04DCKRQ1	Qual Device: SN74LVC1G07DCKRQ1	QBS Reference: SN74HCS74QPWRQ1	QBS Reference: TXS0101QDCKRQ1	QBS Reference: SN74LVC1G16DCKRQ1
SD	C3	PB-Free Solderability	Precondition w/155C Dry Bake (4 hrs +/- 15 minutes)	-	-	-	1/15/0	1/15/0	-
PD	C4	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	3/30/0	1/10/0
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	1/3/0	1/3/0	1/6/0	1/6/0	1/3/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	1/30/0	-	-	-
CHAR	E5	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	-	3/90/0	3/90/0	1/30/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC1G04DCKR is qualified at MSL1 260C
- Qual Device SN74LVC1G07DCKR is qualified at MSL1 260C

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7 eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7 eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2411-055

**Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)**

**Q006 SOT-SC70 at TIEMA
Approve Date 12-October-2025**

Attributes	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Process Reference: SN74AUP1T34QDCKRQ1	QBS Process Reference: SN74LVC1G07QDCKRQ1	QBS Process Reference: SN74LVC2G14IDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic	Logic	Logic
Wafer Fab Supplier	FR-BIP-1	FR-BIP-1	MH8	FR-BIP-1	FR-BIP-1
Assembly Site	TIEMA	TIEMA	HFTFAT	HFTFAT	HFTFAT
Package Group	SOT	SOT	SOT	SOT	SOT
Package Designator	DCK	DCK	DCK	DCK	DCK
Pin Count	5	6	5	5	6

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Mn Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Reference: SN74AUP1T34QDCKRQ1	QBS Reference: SN74LVC1G07QDCKRQ1	QBS Reference: SN74LVC2G14IDCKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/0/0	-	-	-	-
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85% RH	96 Hours	3/231/0	-	-	-	-

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1607QDCRQ1	Qual Device: SN74LVC2617QDCRQ1	QBS Reference: SN74AUP1T34QDCRQ1	QBS Reference: SN74LVC1607QDCRQ1	QBS Reference: SN74LVC2614QDCRQ1
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85% RH	192 Hours	3/231/0	-	-	-	-
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150 C	500 Cycles	3/231/0	-	-	-	-
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150 C	1000 Cycles	3/231/0	-	-	-	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-	-	-	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	3/135/0	-	-	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/50/0	1/30/0	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD-883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/50/0	1/30/0	1/30/0	1/30/0	1/30/0

• QBS: Qual By Similarity, also known as Generic Data
 • Qual Device SN74LVC1607QDCRQ1 is qualified at MSL1260C
 • Qual Device SN74LVC2617QDCRQ1 is qualified at MSL1260C

• Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
 • The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
 • The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
 • The following are equivalent Temp Cycle options per JEDEC47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

• Grade 0 (or E) : -40C to +150C
 • Grade 1 (or Q) : -40C to +125C
 • Grade 2 (or T) : -40C to +105C
 • Grade 3 (or J) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

• Room/Hot/Cold : HTOL, ED

• Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
 • Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2410-028

Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Project Carbon: TIEM DCK
Approve Date 12-October-2025

Product Attributes

Attributes	Qual Device: SN74LVC1607QDCRQ1	Qual Device: SN74LVC2617QDCRQ1	QBS Process Reference: SN74AUP1T34QDCRQ1	QBS Process Reference: SN74LVC1607QDCRQ1	QBS Process Reference: SN74LVC2614QDCRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic	Logic	Logic
Wafer Fab Supplier	FR-BIP-1	FR-BIP-1	MH8	FR-BIP-1	FR-BIP-1
Assembly Site	TIEMA	TIEMA	HFTFAT	HFTFAT	HFTFAT
Package Group	SOT	SOT	SOT	SOT	SOT
Package Designator	DCK	DCK	DCK	DCK	DCK
Pin Count	5	6	5	5	6

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC1607QDCRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC2617QDCRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1607QDCRQ1	Qual Device: SN74LVC2617QDCRQ1	QBS Process Reference: SN74AUP1T34QDCRQ1	QBS Process Reference: SN74LVC1607QDCRQ1	QBS Process Reference: SN74LVC2614QDCRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/0/0	-	3/0/0	-	3/0/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1607QDCKRQ1	Qual Device: SN74LVC2G170DCKRQ1	QBS Process Reference: SN74AUP1T34QDCKRQ1	QBS Process Reference: SN74LVC1607QDCKRQ1	QBS Process Reference: SN74LVC2G140DCKRQ1
PC	A1	JED3C J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	2100	-
HAST	A2	JED3C JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	-	3/231/0	2/1540	3/231/0
ACIUHAST	A3	JED3C JESD22-A102/JED3C JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	2/1540	3/231/0
ACIUHAST	A3	JED3C JESD22-A102/JED3C JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JED3C JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	3/231/0	2/1540	3/231/0
HTSL	A6	JED3C JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	1/450	1/450
HTSL	A6	JED3C JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JED3C JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	1/77/0	1/770	1/770
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
SD	C3	JED3C J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/150
SD	C3	JED3C J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/150
PD	C4	JED3C JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	1/10/0	3/30/0	3/30/0	3/30/0
Test Group D - Die Fabrication Reliability Tests												
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1607QDCKRQ1	Qual Device: SN74LVC2G170DCKRQ1	QBS Process Reference: SN74AUP1T34QDCKRQ1	QBS Process Reference: SN74LVC1607QDCKRQ1	QBS Process Reference: SN74LVC2G140DCKRQ1
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirement	Completed Per Process Technology Requirement	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDD	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirement	Completed Per Process Technology Requirement	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirement	Completed Per Process Technology Requirement	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirement	Completed Per Process Technology Requirement	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirement	Completed Per Process Technology Requirement	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2500 Volts	-	-	-	-	1/30
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	1000 Volts	-	-	1/3/0	1/30	1/30
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	-	-	-	-	1/50
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	1/30/0	3/90/0	1/30/0	3/90/0
Additional Tests												
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable - The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours - The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours - The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles												

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2410-028

For alternate parts with similar or improved performance, please visit the product page on [TI.com](http://www.ti.com)

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