

PCN# 20251103004.2

**Qualification of RFAB using qualified Process Technology, additional Assembly Site & BOM options for select devices
Change Notification / Sample Request**

Date: November 10, 2025

To: MOUSER PCN

Dear Customer:

This is an announcement of a change to a device that is currently offered by Texas Instruments (TI). The details of this change are on the following pages, and are in alignment with our standard product change notification (PCN) [process](#).

TI requires acknowledgement of receipt of this notification within 60 days of the date of this notice. Lack of acknowledgement of this notice within 60 days constitutes acceptance and approval of this change. If samples or additional data are required, requests must be received within 60 days of this notification, given that samples are not built ahead of the change.

The Proposed First Ship date in this PCN letter is the earliest possible date that customers could receive the changed material. It is our commitment that the changed device will not ship before that date. If samples are requested within the 60 day sample request window, customers will still have 30-days to complete their evaluation regardless of the proposed 1st ship date.

Changes outlined in this notification underscore our commitment to product longevity and supply continuity, as well as our continued efforts to transition to newer, more efficient manufacturing processes and technologies. Specifically, this particular notification is related to TI's multiyear transition plan for our two remaining 150-millimeter production lines (DFAB in Dallas, Texas, and SFAB in Sherman, Texas). SFAB closure activities are expected to begin by the end of 2025. DFAB will remain open with a smaller set of 200mm technologies and GaN.

For questions regarding this notice or to provide acknowledgement of this PCN, you may contact your local Field Sales Representative or the Change Management team. For sample requests or sample related questions, contact your local Field Sales Representative. As always, we thank you for your continued business.

TI values customer engagement and feedback related to TI changes. Customers should contact TI if there are questions or concerns regarding a change notification.

Change Management Team
SC Business Services

20251103004.2
Attachment: 1

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records, you have recently purchased these devices. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
SN74LVC1G04QDCKRQ1	SN74LVC1G04QDCKRQ1
SN74LVC1G07QDCKRQ1	NULL
SN74LVC1G17QDCKRQ1	SN74LVC1G17QDCKRQ1

Technical details of this Product Change follow on the next page(s).

PCN Number:	20251103004.2	PCN Date:	November 10, 2025
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Title:	Qualification of RFAB using qualified Process Technology, Die Revision and additional Assembly Site & BOM options for select devices		
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Customer Contact:	Change Management team	Dept:	Quality Services
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Proposed 1st Ship Date:	May 09, 2026	Sample requests accepted until:	January 09, 2026*
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***Sample requests received after January 09, 2026 will not be supported.**

Change Type:					
<input checked="" type="checkbox"/>	Assembly Site	<input checked="" type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input checked="" type="checkbox"/>	Test Site	<input checked="" type="checkbox"/>	Wafer Fab Materials
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input checked="" type="checkbox"/>	Test Process	<input checked="" type="checkbox"/>	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the addition of RFAB using the LBC9 qualified process technology and additional Assembly/Test Site) and BOM options for the devices listed below.

Current Fab Site			Additional Fab Site		
Current Fab Site	Process	Wafer Diameter	Additional Fab Site	Process	Wafer Diameter
FFAB	ASLC10 & ASLnonC10	200 mm	RFAB	LBC9PLV	300 mm

The die was also changed as a result of the process change.

	Current	New
Probe Site	FFAB	None

Die Rev:

Current

Die Rev [2P]	Die Rev [2P]
D,G	A

Construction differences are as follows:

	Current Site	Current Site	Current Site	Additional Site	Additional Site
Assembly Site	HFTF	TFME	UTL2	CDAT	TIEMA
Wire diam/type	Au 0.8 mil	Au 0.8 mil	Au 1.0 mil	Cu 0.8 mil	Cu 0.8 mil
Mold Compound	SID#R-27	SID#R-07	SID#CZ0096	4222198	4222198
Mount Compound	SID# A-03	SID# A-03	SID#PZ0001	4207123	4207123
Symbolization	Same	Same	Same	Additional	Additional
Final Wafer Thickness	7.5 mils	7.5 mils	8 mils	6.0 mils	7.5 mils

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

Changes from Revision E (June 2025) to Revision F (October 2025) Page

- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371.0°C/W 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W 5
- Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W 5
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W 5

Changes from Revision C (June 2025) to Revision D (October 2025) Page

- Changed Junction-to-ambient thermal resistance value for DCK package from: 301.2°C/W to: 371.0°C/W 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 186.5°C/W to: 297.5°C/W.. 5
- Changed Junction-to-board thermal resistance value for DCK package from: 111.8°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 78.3°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 110.6°C/W to: 256.2°C/W..... 5

Changes from Revision D (April 2025) to Revision E (October 2025) Page

- Changed Junction-to-ambient thermal resistance value for DCK package from: 258°C/W to: 371.0°C/W 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 66°C/W to: 297.5°C/W..... 5
- Changed Junction-to-board thermal resistance value for DCK package from: 67°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 66°C/W to: 256.2°C/W..... 5

Changes from Revision D (June 2025) to Revision E (October 2025) Page

- Changed Junction-to-ambient thermal resistance value for DCK package from: 280°C/W to: 371.0°C/W 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 66°C/W to: 297.5°C/W..... 5
- Changed Junction-to-board thermal resistance value for DCK package from: 67°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 66°C/W to: 256.2°C/W..... 5

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
SN74LVC1G04-Q1	SCES482E	SCES482F	http://www.ti.com/product/SN74LVC1G04-Q1
SN74LVC1G07-Q1	SCES826C	SCES826D	http://www.ti.com/product/SN74LVC1G07-Q1
SN74LVC1G14-Q1	SCES865D	SCES865E	http://www.ti.com/product/SN74LVC1G14-Q1
SN74LVC1G17-Q1	SCES663D	SCES663E	http://www.ti.com/product/SN74LVC1G17-Q1

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ.

Qual details are provided in the Qual Data Section.

Reason for Change:

These changes are part of our multiyear plan to transition products from our 150-millimeter and 200-millimeter factories to newer, more efficient manufacturing processes and technologies, underscoring our commitment to product longevity and supply continuity.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive /

negative):

None

Impact on Environmental Ratings:

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
<input checked="" type="checkbox"/> No Change			

Changes to product identification resulting from this PCN:

Fab Site Information:

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
FFAB	TID	DEU	Freising
RFAB	RFB	USA	Richardson

Assembly/Test Site Information:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
HFTF	HFT	CN	Heifei
TFME	NFM	CHN	Economic Development Zone
UTL2	NS2	THA	Bangpakong, Chachoengsao
CDAT	CDA	CHN	Chengdu
TIEMA	CU6	MYS	Melaka

Sample product shipping label (not actual product label)

Product Affected-

SN74LVC1G04QDCKRQ1	SN74LVC1G07QDCKRQ1	SN74LVC1G14QDCKRQ1
SN74LVC1G17QDCKRQ1		

For alternate parts with similar or improved performance, please visit the product page on TI.com

**Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)**

**Q006 SOT-SC70 at TIEMA
Approve Date 12-October-2025**

Attributes	Qual Device:	Qual Device:	QBS Process Reference:	QBS Process Reference:	QBS Process Reference:
	SN74LVC1G07QDCKRQ1	SN74LVC2G17QDCKRQ1	SN74AUP1T34QDCKRQ1	SN74LVC1G07QDCKRQ1	SN74LVC2G14IDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic	Logic	Logic
Wafer Fab Supplier	FR-BIP-1	FR-BIP-1	MH8	FR-BIP-1	FR-BIP-1
Assembly Site	TIEMA	TIEMA	HFTFAT	HFTFAT	HFTFAT
Package Group	SOT	SOT	SOT	SOT	SOT
Package Designator	DCK	DCK	DCK	DCK	DCK
Pin Count	5	6	5	5	6

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Reference: SN74AUP1T34QDCKRQ1	QBS Reference: SN74LVC1G07QDCKRQ1	QBS Reference: SN74LVC2G14IDCKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/0/0	-	-	-	-
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/R5%RH	96 Hours	3/231/0	-	-	-	-

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Reference: SN74AUP1T34QDCKRQ1	QBS Reference: SN74LVC1G07QDCKRQ1	QBS Reference: SN74LVC2G14IDCKRQ1
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/231/0	-	-	-	-
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	-	-	-
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/231/0	-	-	-	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-	-	-	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	3/135/0	-	-	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC1G07QDCKRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC2G17QDCKRQ1 is qualified at MSL1 260C
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED

- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2410-028

**Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)**

**Project Carbon: TIEM DCK
Approve Date 12-October-2025**

Product Attributes

Attributes	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Process Reference: SN74AUP1T34QDCKRQ1	QBS Process Reference: SN74LVC1G07QDCKRQ1	QBS Process Reference: SN74LVC2G14IDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic	Logic	Logic
Wafer Fab Supplier	FR-BIP-1	FR-BIP-1	MH8	FR-BIP-1	FR-BIP-1
Assembly Site	TIEMA	TIEMA	HFTFAT	HFTFAT	HFTFAT
Package Group	SOT	SOT	SOT	SOT	SOT
Package Designator	DCK	DCK	DCK	DCK	DCK
Pin Count	5	6	5	5	6

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC1G07QDCKRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC2G17QDCKRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G07QDCKRQ1	Qual Device: SN74LVC2G17QDCKRQ1	QBS Process Reference: SN74AUP1T34QDCKRQ1	QBS Process Reference: SN74LVC1G07QDCKRQ1	QBS Process Reference: SN74LVC2G14IDCKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/0/0	-	3/0/0	-	3/0/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	Qual Device:	QBS Process Reference:	QBS Process Reference:	QBS Process Reference:
								SN74LVC1G07DCKR01	SN74LVC2G17DCKR01	SN74AUP1T34DCKR01	SN74LVC1G07DCKR01	SN74LVC2G14DCKR01
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	2/0/0	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	-	3/231/0	2/154/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A11B	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	2/154/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A11B	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	3/231/0	2/154/0	3/231/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	1/45/0	1/45/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	1/77/0	1/77/0	1/77/0
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0	1/30/0	1/30/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	1/10/0	3/30/0	3/30/0	3/30/0
Test Group D - Die Fabrication Reliability Tests												
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	Qual Device:	QBS Process Reference:	QBS Process Reference:	QBS Process Reference:
								SN74LVC1G07DCKR01	SN74LVC2G17DCKR01	SN74AUP1T34DCKR01	SN74LVC1G07DCKR01	SN74LVC2G14DCKR01
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements				
TDD	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements				
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements				
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements				
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements				
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2500 Volts	-	-	-	-	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	1000 Volts	-	-	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	-	-	-	-	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	1/30/0	3/90/0	1/30/0	3/90/0
Additional Tests												

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or J) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/HAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2410-028

**Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)**

**Q006 SOT at CDAT
Approve Date 22-SEPTEMBER-2025**

Attributes	Qual Device:	Qual Device:	QBS Package Reference:
	SN74LVC1G04QDCKRQ1	SN74LVC1G07QDCKRQ1	TXS0101QDCKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB
Assembly Site	CDAT	CDAT	CDAT
Package Group	SOT	SOT	SOT
Package Designator	DCK	DCK	DCK
Pin Count	5	5	6

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G04QDCKRQ1	Qual Device: SN74LVC1G07QDCKRQ1	QBS Reference: TXS0101QDCKRQ1
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	3/0/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	-	-	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	-	-	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-	-	3/3/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	-	-	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	-	-	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	-	-	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	-	-	3/231/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	-	-	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	-	-	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	-	-	3/9/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G04QDCKRQ1	Qual Device: SN74LVC1G07QDCKRQ1	QBS Reference: TXS0101QDCKRQ1
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	-	-	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	-	-	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	-	-	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	-	-	3/3/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	-	-	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	-	-	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	-	-	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	-	-	3/231/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	-	-	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	-	-	3/3/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G04QDCKRQ1	Qual Device: SN74LVC1G07QDCKRQ1	QBS Reference: TXS0101QDCKRQ1
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	-	-	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	-	-	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	-	-	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	-	-	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	-	-	3/135/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	-	-	3/3/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/9/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/9/0

- QBS: Qual By Similarity, also known as Generic Data
- Qual Device SN74LVC1G04QDCKRQ1 is qualified at MSL1 260C
- Qual Device SN74LVC1G07QDCKRQ1 is qualified at MSL1 260C
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

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TI Qualification ID: R-CHG-2411-054

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LVC1G04QDCKRQ1	Qual Device: SN74LVC1G07QDCKRQ1	QBS Process Reference: SN74HCS74QPWRQ1	QBS Package Reference: TXS0101QDCKRQ1	QBS Product Reference: SN74LVC1G16DCKRQ1
Test Group A - Accelerated Environment Stress Tests												

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	Qual Device:	QBS Process Reference:	QBS Package Reference:	QBS Product Reference:
								SN74LVC1G04QDCKRQ1	SN74LVC1G07QDCKRQ1	SN74HCS74QPWRQ1	TXS0101QDCKRQ1	SN74LVC1G16DCKRQ1
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	-	3/0/0	3/0/0	1/0/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	3/231/0	3/231/0	1/77/0
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	3/231/0	-	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	-	3/231/0	1/77/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	-	3/231/0	3/231/0	1/77/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-	-	-	1/5/0	1/5/0
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	-	-	-	1/12/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	3/135/0	1/45/0
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	3/231/0	3/231/0	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	-	-	-	-	1/77/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	3/90/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-	-	3/90/0	3/90/0	1/30/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device:	Qual Device:	QBS Process Reference:	QBS Package Reference:	QBS Product Reference:
								SN74LVC1G04QDCKRQ1	SN74LVC1G07QDCKRQ1	SN74HCS74QPWRQ1	TXS0101QDCKRQ1	SN74LVC1G16DCKRQ1
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	1/15/0	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	-	-	3/30/0	3/30/0	1/10/0
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements				
TDD	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements				
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements				
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements				
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements				
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	1/3/0	1/3/0	1/6/0	1/6/0	1/3/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	1/30/0	3/90/0	3/90/0	1/30/0
Additional Tests												

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TI Qualification ID: R-CHG-2411-054

ZVEI ID's: SEM-DE-03, SEM-PW-02, SEM-PW-03, SEM-PW-09, SEM-PW-13, SEM-BD-01, SEM-PA-03, SEM-PA-08, SEM-PA-11, SEM-PA-07, SEM-PA-13, SEM-PA-18, SEM-QG-01, SEM-TF-01

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